Gain-Enhanced Feedforward Path Compensation Technique for Pole–Zero Cancellation at Heavy Capacitive Loads

P. K. Chan and Y. C. Chen

***Abstract*—An improved frequency compensation technique is presented in this paper. It is based on a cascade of a voltage amplifier and a transconductor to form a composite gain-enhanced feedforward stage in a two-stage amplifier so as to broaden the gain bandwidth *via* low-frequency pole–zero cancellation at heavy capacitive loads, but yet without increasing substantial power consumption. The technique has been confirmed by the experimental results. An operational amplifier has been designed to drive a capacitive load of 300 pF. The amplifier exhibits a dc gain of 87 dB, a gain bandwidth of 10.4 MHz at 63.7° phase margin, an average slew rate of 3.5 V/μs, a compensation capacitor of only 6 pF while consuming 2.45 mW at a 3-V supply in a standard 0.6-μm CMOS technology.**

***Index Terms*—Feedforward transconductance amplifier, frequency compensation, pole–zero cancellation, two-stage CMOS amplifier.**

I. Introduction

AMPLIFIERS, making use of pole–zero cancellation techniques [1]–[9] at small or medium capacitive loads, have major advantages of bandwidth efficiency, low power, and small die size. These successful designs have been used extensively for robust and low-cost analog signal processing applications. However, for heavy capacitive load (> 100 pF) in low-power implementation, the compensation zero will be needed to shift to very low frequency at the left-hand-plane (LHP) for pole–zero cancellation. As a consequence, in standard *RC* Miller amplifiers [1]–[5], this requires large values of the zero-nulling resistor and compensation capacitor. However, the parasitic pole formed by the zero-nulling resistor together with parasitic capacitance would limit the extension of bandwidth. In feedforward-based amplifiers [6]–[9], maintaining high bandwidth at high capacitive loads needs substantial increase of feedforward transconductance for counteracting the right-hand plane (RHP) zero, and hence, higher power consumption. This is due to the fact that the structures may not be suitable for tradeoff between gain bandwidth and power dissipation at high capacitive loads. Based on these observations, this raises the motivation in devising an improved compensation methodology to meet the challenges for low-power bandwidth efficiency as well as small silicon area in amplifier design targeted for high capacitive loads.

To achieve the objectives, an amplifier incorporating gain-enhanced feedforward path compensation (GFPC) technique is proposed. This is based on adding a wide-band gain-enhanced voltage amplifier, with low output impedance, before a transconductance stage in the feedforward path of the conventional two-stage amplifier. Hence, the overall feedforward transconductance is enhanced by a gain factor of A_V. The result of which improves the amplifier performance on maximizing bandwidth at the low power constraint together with only small compensation capacitance to keep the amplifier stable.

This paper describes the *RC* Miller compensation technique (RCMC) in Section II. Multipath Miller zero cancellation compensation (MMZCC) technique and the conceptual circuit, together with its example using current push–pull topology are presented in Section III. The proposed GFPC technique and its analysis are described in Section IV. Section V details the implementation of the structure. This is then followed by experimental results, discussions, and performance comparisons in Section VI. Finally, the concluding remarks are given in Section VII.

II. *RC* Miller Compensation (RCMC)

In a classical two-stage operational amplifier, the RHP zero resulting from the feedforward path through the compensation capacitor tends to limit the gain bandwidth (GBW) by introducing extra phase lag. The RHP zero can be blocked *via* either inserting a voltage buffer [3] or a current buffer [10]. Alternatively, another economical approach is to insert a nulling resistor R_C in series with C_c [1]–[3] as shown in Fig. 1. The transfer function is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{-g_{m1}g_{m2}R_1R_2\left[1+sC_C\left(R_C-\frac{1}{g_{m2}}\right)\right]}{(1+sR_CC_1)(1+sg_{m2}R_2R_1C_C)\left(1+s\frac{C_L}{g_{m2}}\right)} \quad (1)$$

where the symbols have their usual meanings and the assumptions are that: 1) each gain stage is greater than one, $g_{mi}R_i >> 1$; 2) interstage coupling capacitances are neglected; and 3) the capacitive load or the compensation capacitor is much larger than the associated parasitic capacitances. It is important to note that these three assumptions are also made for the derivation of the transfer functions for other prior-art circuits in Section III and the proposed amplifier topology in Section IV.

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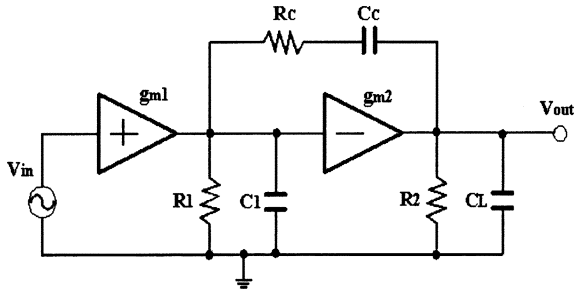

Fig. 1. *RC* miller compensation topology (RCMC).

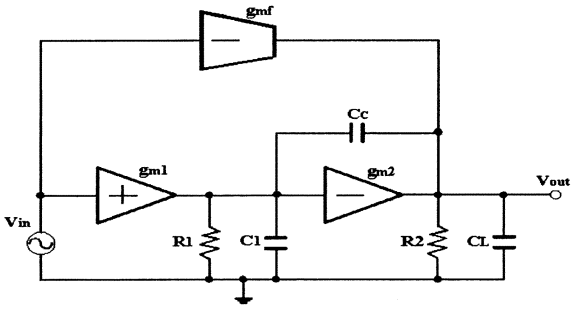

Fig. 2. MMZCC.

From (1), there are three LHP poles and one zero as follows:

$$P_1 \approx \frac{-1}{g_{m2}R_2R_1C_C} \tag{2}$$

$$P_2 \approx \frac{-g_{m2}}{C_L} \tag{3}$$

$$P_3 \approx \frac{-1}{R_CC_1} \tag{4}$$

$$Z_1 \approx \frac{-1}{C_C\left(R_C - \frac{1}{g_{m2}}\right)}. \tag{5}$$

The location of zero depends on the value of R_C. In order to achieve pole–zero cancellation [3], [5], it can be shown that when $R_C = (1+C_L/C_C)(1/g_{m2})$, P_2 is completely cancelled by Z_1. The GBW is independent of the pole–zero cancellation process and is described by the well-known equation as

$$\text{GBW}_{(\text{RCMC})} = \frac{g_{m1}}{C_C}. \tag{6}$$

For accurate pole–zero cancellation, the reciprocal of the series resistor R_C must track the transconductance g_m of the output transistor. This condition is not difficult to meet using the established tracking techniques [3], [5], [13]. As a result, the amplifier is simple, robust, and insensitive to the variations in process, temperature, and supply. However, there are several shortcomings when the amplifier drives large capacitive loads. They are, however, dependent on design approaches. The first approach is of fixing power consumption, the compensation resistor is increased but it will lower the pole P_3 and create the potential complex poles on the basis of collision of poles during the pole-splitting process. Hence, the amplifier would exhibit undesirable peaking effect that degrades the gain margin in frequency response. For the second approach, the transconductance of second gain stage in the amplifier is boosted *via* high biasing current combined with large driving device but at a cost of larger die size and power consumption. The third approach is to sacrifice the gain bandwidth through increasing the compensation capacitor value.

III. Multipath Miller Zero Cancellation Compensaton (MMZCC)

The well-known mutipath Miller zero cancellation compensation technique [6] (MMZCC) had been introduced to counteract the RHP zero by a parallel path that compensates for the direct feed-through effect. The technique improves the bandwidth by removing RHP zero that arises in a Miller-compensated amplifier. Further to MMZCC, other compensation techniques like multipath nested Miller compensation (MNMC) [7] and hybrid nested Miller compensation (HNMC) [8] are reported to extend the gain bandwidth of the amplifier. On the other hand, Nested G_m-C Compensation (NGCC) [9] is also proposed to reduce the zeros, simplifying the transfer function of the nested-Miller amplifier. All these techniques using pole–zero cancellation are effective. The topologies are popular in terms of small area, bandwidth efficiency, and low power at driving small or moderate capacitive loads.

A. MMZCC

MMZCC is an effective method [6] to eliminate the RHP zero. The major advantage is that the positions of the poles are not affected by the additional circuitry. The traditional techniques, such as voltage buffer, current buffer, or nulling resistor for RHP zero removal, intend to obstruct the direct feedforward path through the Miller capacitor. MMZCC, on the other hand, counteracts the RHP zero by a parallel path that compensates for the direct feed-through effect. The transfer function of the MMZCC structure in Fig. 2 is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{-g_{m1}g_{m2}R_1R_2\left[1+s\frac{(g_{mf}-g_{m1})C_C}{g_{m1}g_{m2}}\right]}{(1+sg_{m2}R_2R_1C_C)\left(1+s\frac{C_L}{g_{m2}}\right)} \tag{7}$$

where the symbols have their usual meanings. With reference to (7), there are two LHP poles and one zero as follows:

$$P_1 \approx \frac{-1}{g_{m2}R_2R_1C_C} \tag{8}$$

$$P_2 \approx \frac{-g_{m2}}{C_L} \tag{9}$$

$$Z_1 \approx \frac{-g_{m1}g_{m2}}{(g_{mf}-g_{m1})C_C}. \tag{10}$$

From (10), it should be observed that the zero Z_1 can be moved by controlling g_{mf} and g_{m1}. If $g_{mf} > g_{m1}$, Z_1 will be located at the LHP. If $g_{mf} = g_{m1}$, the zero is shifted to infinity. For implementing pole–zero cancellation (Z_1 on top of P_2) in the scheme of MMZCC, the value of g_{mf} to be obtained is

$$g_{mf} = \left(1+\frac{C_L}{C_C}\right)g_{m1}. \tag{11}$$

This leads to one dominant pole LHP P_1 in the transfer function of (7). From (11), it can be revealed that MMZCC is very

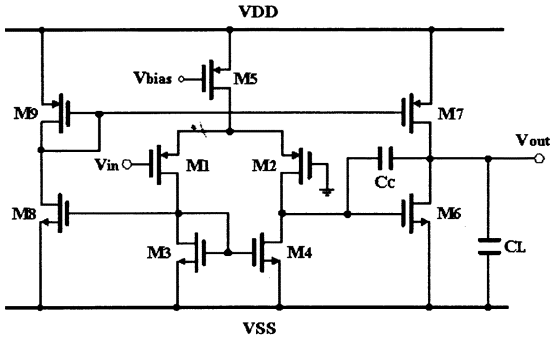

Fig. 3. A CMOS current push–pull operational amplifier with feedforward path.

power effective at small or medium load capacitance C_L, but not at large-load capacitance or small compensation capacitance. It is because device transconductnace is proportional to the square root of the aspect ratio W/L and biasing current I_D. As a consequence, this would contribute larger chip area and huge power consumption for high g_{mf} requirement.

From the dc gain as derived from (7) and the first pole frequency P_1 denoted by (8), the GBW is obtained as

$$\text{GBW}_{(\text{MMZCC})} = \frac{g_{m1}}{C_C}. \tag{12}$$

Although the $\text{GBW}_{(\text{MMZCC})}$ is identical to that of (6) for a two-stage operational amplifier, the g_{m1} can be made higher at identical C_C or alternately, smaller C_C at identical g_{m1} for bandwidth extension under the pole–zero cancellation scheme. The maximum bandwidth will be limited by the allowable phase lag introduced by the nondominant poles. The location of these nondominant poles depends on the number, biasing currents, aspect ratios of active devices, parasitic capacitances, and the circuit techniques in the multistage topologies.

B. MMZCC Using Current Push–Pull Technique

A simple modification of the two-stage operational amplifier improves driving capability to a capacitive load without increasing power dissipation in the second stage [3] significantly. Fig. 3 shows the CMOS operational amplifier having ability to source and sink current at the output under dynamic conditions. The signal at the drain of M_3 is applied to a common-source stage, M_8, resulting in current through M_9 being mirrored in M_7 such that sourcing current to the output load is improved. On the other hand, M_6 provides the sinking current ability from the output load. Hence, a push–pull operational amplifier structure is established in very simple manner.

A small-signal equivalent model of Fig. 3 is shown in Fig. 4. Assuming $A_i = i_7/i_1$ is defined as the current gain in the path formed by current mirrors M_9-M_7, M_3-M_8, the current of M_7 is a function of V_{in}. The transfer function $V_{\text{out}}/V_{\text{in}}$ can be written as

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{-g_{m1}g_{m6}R_1R_2\left[1+s\frac{(0.5A_i-1)C_C}{g_{m6}}\right]}{(1+sg_{m6}R_2R_1C_C)\left(1+s\frac{C_L}{g_{m6}}\right)} \tag{13}$$

where the symbols have their usual meanings. The transfer function is somewhat similar to the pole zero format in (7). From (13), there are two LHP poles and one zero. They are given as follows:

$$P_1 \approx \frac{-1}{g_{m6}R_1R_2C_C} \tag{14}$$

$$P_2 \approx \frac{-g_{m6}}{C_L} \tag{15}$$

$$Z_1 \approx \frac{-g_{m6}}{(0.5A_i-1)C_C}. \tag{16}$$

The dc gain and poles are unaffected by the additional current path, but the zero becomes a function of the current gain *via* current mirrors M_9-M_7, M_3-M_8. When $A_i = 2$, the zero appears at infinity. As A_i increases, the zero moves toward the origin. To ensure that the zero stays in the LHP, $A_i > 2$ is needed [3]. It is also possible for the LHP zero Z_1 to be located on the top of P_2 for pole–zero cancellation. To accomplish this task, the following conditions must be satisfied:

$$\frac{g_{m6}}{(0.5A_i-1)C_C} = \frac{g_{m6}}{C_L}. \tag{17}$$

The value of A_i becomes

$$A_i = 2\left(1+\frac{C_L}{C_C}\right) \tag{18}$$

and the overall feedforward transconductance from Fig. 4 is

$$g_{mf} = \frac{g_{m1}A_i}{2}. \tag{19}$$

Combining the results from (18) and (19), the dependence terms are the same as those of (11) and, hence, is not repeated here. The circuit implementation is simple, but in practice it is useful for small or moderate capacitive loads because of the introduction of potential delay by three stages: differential-pair-based voltage-to-current converter M_1-M_2, and two cascaded current mirror pairs, M_3-M_8, and M_9-M_7. The total delay would have the possibility to jeopardize the feedforward zero compensation either at high capacitive loads or low-power biasing currents. It can be relaxed by widening the feedforward loop bandwidth *via* increasing the power in the current mirror pairs but it might not be the appropriate design issue for low-power implementation.

IV. Gain-Enhanced Feed-Forward Path Compensation (GFPC)

In this section, the GFPC structure is described and analyzed. This includes transfer function and other important performance parameters such as gain-bandwidth product and phase margin.

A. Topology of GFPC Amplifier

A generic amplifier structure using GFPC technique is depicted in Fig. 5. Contrasting to the feedforward topology in Fig. 2, a wide-band gain-enhanced voltage amplifier, with low-

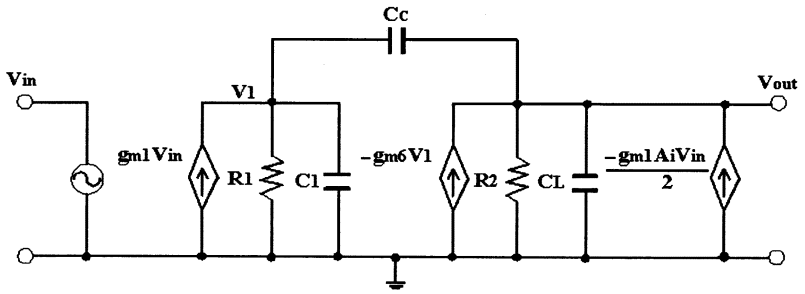

Fig. 4. Small-signal model of Fig. 3.

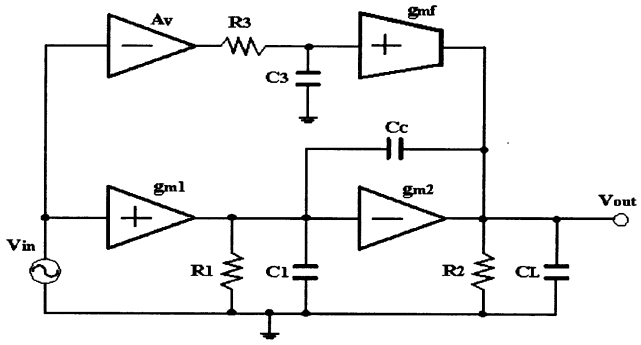

Fig. 5. Topology of the GFPC amplifier.

output impedance, is added in the feedforward path. Hence, the overall feedforward transconductance is given as $g_{mf(\text{overall})} = A_V g_{mf}$. The enhancement factor is A_V times for the transconductor stage.

B. Transfer Function

The equivalent small-signal model of the GFPC amplifier is shown in Fig. 6. Using small-signal analysis, the transfer function is obtained as

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{-g_{m1}g_{m2}R_1R_2\left[1+s\frac{(A_V g_{mf}-g_{m1})C_C}{g_{m1}g_{m2}}\right]\left[1-s\frac{g_{m1}C_3}{(A_V g_{mf}-g_{m1})g_3}\right]}{(1+sg_{m2}R_1R_2C_C)\left(1+s\frac{C_L}{g_{m2}}\right)(1+sR_3C_3)} \tag{20}$$

where the symbols have their usual meanings in (20). The pole frequencies are obtained as follows:

$$P_1 \approx \frac{-1}{g_{m2}R_1R_2C_C} \tag{21}$$

$$P_2 \approx \frac{-g_{m2}}{C_L} \tag{22}$$

$$P_3 \approx \frac{-1}{R_3C_3}. \tag{23}$$

It is also noted that from (20), one LHP zero and one RHP zero are generated and their frequencies are obtained as

$$Z_1 \approx \frac{-g_{m1}g_{m2}}{(A_V g_{mf}-g_{m1})C_C} \tag{24}$$

$$Z_2 \approx \frac{(A_V g_{mf}-g_{m1})g_3}{g_{m1}C_3}. \tag{25}$$

Comparing (24) in the GFPC scheme with (10) in the RCMC scheme, the location of GFPC zero Z_1 is approximately reduced by A_V times if $A_V g_{mf} > g_{m1}$ in (24) and $g_{mf} > g_{m1}$ in (10). This benefits the pole–zero cancellation at very low frequency. For $Z_1 = P_2$, we have

$$g_{mf(\text{overall})} = A_V g_{mf} = \left(1+\frac{C_L}{C_C}\right)g_{m1}. \tag{26}$$

It is important to note that the second pole P_2 of GFPC, defined by (22), is possible situated below the unity-gain bandwidth at heavy capacitive load but it does not affect the overall stability of the amplifier as far as pole–zero compensation process is valid. Substituting (26) into (25), Z_2 can be written as

$$Z_2 = \frac{C_L}{C_C}.\frac{1}{R_3C_3} = \frac{-C_L}{C_C}.P_3 \tag{27}$$

Z_2 is located on RHP at very high frequency, usually ranging from several hundred megahertz to 1-GHz above, the phase lag is insignificant and of little concern.

In summary, the improved frequency compensation scheme is addressed in several key comments: 1) the transconductance g_{mf} in Fig. 5 can be reduced by $1/A_V$ times when compared with that in Fig. 2 at driving identical capacitive load condition; 2) the overall $g_{mf(\text{overall})}$ boosted by the voltage gain amplifier reduces significant power consumption of the entire amplifier since the LHP zero Z_1 can compensate the LHP pole P_2 at low frequency; 3) the result of small compensation capacitor leads to smaller silicon area; and 4) the major nondominant parasitic LHP pole P_3 becomes the new second pole that defines the phase margin of the operational amplifier; and note that this parasitic pole, arised from the gain-enhanced voltage amplifier, is independent of the transconductance g_{m2} in the second gain stage.

C. Gain-Bandwidth (GBW) Product and Phase Margin (PM)

The GBW product and the phase margin of the GFPC amplifier are given by

$$\text{GBW}_{(\text{GFPC})} = \frac{g_{m1}}{C_C} \tag{28}$$

$$\text{PM}_{(\text{GFPC})} \cong 180^\circ - \tan^{-1}\left(\frac{\text{GBW}}{P_1}\right) - \tan^{-1}\left(\frac{\text{GBW}}{P_3}\right). \tag{29}$$

Refer to (29), the contribution of phase lag by the second pole P_2 is eliminated whereas the pole P_3 becomes the new second pole, which is usually situated at very high frequency. The $\text{GBW}_{(\text{GFPC})}$ can be made high at large capacitive loads

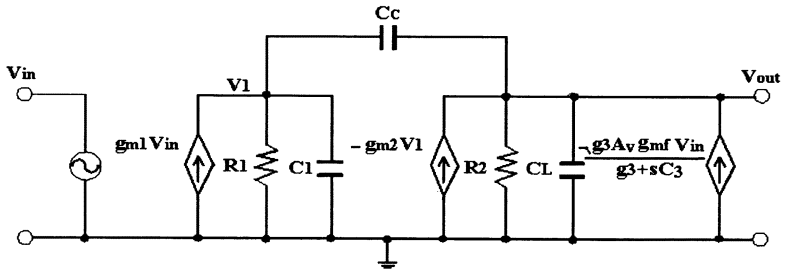

Fig. 6. Equivalent small-signal model of the GFPC amplifier.

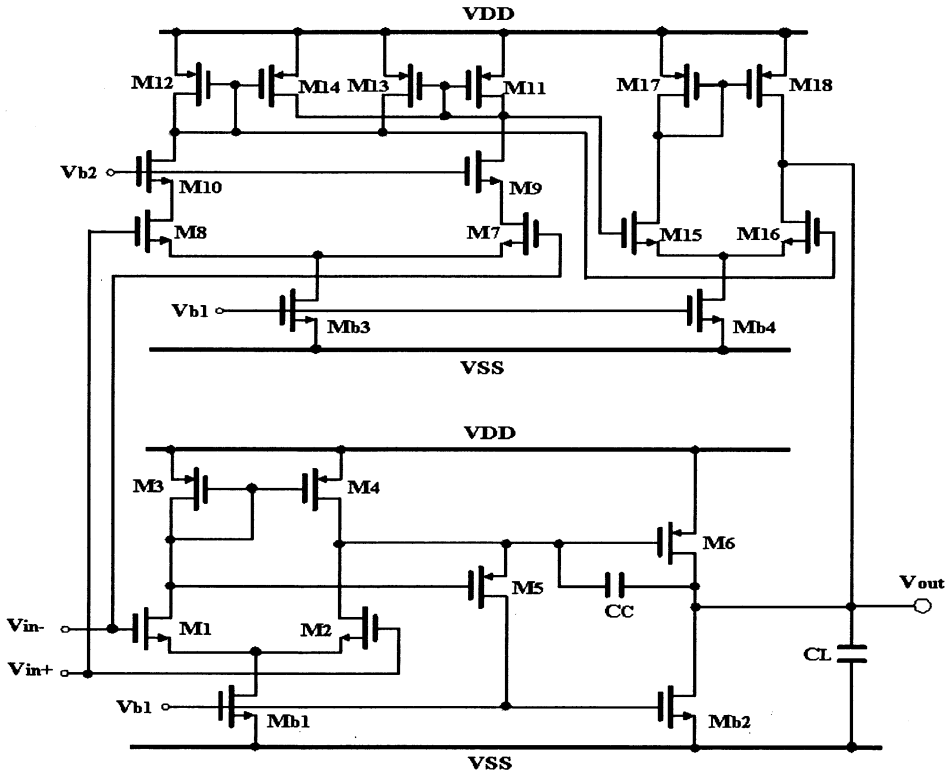

Fig. 7. Schematic of the GFPC operational amplifier.

because the GFPC amplifier is very stable even at small compensation capacitor value.

Assuming that the RHP zero Z_2 is situated at very high frequency, the phase margin of GFPC amplifier is about 60° when P_3 is located at 1.73 times unity-gain frequency. Further advantage is that P_3 can be separately optimized to yield maximum bandwidth in the GFPC amplifier, whereas P_3 in the RCMC amplifier is a function of R_C, which controls 1) the pole–zero cancellation according to (5) and 2) the position of P_3 according to (4). Hence, the low-frequency pole–zero compensation at heavy capacitive load leads to the design tradeoff issues between stability and bandwidth in the RCMC structure, but it is relatively easier to control the phase margin and bandwidth in the GFPC amplifier.

V. Implementation of GFPC Amplifier

A. Circuit Description

Fig. 7 shows the schematic of the operational amplifier using the proposed compensation technique. In the main path, transistors M_1-M_4, and M_{b1} form the first gain stage. This is the most critical stage, which dictates the GBW, input common-mode range, internal slew rate (SR), offset, and so forth. Transistors M_6 and M_{b2} form the second class-A gain stage. The standalone class-A output stage may not meet the external SR issue at heavy capacitive load because the constant current source transistor M_{b2} limits the SR and, on the other hand, is constrained by the static power consumption requirement. To relax these drawbacks, a SR enhancement transistor [11], which is applicable for class-A output topology in low-power design, is adopted. The major advantages of this technique are simple, and efficient, and only one transistor is needed, while without sacrificing the power consumption and area. In the implementation, a single transistor M_5 is added to improve the SR of the GFPC amplifier.

In the feedforward path, high feedforward transconductance is obtained economically in low power by cascading a gain-enhanced voltage amplifier with a transconductor in Fig. 7. The transconductor comprises transistors M_{15}-M_{18}, and M_{b4} while the voltage amplifier is comprised of a differential input pair

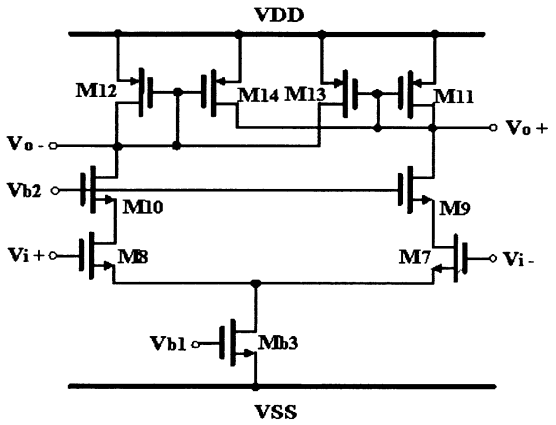

Fig. 8. Voltage gain stage with drain-coupled active load and cascode transistors.

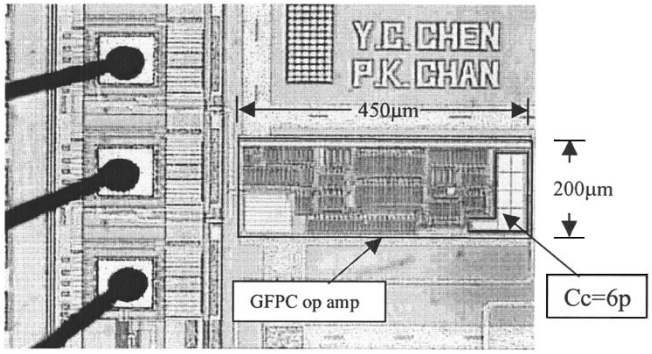

Fig. 9. Microphotograph of the GFPC operational amplifier.

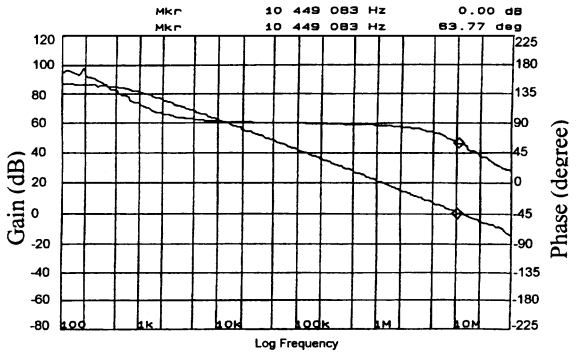

Fig. 10. Measured frequency response of the GFPC op amp while driving a 300-pF load.

M_7-M_8 with drain-coupled active loads M_{11}-M_{14} using negative impedance concept [12] for voltage gain enhancement. Finally, the transistor M_{b3} sets the biasing current for this stage.

In order to achieve bandwidth and area efficient GFPC amplifier, the voltage-gain stage as shown in Fig. 8 should have the attributes of low power, broad bandwidth, and high gain as well as small silicon overhead. Assuming matched process parameters in transistor pairs, M_7-M_8, M_9-M_{10}, M_{11}-M_{12}, and M_{13}-M_{14}, the differential voltage gain can be derived as

$$A_V \approx \frac{g_{m8}}{\frac{g_{ds8}}{g_{m10}r_{ds10}} + g_{ds12} + g_{ds13} + g_{m12} - g_{m13}}. \quad (30)$$

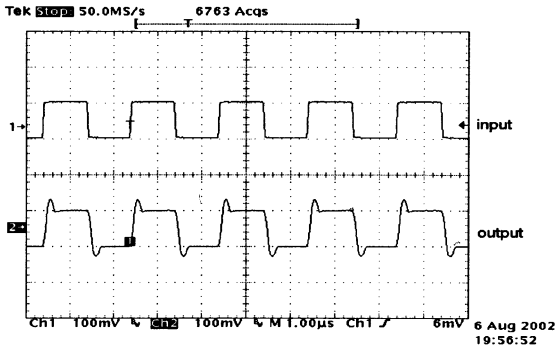

Fig. 11. Measured small-signal transient response of the GFPC op amp in unity-gain configuration while driving a 300-pF load.

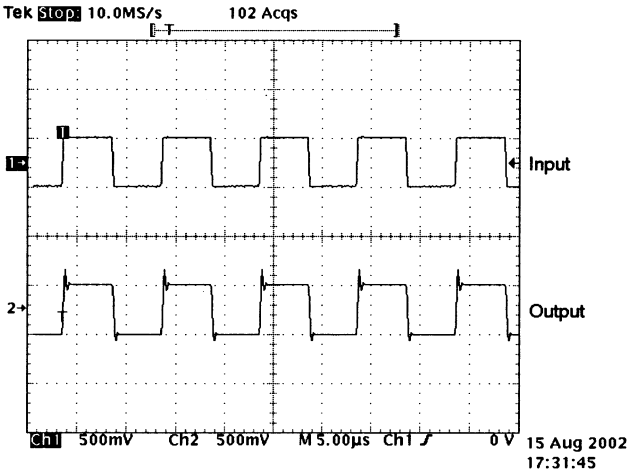

Fig. 12. Measured large-signal transient response of the GFPC op amp in unity-gain configuration while driving a 300 pF load.

TABLE I
MEASUREMENT RESULTS OF THE GFPC AMPLIFIER

Technology	CMOS 0.6 μm n-well
Gain Bandwidth (GBW)	10.4 MHz
DC Gain	87 dB
Phase Margin (PM)	63.7 °
$PSRR^+$ @ 1kHz	88 dB
$PSRR^+$ @ 10kHz	77 dB
$PSRR^-$ @ 1kHz	85 dB
$PSRR^-$ @ 10kHz	73 dB
Positive Slew Rate	3.9 V/μs
Negative Slew Rate	3.1 V/μs
Small signal 1% settling time +	272 ns
Small signal 1% settling time -	320 ns
Large signal 1% settling time +	629 ns
Large signal 1% settling time -	544 ns
Power Dissipation	2.45 mW @ 3 V
Load	300 pF

It can be seen that the effect of the cascode transistors M_9-M_{10} reduces the $g_{ds8}/(g_{m10}.r_{ds10})$ term to insignificant level. Not only does it improve the precision, it reduces the Miller capacitance reflected to the input capacitance. Thus, the voltage-gain expression can be approximated as

$$A_V \approx \frac{g_{m8}}{g_{ds12} + g_{ds13} + (g_{m12} - g_{m13})} \quad (31)$$

TABLE II
PERFORMANCE COMPARISON OF OPERATIONAL AMPLIFIERS USING DIFFERENT COMPENSATION TECHNIQUES

	Gain (dB)	GBW (MHz)	PM (°)	SR (V/μs)	Power (mW@V_{dd})	C_L (pF)	$C_{C(sum)}$ (pF)	$\frac{C_L}{C_{C(sum)}}$	FOM_S $\left(\frac{MHz \cdot pF}{mW}\right)$	FOM_L $\left(\frac{V/\mu s \cdot pF}{mW}\right)$	Area (mm^2)	Technology
NMC [7]	100	60	40	20	76@8	100	-	-	79	26	1.8	3GHz f_t BJT
MNMC [7]	100	100	40	35	76@8	100	-	-	132	46	1.8	3GHz f_t BJT
HNMC [8]	120 120	2 0.2	65 64	5 0.2	0.45@1.5 0.023@1.5	10 10	-	-	44 89	111 89	0.05	0.8μm CMOS
MHNMC [8]	120 120	6 0.6	69 53	13 0.7	0.450@1.5 0.023@1.5	10 10	-	-	133 267	289 311	0.05	0.8μm CMOS
NGCC [9]	100	1	58	5	1.4@2	20	-	-	14	71	0.22	2μm CMOS
EFC [13]	102	47	76	69	6.9@3	40	-	-	272	400	-	0.6μm CMOS
DFCFC1 [14]	>100	2.6	43	1.32	0.420@2	100	21	4.76	649	314	0.11	0.8μm CMOS
DFCFC2 [15]	>100	2.6	48	1.04	0.676@2	100	34	2.94	384	154	0.18	0.8μm CMOS
GFPC This work	87	10.4	63.7	3.5	2.45@3.0	300	6	50	1273	429	0.09	0.6μm CMOS

where A_V is dependent upon the choice of the aspect ratio, biasing current and channel lengths in the cross-coupled transistors. For short channel devices being used in the cross-coupled active loads to achieve high-bandwidth objective, the two output conductance terms cannot be ignored despite of the dominant transconductance terms, g_{m12} and g_{m13}. It degrades slightly in tracking design methodology. The maximum tracking error is expected to be no more than $\pm 15\%$. This is still acceptable in practical applications. However, if the difference $(g_{m12} - g_{m13})$ is made much larger than the sum of the two conductance terms $(g_{ds12} + g_{ds13})$ in (31), the final voltage gain becomes

$$A_V \approx \frac{g_{m8}}{g_{m12} - g_{m13}}. \tag{32}$$

This would improve the tracking accuracy because of the ease in matching g_m terms. The tracking error ranges from few percentages to less than $\pm 10\%$ against variations in process, temperature and supply.

B. Silicon Area of the GFPC Amplifier

Usually, the compensation capacitors and the active area of the output stage for amplifiers that drive heavy capacitive loads dominate the silicon area. However, based on the merits that low-power output stage and small compensation capacitor are allowed in the proposed amplifier as shown in Fig. 9, the required dimension for the whole amplifier is reduced significantly. Although the silicon area contributed by the voltage gain enhancement stage occupies 18% of the total area of 0.09 mm^2, but the significant reduction of compensation capacitor improves the silicon overhead, and thus small area is also achieved in this GFPC scheme.

VI. RESULTS AND DISCUSSIONS

A. Measured Results

The measured frequency response in Fig. 10 demonstrates that the amplifier exhibits high-bandwidth efficiency. The high stability of the operational amplifier is also validated even under the ultimate high ratio in $C_L/C_C = 300\ \text{pF}/6\ \text{pF} = 50$ for 10.4-MHz GBW and 63.7° PM while consuming only 2.45 mW in a standard low-cost CMOS technology. It is also observed that there is no peaking effect in the frequency response. This gives a favorable characteristic.

The small-signal transient response in Fig. 11 shows that the amplifier has good settling characteristic of about an average 296 ns for a 100-mV step. The reasons are that the PM of the GFPC amplifier is above 60° and the pole–zero doublet spacing is also compressed well *via* the tracking design. As a consequence, the output voltage can settle within a reasonably short time. The only limitation to settling time is due to the external-limited SR effect. For the large-signal transient response of a 0.5-V step in Fig. 12, the total settling time is at the average of 586 ns and the average SR is 3.5 $\text{V}/\mu\text{s}$. These performance parameters are still acceptable for a high capacitive load of 300 pF. Improving the slew-rate enhancement circuit is possible to further reduce the large-signal slew time.

In view of the second pole being positioned below the GBW for the pole–zero cancellation process in the GFPC scheme, the power to the output transistors can be made small and so does the sizing that leads to small capacitive parasitic in the respective output driving device and biasing device. In addition, lower-compensation capacitor is also achieved in the scheme. The measured performance of the power-supply rejection is acceptable good, which is 77 dB of PSRR+ and 73 dB of PSRR- at 10 kHz in such a noncascode-based amplifier. These implications are translated to small integrated circuit area, depicting the complete operational amplifier, occupying 0.09 mm^2 in the microphotograph of Fig. 9. This confirms the area efficiency of the GFPC method despite of the small area overhead from the gain-enhanced voltage amplifier. Experimental results are summarized in Table I. The measured results were obtained using a HP3589A network analyzer and Tektronix TDS754D.

B. Performance Comparisons

Table II summarizes the performance of the operational amplifiers using other topologies. In order to compare the relative performance of the frequency compensation techniques, two well-known figure of merits, FOM_S and FOM_L, are used to define respective small-signal and large-signal performances in normalized formats as follows:

$$\text{FOM}_S = \frac{\text{GBW} \cdot C_L}{\text{power}} \tag{33}$$

$$\text{FOM}_L = \frac{SR \cdot C_L}{\text{power}}. \tag{34}$$

The units of FOM_S and FOM_L are $\text{MHz}\cdot\text{pF}/\text{mW}$ and $\text{V}/\mu\text{s}\cdot\text{pF}/\text{mW}$, respectively. An average SR is used. These form the benchmark for the comparison with the results from this work. A larger figure of merits implies a better frequency compensation topology. It should also be noted the figure of merits are also linkage to the phase margin of the amplifier. The 60° PM is an appropriate value although some works are deviated due to application issues.

It can be seen from Table II that the measured performance of the GFPC amplifier is comparable with those of reported amplifier structures with different compensation methodologies in terms of power efficiency, bandwidth efficiency, and area efficiency. The experimental results have confirmed that the GFPC amplifier can achieve the stated objectives.

If a lower PM is allowed in the applications for a capacitive load of 1000 pF, further simulation results have shown that, with slight modification of design parameters, the GFPC amplifier can achieve the GBW of 6.44 MHz at PM of 52 °, an average SR of 1.7 $\text{V}/\mu\text{s}$, a compensation capacitance of 8 pF, $\text{FOM}_S = 2800$ and $\text{FOM}_L = 739$ at power consumption of 2.3 mW. This is also comparable with the state-of-the-art work [14]–[15] achieved in view of bandwidth, size of compensation capacitor, SR, and settling times. More importantly, the GBW is broadened at the conditions of similar level of PM, figures of merits, and capacitive load except with slightly lower dc gain on the basis of a two-stage topology.

VII. Conclusion

A CMOS operational amplifier with GFPC technique has been presented. The use of the composite gain-enhanced feedforward stage for intentional low-frequency pole–zero cancellation makes a significant improvement for the ability of the amplifier to drive heavy capacitive loads, while achieving high-gain bandwidth, high-load capacitance to compensation capacitance ratio, and very small silicon area under low-power constraint. This leads to large values on figure of merits, FOM_S and FOM_L, when compared with the reported works achieved so far. Besides, the measurement results have shown that the amplifier displays good stability, with absence of peaking effect. This improved frequency compensation technique will be found useful for amplifier design in analog signal processing applications.

References

[1] P. R. Gray and R. G. Meyer, "MOS operational amplifier design-a tutorial overview," *IEEE J. Solid-State Circuits*, vol. SSC-17, pp. 969–982, Dec. 1982.

[2] R. Grergorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

[3] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. London, U.K.: Oxford Univ. Press, 1987.

[4] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Norwell, MA: Kluwer, 1995.

[5] W. C. Black, D. J. Allstot, and R. A. Reed, "A high performance low power CMOS channel filter," *IEEE J. Solid -State Circuits*, vol. SSC-15, pp. 921–929, Dec. 1980.

[6] R. G. H. Eschauzier and J. H. Huijsing, "An operational amplifier with multipath miller zero cancellation for RHP zero removal," in *Proc. ESSCIRC 1993*, Editions Frontieres, Gif-sur-Yvettes, France.

[7] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1709–1717, Dec. 1992.

[8] R. G. H. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested miller compensation for 120 dB gain and 6 MHz UGF," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1497–1504, Dec. 1994.

[9] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested $G_m - C$ compensation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2000–2011, Dec. 1997.

[10] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-18, pp. 629–633, Dec. 1983.

[11] V. R. Saari, "Lower-Power high-drive CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-18, pp. 121–127, Feb. 1983.

[12] D. J. Allstot, "A precision variable-supply CMOS comparator," *IEEE J. Solid-State Circuits*, vol. SSC-17, pp. 1080–1087, Dec. 1982.

[13] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 339–347, Mar. 1999.

[14] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 221–230, Feb. 2000.

[15] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst.*, vol. 48, pp. 1041–1056, Sept. 2001.

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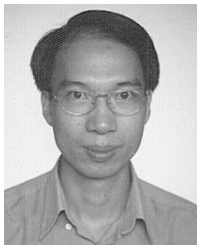

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