Design Methodology and Advances in Nested-Miller Compensation

Gaetano Palumbo, *Senior Member, IEEE*, and Salvatore Pennisi, *Member, IEEE*

***Abstract*—The nested Miller compensation of three-stage amplifiers is reviewed by using a simple design-oriented approach. The method provides stable amplifiers by accurately controlling the overall phase margin as well as that of the internal loop. Furthermore, the use of nulling resistors to remove the RHP zeros is discussed and optimization criteria are described. A novel technique is presented which allows an amplifier's frequency and settling performance to be greatly improved without increasing power consumption. Thanks to the small compensation capacitors employed, the approach is amenable for integration and in particular where large load capacitors have to be driven. SPICE simulations based on a 0.8-μm CMOS design are given and found in remarkable agreement with the theoretical analysis.**

***Index Terms*—Amplifiers, analog integrated circuits, circuit stability, CMOS analog integrated circuits, CMOSFET power amplifiers, compensation, feedback amplifiers, feedback circuits, frequency compensation, multistage amplifier, zero compensation.**

I. Introduction

DUE TO THE decrease in supply voltages, cascode topologies are not suitable for IC applications demanding both high gain and swing, such as high-accuracy and high-linearity circuits, and high-Q (switched-capacitor) filters. Presently, amplifiers exhibiting dc gains in excess of 100 dB can profitably be implemented with a cascade of three simple stages. Therefore, multistage amplifiers and their frequency compensation have become increasingly important in modern microelectronics [1]–[4].

In the design of two-stage amplifiers, it is common practice to employ the *Miller* compensation technique since it allows the use of a relatively low-valued compensation capacitor (which is amplified by the Miller effect) and increases the achievable bandwidth thanks to the well-known *pole-splitting* feature. It is also known that the stability of Miller-compensated amplifiers is deteriorated by a right-half-plane (RHP) zero which must be eliminated in CMOS amplifiers especially in low-power applications, due to the low transconductance of MOS transistors.

Miller compensation can also be applied to multistage amplifiers [5]–[12], and in this context three main possible arrangements have been recognized [4]. The *nested Miller* (NM) compensation is one of these, and can be profitably used when only the final gain stage is voltage-inverting. Several of the NM-compensated amplifiers considered in the literature are implemented in bipolar technology or have high-drive capability and are not designed for low-power CMOS applications [2], [10]. Here, the main effort of researchers has been to improve the by nature poor frequency performance of NM-compensated amplifiers. For instance, in [2] a technique which allows the maximization of the gain-bandwidth product is described.

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The authors are with the Dipartimento Elettrico, Elettronico e Sistemistico, Universita' Di Catania, (DEES), Catania I-95125, Italy.

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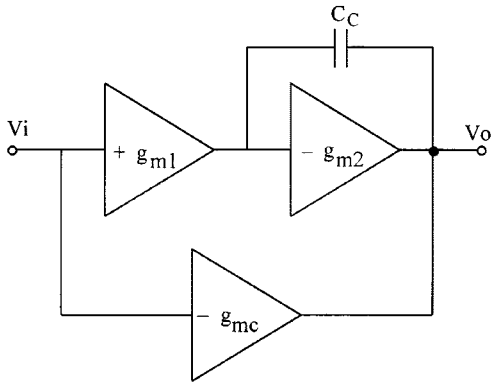

Fig. 1. Basic module for *multipath* NM zero cancellation.

Although the effects of parasitic zeros introduced by the NM compensation network were not taken into account in the early literature, for low-voltage low-power CMOS designs the removal of the right-half-plane (RHP) zero is mandatory and different strategies have been developed. One such design uses a transconductance-capacitance compensation scheme based on the nesting of a basic module (shown in Fig. 1) [4], [19]. The last work describes a systematic (*multipath*) compensation technique for a generic N-stage amplifier. However, the approach requires a computer-aided procedure to find transconductance values for each amplifier stage (this is a first limitation since transconductances are generally set by other specifications). Moreover, the particular choice of the capacitor values limits the maximum achievable bandwidth and the use of the feedforward transconductance has detrimental effects on the *CMRR*, as it creates an asymmetrical input-output path increasing the common-mode gain by approximately one gain stage.

Recently, another approach for RHP zero removal was reported [14]. It employs an auxiliary inverting stage which is used to increase (with the Miller effect) the internal compensation capacitor. This auxiliary stage is not loaded by the external load capacitor C_L, but only by parasitic capacitances. In such a manner small compensation capacitors can be used allowing increased bandwidth and slew-rate at the expense of a limited increase in circuit complexity and power dissipation. However, the proposed implementation [20, Fig. 6] has the damping-factor-control-stage which operates in open-loop conditions, thus, its bias point stability is endangered.

Except for the approach described in [15], in all existing works, the use of nulling resistors to provide RHP zero can-

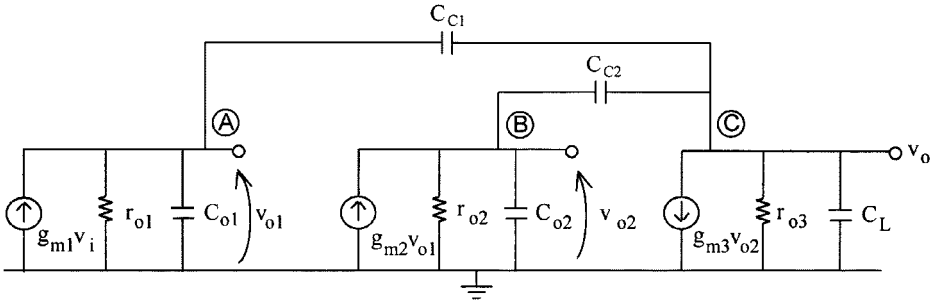

Fig. 2. Small-signal model of a three-stage NM-compensated amplifier.

cellation have been *a priori* excluded. It is our conviction that this method remains one of the best suited because of its inherent circuit-level simplicity, low-voltage low-power requirements, and the possibility of converting a RHP zero into a left-half-plane (LHP) one.

The purpose of this paper is twofold.

- The NM compensation is reviewed.
- An efficient approach based on nulling resistors is presented.

Section II presents a new, simple design-oriented method which, by neglecting the effects of parasitic zeros, provides results in agreement with those reported in previously published works. As customary in amplifier design, we use the phase margin (ϕ) as the main design parameter which, in conjunction with the gain-bandwidth product (*GBW*), is the most meaningful and can simply be set by a pencil-and-paper computation. Techniques for the removal of RHP zeros using nulling resistors are also dealt with in Section III, and an optimization of the method suggested in [15] is given. In these above two sections an assessment and optimization of previously presented works is hence attempted. Regarding the second point, a compensation approach which exploits double pole–zero cancellation is presented in Section IV. Finally, SPICE simulations on a three-stage amplifier example implemented in a 0.8-μm CMOS technology and powered with a 2-V supply are provided in Section V.

II. NM Compensation

In this section, the NM compensation technique is reviewed by use of a novel design-oriented approach. Let us consider the small-signal equivalent circuit of a three-stage amplifier depicted in Fig. 2 including the compensation capacitors. Parameters $g_{\rm mi}$ and $r_{\rm oi}$ are the i-th stage transconductance and output resistance, respectively. Capacitors $C_{\rm oi}$ represent the equivalent capacitance at the output of each stage, while C_L is the equivalent load capacitor. In the proposed analysis, we neglect the effects of the parasitic capacitances $C_{\rm oi}$ since they are generally one order of magnitude lower than compensation capacitances.

Under these assumptions and neglecting second-order terms, the open-loop gain of the circuit in Fig. 2 is expressed by

$$A(s)=A_o\frac{1-\frac{C_{C2}}{g_{m3}}s-\frac{C_{C1}C_{C2}}{g_{m2}g_{m3}}s^2}{\left(1+\frac{s}{\omega_{p1}}\right)\left[1+\left(\frac{1}{g_{m2}}-\frac{1}{g_{m3}}\right)C_{C2}s+\frac{C_{C2}C_L}{g_{m2}g_{m3}}s^2\right]}. \quad (1)$$

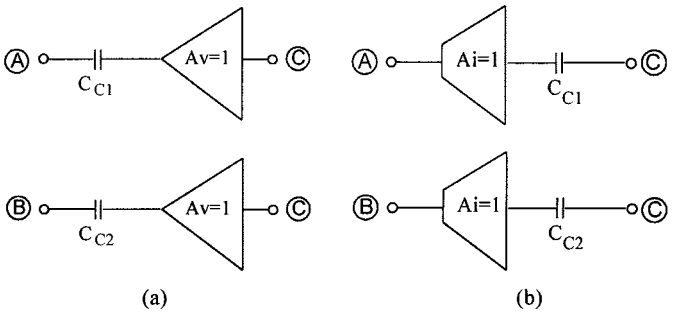

Fig. 3. Compensation network: (a) With voltage followers; (b) Current followers.

In (1) A_o is the dc open-loop gain equal to $g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}$ and ω_{p1} is the frequency of the dominant pole $\omega_{p1}\approx 1/\left(r_{o1}g_{m2}r_{o2}g_{m3}ro3C_{c1}\right)$, which gives the gain-bandwidth product, ω_{GBW}, of the amplifier

$$\omega_{\rm GBW}=A_o\omega_{p1}\approx\frac{g_{m1}}{C_{C1}}. \quad (2)$$

Equation (1) also includes two other (higher) poles and two zeros. Since the coefficients of the s and s^2 terms in the numerator are both negative, a RHP zero is created that is located at a lower frequency than the other LHP zero. Both zeros can be nominally eliminated by using voltage followers [16], [17] or current followers [18], [19] which break the feedforward path. These compensation networks are depicted in Fig. 3(a) and (b). As already mentioned, another solution is the multipath Miller approach [13]. Referring to Fig. 1, we have a zero cancellation if $g_{\rm mc}$ equals g_{m1} due to the effect described in [4].

When using any of these well-known techniques or in the case of a very high g_{m3}, such as in power amplifiers [9], [10], relationship (1) can be simplified into

$$A(s)=A_o\frac{1}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{C_{C2}}{g_{m2}}s+\frac{C_{C2}C_L}{g_{m2}g_{m3}}s^2\right)}. \quad (3)$$

Equation (4) allows a very clear interpretation of compensation behavior. For a dominant-pole frequency response (which means that ω_{GBW} equals the unity-gain frequency ω_T), the second and third stage can be considered as closed in unity-gain feedback configuration by capacitor C_{C1}, acting as a short circuit for frequencies above ω_T. Consider now the open-loop gain of the second and third stage alone (which we also refer to as the *inner* amplifier), $A_i(s)$, its dc gain, the dominant pole ω_{p1i} due

to Miller effect on C_{C2}, and the second pole ω_{p2i} at the output terminal. They are all given by

$$A_{oi} = g_{m2}g_{m3}r_{o2}r_{o3} \tag{4}$$

$$\omega_{p1i} \approx \frac{1}{r_{o2}g_{m3}r_{o3}C_{C1}} \tag{5}$$

$$\omega_{p2i} \approx \frac{g_{m3}}{C_L}. \tag{6}$$

If now we assume $A_i(s)$ in unity-gain feedback connection, the resulting closed-loop transfer function is characterized by exactly the same second-order polynomial as in the denominator of (3), as demonstrated in the Appendix I. This simple consideration allows, in turn, the straightforward compensation technique discussed below.

For a well designed (i.e., with appropriate stability margins) inner amplifier, the second pole ω_{p2i} must be located well beyond the unity-gain frequency ω_{Ti}, which, under the dominant-pole behavior assumption, is given by

$$\omega_{Ti} \approx \frac{g_{m2}}{C_{C2}}. \tag{7}$$

In order to avoid overshoot in the module of the inner amplifier frequency response, a proper ratio, K_i, between ω_{p2i} and ω_{Ti} has to be set. The trigonometric tangent of parameter K_i is the phase margin of the inner amplifier and a fairly optimum value is 2 (i.e., an inner phase margin of about 64°) which is the minimum value guaranteeing a monotonic behavior in the module of the frequency response. This leads to the expression of capacitor C_{C2},

$$C_{C2} = 2\frac{g_{m2}}{g_{m3}}C_L. \tag{8}$$

In other words, we have an external feedback loop through C_{C1} and an inner one through C_{C2}. The stability of the inner loop must be first established so that we can proceed to the external one. Any design attempt not providing a proper phase margin to the inner loop would inevitably require an extremely high value of C_{C1} or even not achieve stability at all.

Now we return to the frequency response of the whole open-loop amplifier, which can be rewritten as

$$A_o(s) = A_o \frac{1}{1+\frac{s}{\omega_{p1}}} \frac{1}{1+\frac{s}{\omega_{Ti}}+\frac{s^2}{2\omega_{Ti}^2}} \tag{9}$$

and evaluating the phase margin we get

$$\tan(\phi) = \tan\left(90° - \tan^{-1}\frac{\frac{\omega_T}{\omega_{Ti}}}{1-\frac{\omega_T^2}{2\omega_{Ti}^2}}\right) \approx \frac{1-\frac{1}{2}\left(\frac{\omega_T}{\omega_{Ti}}\right)^2}{\frac{\omega_T}{\omega_{Ti}}}. \tag{10}$$

Solving (10) for ω_T/ω_{Ti} and combining with (2) and (7) gives the expression of capacitance C_{C1} as a function of the required phase margin

$$C_{C1} = \left[\tan(\phi) + \sqrt{\tan^2(\phi)+2}\right]\chi C_L \tag{11}$$

where we have defined χ equal to g_{m1}/g_{m3}.

Equations (8) and (11), albeit very similar to those already reported in previously published works, are more general. For instance, in [4] a third-order Butterworth frequency response in unity-gain configuration is assumed, yielding the same expression of C_{C2} as in (8), while the expression of C_{C1} is $4\,(g_{m1}/g_{m3})\,C_L$, evaluated only for a phase margin of about 60°. To achieve a better phase margin, say of 70°, the term in the square brackets of (11) should be equal to 5.8 instead of 4. In general, NM compensation requires high-valued compensation capacitors. Specifically, for high g_{m1}/g_{m3} ratios, the value of C_{C1} is in the same range as that of the load capacitor and can even be higher. This, of course, limits the maximum achievable bandwidth.

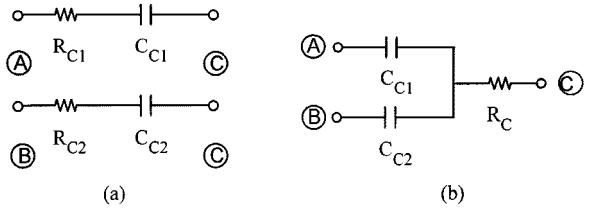

Fig. 4. Compensation networks with nulling resistors: (a) Conventional one; (b) With a single resistor.

III. The Use of Nulling Resistors to Eliminate RHP Zeros

A nulling resistor connected in series with the compensation can completely eliminate the RHP zero or even transform it into a LHP one [20], [21]. This approach has been avoided in the past for NM-compensated amplifiers because of its exacting requirements if used in a conventional fashion, as will now be explained.

Fig. 4(a) illustrates the conventional *RC* compensation network to be used in the three-stage amplifier of Fig. 2, which includes two nulling resistors R_{C1} and R_{C2}.

With the introduction of these two resistors the open-loop gain given in (1) we obtain (12) shown at the bottom of the next page. Observe that according to the Appendix I, only R_{C2} modifies the denominator because R_{C2} changes the zero of the inner amplifier. It is also clear that the numerator of (12) is greatly different from that of (1) and now depends on R_{C1} and R_{C2}. Now, it is possible to nullify the s^2 term and to make positive the s term by choosing

$$R_{C2} = \frac{1}{g_{m2}g_{m3}R_{C1}} + \frac{1}{g_{m3}}. \tag{13}$$

In this manner, the zero can be exploited to increase the phase margin. However, a complex matching between R_{C1} and R_{C2} is required. We shall not further develop this approach since, as described in the following, a better technique based on a single nulling resistor was developed [15]. It is illustrated in Fig. 4(b).

When applied to the amplifier in Fig. 2, the compensation network in Fig. 4(b) gives the loop-gain expression (14) shown at the bottom of the next page. In this case, the s^2 term in the numerator can simply be set equal to zero by choosing

$$R_C = \frac{1}{gm3} \tag{15}$$

and the loop-gain only has a negative zero which can be used to increase the phase margin.

It is worth noting that in this case, the s coefficient within square brackets in the denominator is independent of R_C. Therefore, (8) cannot be used, but the same procedure can still be adopted to achieve new simple equations for C_{C1} and C_{C2}, for a given value of the inner and overall phase margin. After having substituted (15) in (14) and assuming as usual $K_i = 2$ for the inner amplifier, we can set C_{C2} and evaluate the phase margin

$$C_{C2} = 2\frac{g_{m2}}{g_{m3} - g_{m2}} C_L \tag{16}$$

$$\tan(\phi) = \tan\left(90^\circ - \tan^{-1}\frac{\frac{\omega_T}{\omega_{Ti}}}{1 - \frac{\omega_T^2}{2\omega_{Ti}^2}} + \tan^{-1}\frac{\omega_T}{\omega_Z}\right) = \frac{2\omega_{Ti}\left(\frac{\omega_T}{\omega_{Ti}}\right)^2 + \omega_Z\left[2 - \left(\frac{\omega_T}{\omega_{Ti}}\right)^2\right]}{\frac{\omega_T}{\omega_{Ti}}\left\{\omega_{Ti}\left[\left(\frac{\omega_T}{\omega_{Ti}}\right)^2 - 2\right] + 2\omega_Z\right\}} \tag{17}$$

where ω_z is the frequency of the zero $1/R_C C_{C1}$ and ω_{Ti}, comparing (9) with (14) and using (16) is $g_{m3}/2C_L$. Solving (17) for ω_{Ti}/ω_T and combining with (2) and (15) gives the value of capacitance C_{C1} we obtain (18) shown at the bottom of the page where again we have put χ equal to g_{m1}/g_{m3}. By considering that χ is lower than $\tan(\phi)$ for the phase margin of interest (i.e., for $\phi \geq 60^\circ$), the above equation can be approximated well by

$$C_{C1} \approx \frac{\tan(\phi) + \sqrt{2 + \tan^2(\phi) + 2\chi\tan(\phi)}}{1 + \chi\tan(\phi)}\chi C_L \tag{19}$$

which is more suitable for pencil and paper design and is equal to (11) for $\chi \ll 1$. As expected, compared to (11), (19) gives lower values of C_{C1} for the same phase margin.

It is interesting to note that we assumed no constraint for transconductances except $g_{m3} > g_{m2}$, otherwise C_{C2} in (16) would be negative. This allows the power consumption to be optimized since low quiescent currents can be used and, perhaps more importantly, we are free to choose the input and output transconductances g_{m1} and g_{m3}. Unfortunately, like for classic NM compensation, this method still requires large compensation capacitors for heavy capacitive loads. For instance, if $g_{m3} = 4g_{m1}$ and for a target phase margin of 70°, the required compensation capacitor C_{C1} becomes equal to $0.9C_L$.

IV. Nulling-Resistor Technique With Double Pole–Zero Cancellation

To overcome the above drawback, an alternative compensation technique that can be profitably exploited in cases of heavy capacitive load is presented in this section.

A. Design Equations

The previous single-resistor compensation technique can be modified by adding another resistor R_{C2} in series with capacitor C_{C2}, as illustrated in Fig. 5. Although this change may appear of marginal significance, it turns out to be very attractive since it allows pole–zero compensation to be achieved at the same time, by using reduced values of compensation capacitors. This in turn leads to an improvement in terms of gain-bandwidth product, slew-rate, and settling time.

The transfer function of the amplifier in Fig. 2, using the compensation network in Fig. 5 becomes (20), shown at the bottom of the next page. It can be seen that the zeros can both be made negative and their values can be adjusted to exactly cancel the two higher poles. By again setting

$$R_C = \frac{1}{g_{m3}} \tag{21a}$$

and equating the coefficients of the second-order polynomials we get

$$C_{C1} = \frac{g_{m3} - g_{m2}}{g_{m2}} C_{C2} \tag{21b}$$

$$R_{C2} = \frac{1}{g_{m3}}\frac{C_L}{C_{C2}}. \tag{21c}$$

B. Discussion

Note that relations (21) are independent of g_{m1} and, ideally, the compensation capacitors are also independent of the load ca-

$$A(s) = A_o\frac{1 + \left[R_{C1}C_{C1} + \left(R_{C2} - \frac{1}{g_{m3}}\right)C_{C2}\right]s - \frac{1+(1-g_{m3}R_{C2})g_{m2}R_{C1}}{g_{m2}g_{m3}}C_{C1}C_{C2}s^2}{\left(1 + \frac{s}{\omega_{p1}}\right)\left[1 + \left(R_{C2} + \frac{1}{g_{m2}} - \frac{1}{g_{m3}}\right)C_{C2}s + \frac{C_{C2}C_L}{g_{m2}g_{m3}}s^2\right]} \tag{12}$$

$$A(s) = A_o\frac{1 + \left[R_C C_{C1} + \left(R_C - \frac{1}{g_{m3}}\right)C_{C2}\right]s + \frac{g_{m3}R_C - 1}{g_{m2}g_{m3}}C_{C1}C_{C2}s^2}{\left(1 + \frac{s}{\omega_{p1}}\right)\left[1 + \left(\frac{1}{g_{m2}} - \frac{1}{g_{m3}}\right)C_{C2}s + \frac{1 - g_{m2}R_C}{g_{m2}g_{m3}}C_{C2}C_L s^2\right]} \tag{14}$$

$$C_{C1} = \frac{\left[\sqrt{\chi^2\left(2\tan^2(\phi) + 1\right) + 2\chi\tan(\phi) + 2 + \tan^2(\phi)} + \tan(\phi) - \chi\right]}{1 + \chi\tan(\phi)}\chi C_L \tag{18}$$

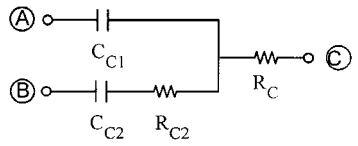

Fig. 5. Proposed two-resistor compensation network.

pacitor. This means that a suitable value of C_{C1} can be chosen to maximize the gain-bandwidth product, which can now reach the same order of magnitude as an optimized two-stage Miller-compensated OTA [20]. Again g_{m3} must be higher than g_{m2}, so that compensation elements will be positive. Moreover, these relations only require matching of capacitors and transconductances. By substituting (21) in (20) we find that the transfer function frequency response of the amplifier is now a single-pole function.

Observe that of all the possible solutions that reduce (20) to a single-pole function, the one chosen has also the property of providing an inherent pole–zero cancellation for the (open-loop) transfer function of the amplifier constituted by only the second and third stage. Indeed, denoting as ω_{P2}^* and ω_Z^* their second pole and (negative) zero, respectively, these are given by

$$\omega_{P2}^* = \frac{g_{m3}}{C_L} \tag{22}$$

$$\omega_Z^* = \frac{1}{\left(R_{C2} + R_C - \frac{1}{g_{m3}}\right) C_{C2}} \tag{23}$$

whose expressions perfectly match if (21) are used. However, the *inner* amplifier (as defined in Section II), which is closed in feedback loop by capacitor C_{C1}, is comprised between the input of the second stage and the common node of R_{C2} and R_C. Therefore, according to our design methodology, we have to primarily check the stability of this *inner* feedback loop. The open-loop transfer function of the inner amplifier is

$$A_i(s) = A_{io} \frac{1 + \left(R_{C2} - \frac{1}{g_{m3}}\right) C_{C2} s - \frac{R_C C_{C2} C_L}{g_{m3}} s^2}{1 + g_{m3} r_{o2} r_{o3} C_{C2} s + r_{o2} r_{o3} C_{C2} C_L s^2} \tag{24}$$

where $A_{io} = g_{m2} r_{o2} g_{m3} r_{o3}$. From (24) and using (21) we derive the expressions of the unity-gain frequency and that of the second pole and zeros of the inner amplifier

$$\omega_{Ti} = \frac{g_{m2}}{C_{C2}} \tag{25a}$$

$$\omega_{P2i} \approx \frac{g_{m3}}{C_L} \tag{25b}$$

$$\omega_{Z1i} \approx \frac{g_{m3}}{C_L - C_{C2}} \tag{25c}$$

$$\omega_{Z2i} \approx \left(\frac{C_L}{C_{C2}} - 1\right) \frac{g_{m3}}{C_L} \tag{25d}$$

showing that the second pole and the zero remain very close provided that $C_{C2} < C_L$. In this case, the second (RHP) zero tends to g_{m3}/C_{C2} and in order to ensure stability it must be higher than the unity-gain frequency given in (25a). Setting the inner phase margin greater than 64° yields $g_{m3} > 2g_{m2}$. The above relation establishes a lower limit for the ratio between g_{m3} and g_{m2}. Under this condition, any value of C_{C2} lower than C_L ideally ensures the stability of the inner amplifier. A minimum usable value for C_{C2} exists in reality. Compensation capacitors must be greater than parasitic capacitances at the high-impedance nodes to be valid for development. Besides, and usually more important, slew-rate considerations posit the fundamental limit for the minimum value of C_{C2}, as discussed below.

It is well known that when the amplifier's input is fed with a large voltage step, the amplifier is not operating as a negative feedback system and the output exhibits slewing behavior [22], [23]. This is usually caused by one of the differential input transistors that is completely turned off. Once the voltage difference between the two amplifier inputs is smaller than a certain amount, the input stage is able to restore negative feedback and the output voltage starts to settle. However, the closed-loop slewing time interval can be greatly increased, and overshoot can even occur if, in addition to the input pair, the (active) output transistor also turns off. In this case the input differential pair cannot restore feedback until the output transistor turns on. To prevent the deep cut-off of the output transistor, the internal *SR* (given by the ratio between the maximum current available from the second stage, I_{sat2}, termed the *saturation* current, and C_{C2}) must be set not greater than the external *SR* (given by the ratio between the saturation current of the output stage, I_{sat3}, and C_L). Hence we get

$$C_{C2} \geq \frac{I_{\text{sat2}}}{I_{\text{sat3}}} C_L. \tag{26}$$

Note that this effect is usually not seen using conventional compensation strategies, as they lead to high-valued compensation capacitors, which lie in the same range as the load capacitor. As a result of the above considerations, we see that the potential of the proposed compensation technique cannot be fully exploited if only a moderate saturation output current is available and/or a large capacitive load has to be driven, since large values of compensation capacitor C_{C2} must be used. This limitation is (substantially) overcome by adopting a class AB output stage with high drive capability. In this case C_{C2} needs only be greater than the parasitic capacitance to (20) remain valid. Note that the implementation of a class AB output stage can be very straightforward in a multistage NM-compensated amplifier where at least two high-impedance nodes with a phase shift of 180° are available to drive the

$$A(s) = A_o \frac{1 + \left[R_C C_{C1} + \left(R_{C2} + R_C - \frac{1}{g_{m3}}\right) C_{C2}\right] s + \frac{(1 + g_{m2} R_{C2}) g_{m3} R_C - 1}{g_{m2} g_{m3}} C_{C1} C_{C2} s^2}{\left(1 + \frac{s}{\omega_{p1}}\right) \left[1 + \left(R_{C2} + \frac{1}{g_{m2}} - \frac{1}{g_{m3}}\right) C_{C2} s + \frac{1 - g_{m2} R_C}{g_{m2} g_{m3}} C_{C2} C_L s^2\right]} \tag{20}$$

two output transistors. In contrast, this becomes a rather complex solution in a two-stage architecture especially when using low-voltage power supply [11], [12].

The above procedure is unable to provide an expression for the equivalent second pole, which now depends on parasitic capacitances. This does not constitute a problem in those cases where relatively large compensation capacitances are used, as the phase margin will be approximately 90°. However, to completely exploit the advantages of such a technique small compensation capacitors must be used to maximize bandwidth. In this case we are not able to anticipate the value of the phase margin, and computer simulations are mandatory to verify the design viability. It is worth noting that now the actual equivalent second pole derives from the high frequency behavior of real amplifier implementations not modeled in the circuit in Fig. 2. Indeed, the second pole can be estimated by considering the smallest ratio between the transconductances exhibited by the active-load circuitry (usually, current mirrors or common gate transistors) and their associated parasitic capacitances. Moreover, using the equality condition in (26) gives a dominant pole determining a phase margin which is usually greater than 80°, and often close to 90°.

A final remark concerns the effects of process and temperature variations. These do not allow a perfect pole–zero cancellation and two pole–zero doublets arise which could deteriorate the amplifier stability especially if the lower doublet appears on the left of the transition frequency. This issue is common to all the pole–zero canceling approaches. In [24], biasing schemes allowing pole–zero tracking are discussed for both cases in which a MOS in triode or an on-chip linear resistor are used to implement the compensation resistors. These techniques can also be adapted and profitably exploited for our compensation approach.

V. Simulation Results

The previously proposed compensation techniques were validated and compared through simulations with SPICE, using the model parameters of a 0.8-μm double-metal double-poly process. The simplified schematic of the three-stage amplifier used in the simulations is illustrated in Fig. 6. The circuit is made up of two (complementary) differential stages (M1-M5 and M6-M10) and a final common-source stage (M11-M12). Observe that the load transistor of the last stage, M11, can be either configured as a current source or its gate can be connected to the output of the first differential amplifier to provide a class AB output stage with improved slew-rate performance. Both these design options will be utilized and results compared. Note that although M11 does not significantly alter the output transconductance, it introduces a zero-compensation path which increases the phase margin, similarly to the technique described in [4].

The circuit uses a supply voltage of 2 V and dissipates 0.16 mW. Its transistor aspect ratios are reported in Table I. The bias currents in the first two stages is 20 μA, while the current in the output stage is 40 μA. The transconductances of the first, second and third stage are 3.8 10^{-4}, 3.1 10^{-4}, and 11.5 10^{-4} A/V, respectively. Note that g_{m1} and g_{m2} represent the transconductance of each transistor of the pairs M1-M2 and M6-M7, respectively, while g_{m3} is the transconductance of transistor M12. A moderate value of g_{m3} was intentionally chosen in order to show the effectiveness of the technique also with low output transconductances. In fact, the higher the value of g_{m3} the simpler the frequency compensation. The dc gain of the amplifier was 109 dB.

We considered two different load conditions, namely, C_L equal to 20 and 100 pF. For a target phase margin of 70°, and in conformity with the compensation procedure given in Section II, we found for the two cases the values of the compensation capacitors reported in the first and fourth rows of Table II.

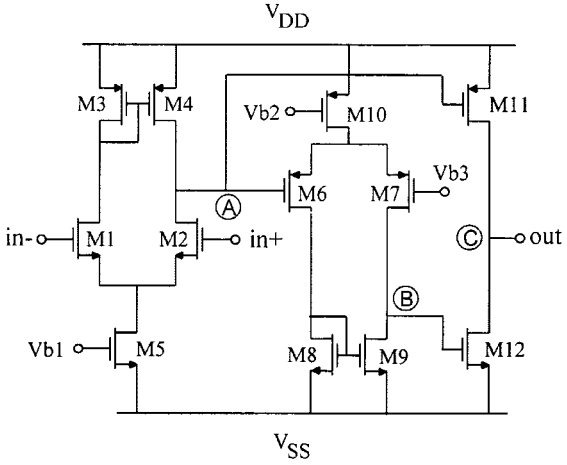

Fig. 6. Three-stage op-amp used for the simulations.

TABLE I
Transistor Aspect Ratios

Transistor	W/L
M1, M2	70/0.8
M3, M4	150/0.8
M5, M8, M9	40/0.8
M6, M7	140/0.8
M10	80/0.8
M11	600/0.8
M12	160/0.8

TABLE II
Component Values for Different Zero-Canceling Approaches

Zero cancellation technique	C_L (pF)	C_{C1} (pF)	C_{C2} (pF)	R_C (Ω)	R_{C2} (kΩ)
ideal voltage followers	20	38	12	–	–
as in reference [15]		20	15	870	–
proposed		8	3	870	5.8
ideal voltage followers	100	191.5	54	–	–
as in reference [15]		101	74	870	–
proposed		40.5	15	870	5.8

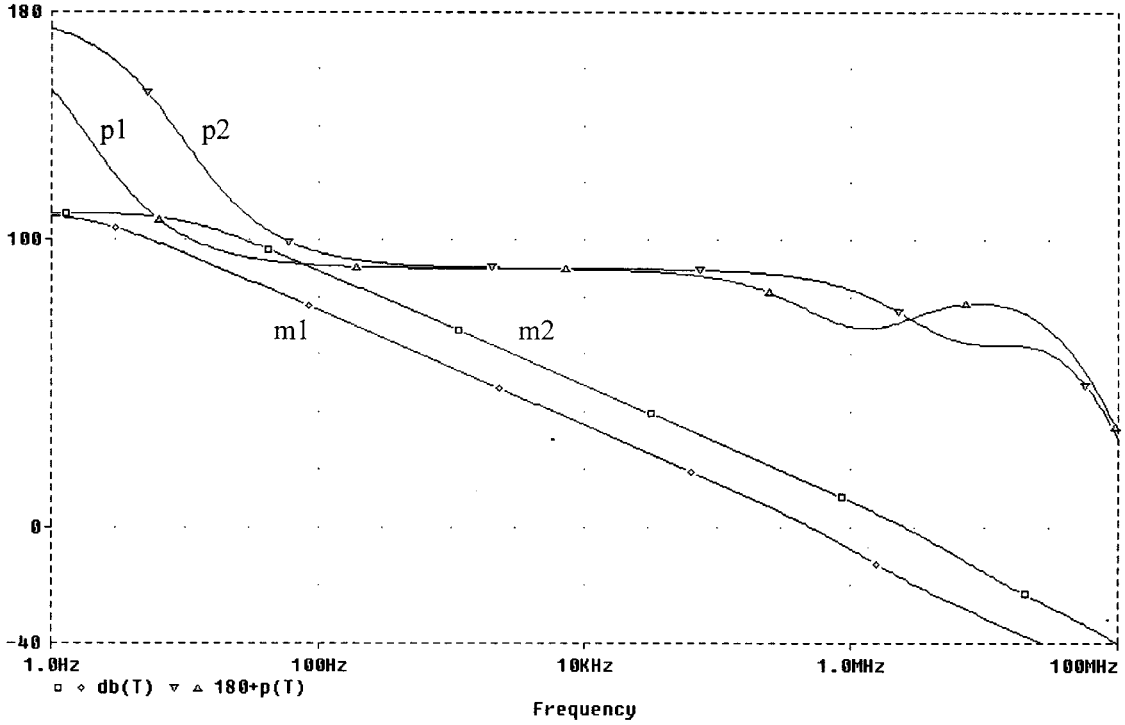

Fig. 7. Loop gain of the amplifier using the single nulling resistor compensation approach. Curves m1-p1 and m2-p2 refer to the case with $C_L = 100$ pF, and $C_L = 20$ pF, respectively.

Provided that the zeros are eliminated (for instance, with ideal voltage followers simulated using voltage-controlled voltage-sources) *GBW* and ϕ were 1.8 MHz, 70° and 370 kHz, 70.5°, respectively. No appreciable variations were observed when configuring M11 as a current source. Indeed, a less than 15% gain-bandwidth product error and a less than 1° phase margin error were always observed.

Of course, ideal voltage followers are only a simulation artifice to nominally eliminate the effect of zeros which would otherwise cause a poor phase margin or even instability. A more realistic method is to introduce one nulling resistor, as described in Section III. According to (15), (16) and (19), a phase margin of 70° requires the values of R_C, C_{C1} and C_{C2} in Table II (second and fifth rows). Note that the required value of C_{C1} is about one half lower than that required by the simple NM compensation (though the value of C_{C2} is now increased). Nevertheless, for the 100-pF load, the required value of C_{C1} is still too high for integration. The frequency response of the loop gain for the two cases is illustrated in Fig. 7 (module and phase, curves m1-m2 and p1-p2, respectively). The *GBW* and ϕ were 2.5 MHz, 73.4° and 505 kHz, 74.6°, respectively. The value of the phase margin is higher than what was anticipated because of the action of M11. By connecting M11 as a constant current source the phase margin was respectively 66.4° and 67° for the two cases, yielding an error lower than 4°. Fig. 8 shows the time responses of the amplifier in unity-gain configuration to an input step of $0.5V_{\rm pp}$. The 0.1% settling time for the 20-pF and the 100-pF load case is $T_S^{+/-} = 513/615$ ns and $T_S^{+/-} = 2.98/3.06$ μs, respectively.

Finally, the novel compensation technique with double pole–zero cancellation described in Section IV was considered. For the 20-pF-load and 100-pF-load case we chose C_{C2} equal to 3 and 15 pF. These (minimum) values are obtained by evaluating the maximum current delivered by M11, which is about 100 μA, and using (26). Note also that these values are much higher than parasitic capacitances (that are in the range of some fF), as required by our analysis to be valid. All the compensation elements are calculated using (21) and are reported in Table II (third and sixth rows).

The frequency response of the loop gain is illustrated in Fig. 9, for both load cases. The *GBW* and ϕ are 7 MHz, 85° and 1.4 MHz, 91° respectively. Again, the phase margin is increased due to the effect of M11. By configuring M11 as a constant bias current the phase margin is reduced by 5° in both cases. The excessive phase margin shows that higher gain-bandwidth products could be achieved by adopting an output stage with higher drive capability in order to prevent *SR* unbalance.

The time response to an input step of $0.5V_{\rm pp}$ with the amplifier in unity-gain configuration is illustrated in Fig. 10. The 0.1% positive and negative settling time is $T_S^{+/-} = 293/275$ ns, and $T_S^{+/-} = 464/417$ ns, for C_L equal to 20 and 100 pF, respectively. The positive and negative *SR* are quite similar and are 2.1 V/μs (for C_L equal to 20 pF) and 0.46 V/μs (for C_L equal to 100 pF). We also established, by using smaller compensation capacitors, that the *SR* unbalance between the second and the output stage produces an overshoot in the closed-loop step response causing the settling time deterioration. To illustrate this concept, Fig. 11 shows two step responses: curve a is obtained setting C_{C2} equal to 10 pF while curve b is obtained setting C_{C2} equal to 5 pF, both with $C_L = 100$ pF. The other values of compensation components are calculated using (21).

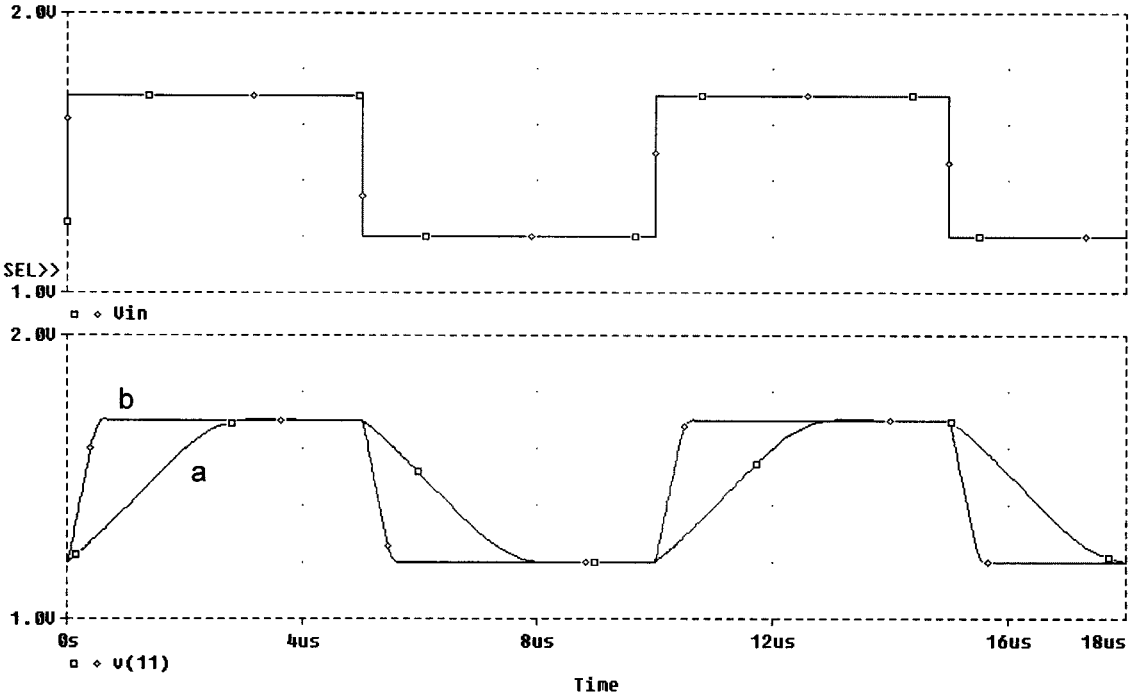

Fig. 8. Step response of the amplifier using the single nulling resistor approach. Curves a and b refer to the case with $C_L = 100$ pF,and $C_L = 20$ pF, respectively.

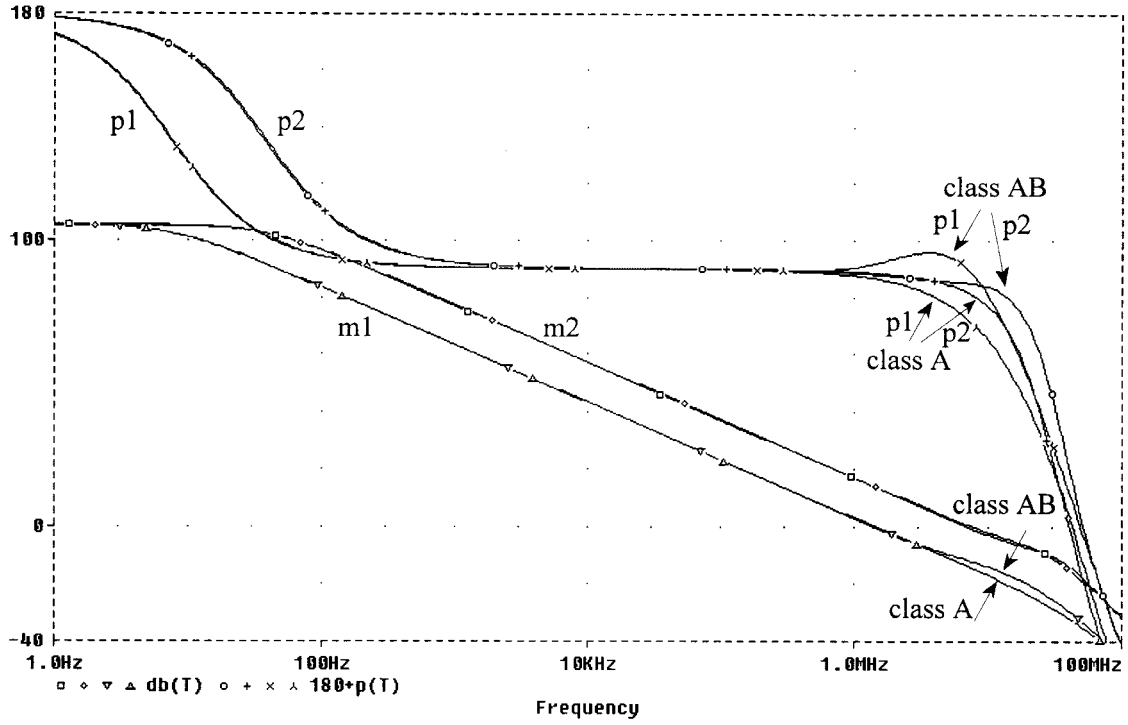

Fig. 9. Loop gain of the amplifier using the pole–zero canceling approach. Curves m1-p1 and m2-p2 refer to the case with $C_L = 100$ pF, and $C_L = 20$ pF, respectively. The influence of transistor M11 on the diagrams is also highlighted.

The positive and negative (0.1%) settling times for curve a were found to be 1.2 μs and 700 ns, respectively, while for curve b they were 942 ns and 474 ns. This means that the lower the C_{C2}, the higher the increase in positive settling time and peaking. We point out that this effect is *only* due to large-signal nonlinear effects of the amplifier, which does not operate as a negative-feedback system, and it is not due to ill-defined stability conditions. In fact, under the same compensation settings the amplifier exhibits a single-pole frequency behavior with a phase margin higher than 85°. Peaking occurred only in the positive transition where the lower maximum current provided by transistor M11 (which is lower than that achievable from M12) limited the output slew-rate performance.

Then, we evaluate the sensitivities of the compensation approach compared to process variations. Note that no tracking biasing technique was utilized, and the compensation resistors

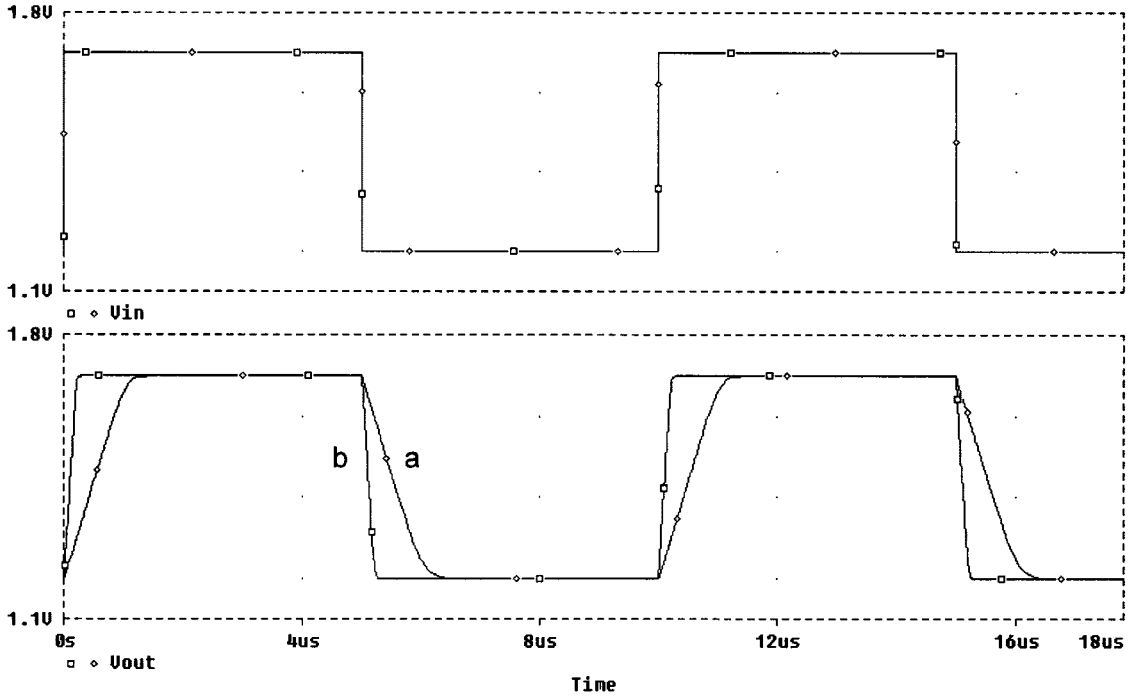

Fig. 10. Step response of the amplifier using the pole–zero canceling approach. Curves a and b refer to the case with $C_L = 100$ pF, and $C_L = 20$ pF, respectively.

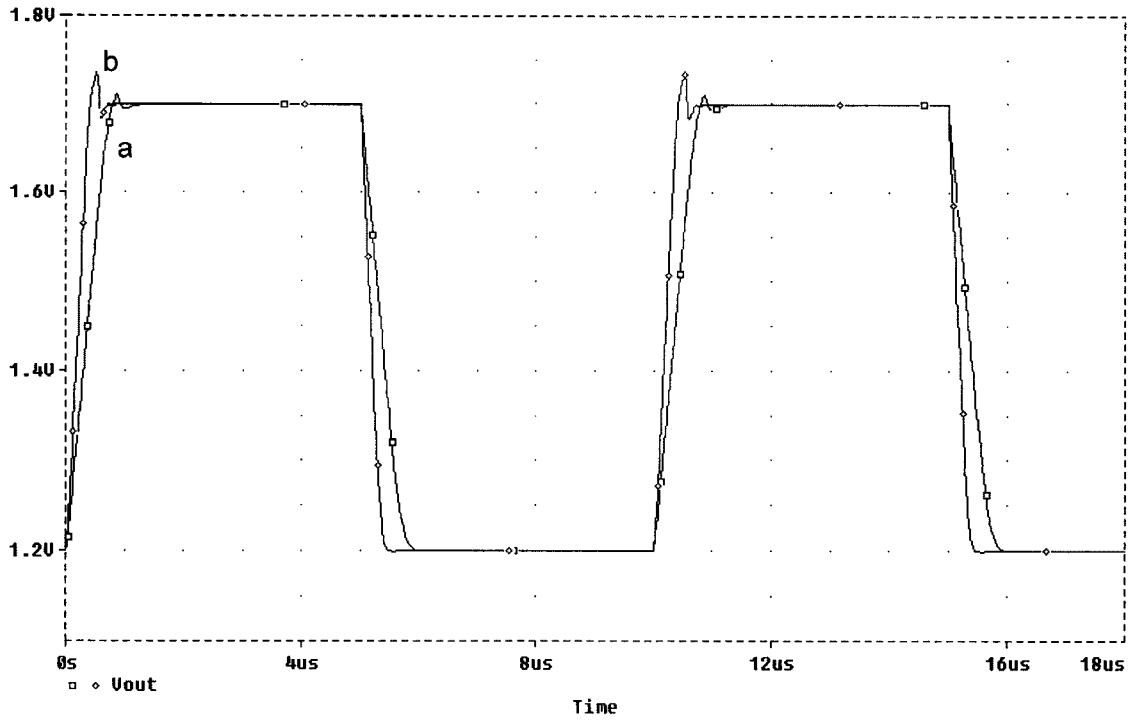

Fig. 11. Step response showing overshoot due to SR unbalance between the second and third stage. Curve. a and b are obtained setting C_{C2} equal to 10 pF, and 5 pF, respectively, both using a 100-pF load.

were assumed as linear on chip resistors. When only the load capacitance, C_L, is change d by 20%, the phase margin varies only by 2°. While for a 20% variation in both compensation resistances the phase margin varies by 4°. In both cases the *GBW* remains almost unchanged. This is explained by the fact that *GBW* depends only on g_{m1} and C_{C1}. Indeed, a 20% variation in both C_{C1} and C_{C2} produces the same percentage variation in *GBW* (caused by C_{C1} only) and a deviation from the nominal phase margin of 3°. Finally, Montecarlo simulations were performed to evaluate the impact of transistor mismatches on the *GBW* and ϕ whose biggest deviations were as high 25% and 2° respectively.

Table III summarizes the simulated ω_{GBW} and ϕ for the above cases, all with transistor M11 connected as in Fig. 6.

TABLE III
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN FOR DIFFERENT ZERO-CANCELING APPROACHES

Zero cancellation technique	C_L (pF)	*GBW* (MHz)	ϕ (°)
ideal voltage followers	20	1.8	70
as in reference [15]		2.5	73.4
proposed		7.0	85
ideal voltage followers	100	0.4	70.5
as in reference [15]		0.5	74.6
proposed		1.4	91

VI. CONCLUSIONS

In this paper, novel design procedures for three-stage nested-Miller compensated amplifiers were discussed. First we defined a simple compensation strategy which accurately controls the phase margin of the main amplifier as well as that of the internal loop. This method provides stable circuits with controlled settling behavior, provided that the *SR* balance condition of the internal loop is also verified.

The use of nulling resistors in the compensation network was also investigated and existing techniques were reinterpreted at the light of the above approach. Finally, a new double pole–zero canceling technique was proposed, which eliminates the first two nondominant poles of the open-loop amplifier. The approach enables high-speed, low power dissipation and is also well suited for amplifiers with heavy capacitive loads. The method requires lower values of compensation capacitors. Thus the unity-gain frequency, settling time and slew-rate performance can be considerably improved without any increases in power dissipation. Compared to previously published standard and even optimized approaches, the proposed one permits remarkable bandwidth and settling improvement, and provides a *GBW* which is in the same range as that achievable by a two-stage Miller-compensated OTA under the same load conditions and comparable power dissipation. Simulations in excellent agreement with the theoretical analysis were also given.

APPENDIX

Let $A(s)$ be the open-loop gain of a dominant-pole amplifier characterized by a dc gain A_o, a dominant pole ω_{p1}, a nondominant pole ω_{p2} and a zero ω_z

$$A(s) = A_o \frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{A.1}$$

where $A_0 \gg 1$ and $\omega_{p1} \ll \omega_{p2}, \omega_z$. By closing $A(s)$ in unity-gain loop, the resulting transfer function is

$$A_{CL}(s) = \frac{1}{1+\frac{1}{A(s)}} \approx \frac{\left(1+\frac{s}{\omega_z}\right)}{1+\left(\frac{1}{\omega_z}+\frac{1}{A_o\omega_T}\right)s+\frac{1}{\omega_T\omega_{p2}}s^2} \tag{A.2}$$

Note that although ω_{p2} and ω_z could be of the same order of magnitude, only the zero modifies the cut-off frequency of $A_{CL}(s)$. Specifically, the cut-off frequency is decreased or increased by the action of a RHP or a LHP zero, respectively.

Now, let $A(s)$ be the open-loop gain of the inner amplifier in Fig. 2, with its dc gain, poles and the transition frequency given by (5) – (6) and with the RHP zero equal to g_{m3}/C_{C2}. Under these assumptions the denominator of (A.2) exactly equals the second-order polynomial given in (1). Moreover, as a particular case, if the frequency of the zero is infinitely large, (A.2) is equal to (4).

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Gaetano Palumbo (M'91–SM'98) was born in Catania, Italy, in 1964. He received the laurea degree in electrical engineering in 1988, and the Ph.D. degree in 1993, both from the University of Catania, Catania, Italy.

In 1994, he joined the DEES (Dipartimento Elettrico Elettronico e Sistemistico) at the University of Catania as a Researcher, subsequently becoming Associate Professor in 1998, and a full Professor in the same department, since 2000. His primary research interest has been analog circuits with particular emphasis on feedback circuits, compensation techniques, current-mode approach, and low-voltage circuits. In recent years, his research has also embraced digital circuits with emphasis on bipolar and MOS current-mode digital circuits, adiabatic circuits, and high-performance building blocks focused on achieving optimum speed within the constraint of low power operation. In all these fields he is developing some research in collaboration with STMicroelectronics of Catania.

He was the co-author of the books *CMOS Current Amplifiers* (Norwell, MA: Kluwer, 1999), and *Feedback Amplifiers: theory and design* (Norwell, MA: Kluwer, 2001). He is a contributor to the *Wiley Encyclopedia of Electrical and Electronics Engineering*. In addition, he is the author or co-author of more than 180 scientific papers on referred international journals (over 70) and in conferences. From June 1999 to the end of 2001 he served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I, for "Analog Circuits and Filters."

Salvatore Pennisi (M'01) was born in Catania, Italy, in 1965. He received the laurea degree in electronics engineering in 1992, and the Ph.D. degree in electrical engineering, both from the University of Catania, Catania, Italy, in 1997.

In 1996, he joined the DEES (Dipartimento Elettrico Elettronico e Sistemistico) at the University of Catania as an Assistant Professor and teaches courses on Electronics and Microelectronics. His primary research interests include circuit theory and analog design with emphasis on current-mode techniques. In this field, he has developed various innovative building blocks and unconventional architectures for operational amplifiers. More recently, his research activities have involved low- voltage/low-power circuits, multistage amplifiers, and IF CMOS blocks.

Dr. Pennisi is the author or co-author of more than 70 publications on international journals and conferences, as well as of the books *CMOS Current Amplifiers* (Norwell, MA: Kluwer, 1999), and *Feedback Amplifiers-Theory and Design* (Norwell, MA: Kluwer, 2001), and has written an entry in the *Wiley Encyclopedia of Electrical and Electronics Engineering*