Three-Stage Large Capacitive Load Amplifier with Damping-Factor-Control Frequency Compensation

Ka Nang Leung, Philip K. T. Mok, *Member, IEEE*, Wing-Hung Ki, *Member, IEEE*, and Johnny K. O. Sin, *Senior Member, IEEE*

***Abstract*—A novel damping-factor-control frequency compensation (DFCFC) technique is presented in this paper with detailed theoretical analysis. This compensation technique improves frequency response, transient response, and power supply rejection for amplifiers, especially when driving large capacitive loads. Moreover, the required compensation capacitors are small and can be easily integrated in commercial CMOS process.**

Amplifiers using DFCFC and nested Miller compensation (NMC) driving two capacitive loads, 100 and 1000 pF, were fabricated using a 0.8-μm CMOS process with $V_{\rm tn} = 0.72$ V and $V_{\rm tp} = -0.75$ V. For the DFCFC amplifier driving a 1000-pF load, a 1-MHz gain-bandwidth product, 51° phase margin, 0.33-V/μs slew rate, 3.54-μs settling time, and 426-μW power consumption are obtained with integrated compensation capacitors. Compared to the NMC amplifier, the frequency and transient responses of the DFCFC amplifier are improved by one order of magnitude with insignificant increase on the power consumption.

***Index Terms*—Damping factor, frequency compensation, large capacitive load, multistage amplifier.**

I. Introduction

With the rapid decrease in the supply voltage in VLSI, more circuit designers are aware of the importance of low-voltage multistage amplifiers. However, all multistage amplifiers suffer close-loop stability problems due to their multiple-pole nature. Therefore, many frequency compensation topologies have been proposed [1]–[6].

As mentioned by Eschauzier *et al.* [1] and Huijsing *et al.* [2], multistage amplifiers suffer bandwidth reduction, and a single-stage amplifier is optimum on bandwidth. Compared to a single-stage amplifier, the gain-bandwidth products of a two-stage simple Miller compensated (SMC) amplifier and a three-stage nested Miller compensated (NMC) amplifier are reduced to half and one quarter, respectively [1], [2]. As a result, other advanced topologies, such as multipath NMC (MNMC), hybrid NMC (HNMC), multipath HNMC (MHNMC), and nested Gm-C compensation (NGCC), were developed to overcome the bandwidth reduction problem [1]–[5]. For these topologies, which are based on NMC, pole–zero cancellation and feed-forward technique are used to extend the bandwidth.

However, from the findings shown in Fig. 1, the bandwidth improvements by the above-mentioned topologies over NMC are not sufficient, and the provided bandwidths are narrower than the bandwidth of a single-stage amplifier. In addition, tradeoffs between bandwidth and other amplifier characteristics such as settling time and power consumption are required. In particular, higher power consumption is needed to increase the bandwidth when the amplifier is required to drive a large capacitive load such as the error amplifier in a linear regulator. Furthermore, both small-signal and settling behavior should be improved at the same time in order to obtain a fast amplifier [7]. Nevertheless, the above-mentioned topologies are mainly concerned with the improvement of the frequency response.

Another issue to be considered is the optimum number of gain stages. Generally, frequency compensation techniques for three-stage amplifiers are adequate for practical purposes since three-stage amplifiers maintain a good compromise between the voltage gain ($\sim$100 dB) and power consumption. Any extra gain stage complicates the circuit structure and increases the complexity of the frequency compensation.

With respect to the above problems, a novel damping-factor-control frequency compensation (DFCFC) technique [8] is presented in this paper. As illustrated in Fig. 1 and shown later in the paper, this topology substantially increases the bandwidth of a three-stage amplifier, especially when driving large capacitive loads. The improvement can be as large as one order of magnitude. Furthermore, a DFCFC amplifier is able to provide a wider bandwidth than a single-stage amplifier with significantly improved transient response and power supply rejection ratio. To achieve the above enhancements, the required values of the compensation capacitors are small, and there is a small increase on the power consumption and circuit complexity.

In the next section, a brief review on NMC is given. The purpose of the review is to take NMC as a common reference when comparing DFCFC to all published topologies. DFCFC is introduced in Section III. The transfer function, stability criteria, transient response, and power supply rejection ratio are addressed. In Sections IV and V, the implementation of the structure and experimental results are presented. Finally, the conclusion of this paper is given in Section VI.

II. Brief Review on NMC

The structure and equivalent circuit of a three-stage amplifier using NMC is shown in Fig. 2. The transconductance, output resistance, and lumped output parasitic capacitance of the gain stages are notated by $g_{m(1-3)}$, $R_{(1-3)}$, and $C_{p(1,2)}$, respectively. C_{m1} and C_{m2} are the compensation capacitors, and C_L is the loading capacitance. It should be noted that in order to obtain

Manuscript received July 2, 1999; revised September 30, 1999. This work was supported by the RGC Competitive Earmarked Research Grant HKUST6007/97E, Hong Kong SAR Government.

The authors are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, China.

Publisher Item Identifier S 0018-9200(00)00938-0.

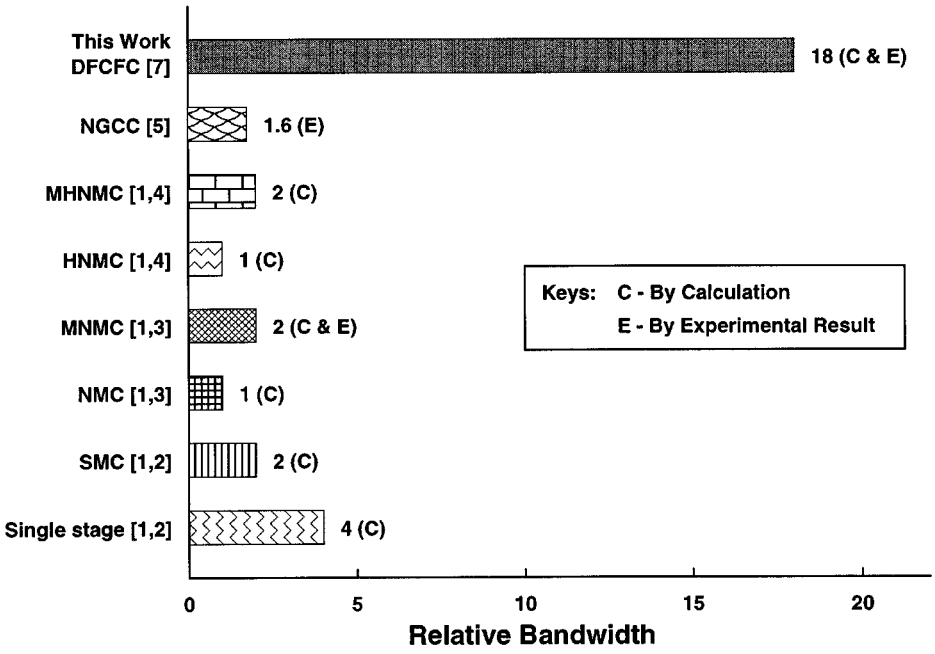

Fig. 1. Bandwidth comparison of different frequency compensation topologies (take NMC as the reference).

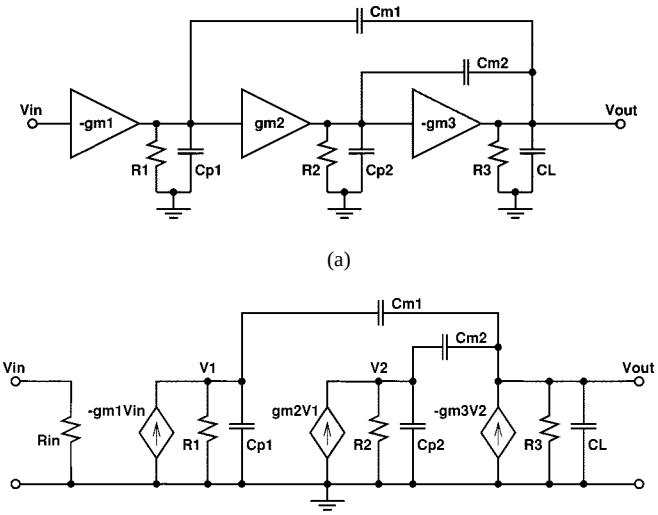

Fig. 2. (a) Structure of a three-stage NMC amplifier. (b) Equivalent small-signal circuit of the three-stage NMC amplifier.

negative capacitive feedback loops by C_{m1} and C_{m2}, the gains of the second stage and output stage are positive and negative, respectively.

As there are three high impedance nodes in the structure, there are three poles. Solving the equivalent circuit with the following assumptions: 1) C_{m1}, C_{m2}, and $C_L \gg C_{p1}$ and C_{p2}, and 2) $g_{m3} \gg g_{m1}$ and g_{m2}, the small-signal transfer function, $A_{v(\mathrm{NMC})}(s) = (V_{\mathrm{out}}(s)/V_{\mathrm{in}}(s))$, is calculated as

$$A_{v(\mathrm{NMC})}(s) = \frac{A_{\mathrm{dc}}}{\left(1+\frac{s}{p_{-3\,\mathrm{B}}}\right)\left(1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_L C_{m2}}{g_{m2}g_{m3}}\right)} \quad (1)$$

where $A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the dc gain, and $p_{-3\ \mathrm{dB}} = (C_{m1}g_{m2}g_{m3}R_1R_2R_3)^{-1}$ is the dominant pole. To stabilize the NMC amplifier, the NMC amplifier should have third-order Butterworth frequency response [9] in unity-feedback configuration, and C_{m1} and C_{m2} should obey the following dimension conditions [1]–[3]:

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_L \quad (2)$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_L. \quad (3)$$

From the second-order function at the denominator of (1), the positions of the second and third pole depend on C_{m2} and C_L, and the damping factor of the second-order function is controlled by C_{m2}. From (1) and (3), the nondominant poles depends on C_{m2} and thus depends on the loading capacitance C_L. This is not preferable as the loading capacitance will affect the location of the nondominant poles and therefore affects the stability of the amplifier. When driving a large capacitive load, a larger C_{m2} is required, and the nondominant poles will locate at rather low frequencies. Therefore, the bandwidth of an NMC amplifier is poor.

Substituting the dimension conditions of C_{m1} and C_{m2} into (1), the second and third pole will form a complex pole with damping factor of $1/\sqrt{2}$. The gain-bandwidth product $\mathrm{GBW}_{(\mathrm{NMC})}$ and phase margin $\mathrm{PM}_{(\mathrm{NMC})}$ are [1]

$$\mathrm{GBW}_{(\mathrm{NMC})} = \frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) \quad (4)$$

$$\mathrm{PM}_{(\mathrm{NMC})} \approx 60^\circ. \quad (5)$$

From the above results, the gain-bandwidth product decreases as the loading capacitance increases. The only method to in-

crease the bandwidth of an NMC amplifier is to enlarge g_{m3} by increasing the quiescent current and size of the transistors of the output gain stage. Moreover, from the design point of view, NMC is not suitable for low-power design as the previously stated assumption, $g_{m3} \gg g_{m1}$ and g_{m2}, may not be valid. Although small bias current and small transistor size can reduce g_{m2} such that g_{m2} is smaller than g_{m3}, the same does not apply to g_{m1}. This is due to the small bias current at the input stage which reduces the slew rate of the amplifier [10]–[15] and the small size of the input differential pair, which introduces a large offset voltage [15]. Thus, NMC may not be suitable for amplifiers driving large capacitive loads and in low-power designs.

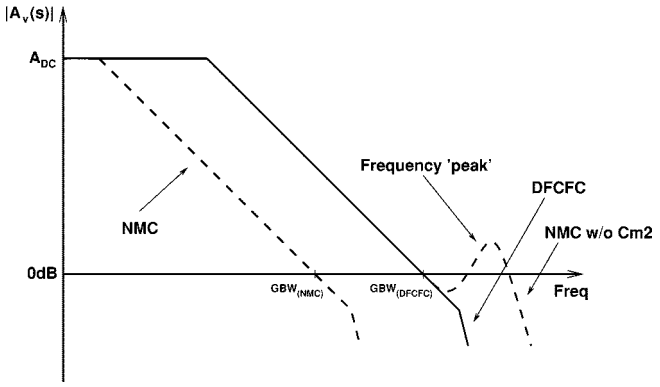

Fig. 3. Bode plot of the frequency responses.

III. DFCFC

In this section, detailed analysis on the transfer function, stability criteria, slew rate, settling time, and power supply rejection ratio of the proposed DFCFC structure are discussed.

A. Structure of DFCFC

From the discussion in the previous section, the poor bandwidth of an NMC amplifier is mainly due to the presence of C_{m2}, which is part of capacitive load to the amplifier [1], [6]. By eliminating C_{m2}, the capacitive load at the output is reduced. The nondominant poles will then relocate at higher frequencies, and the bandwidth of the NMC amplifier can be extended. Nevertheless, the two nondominant poles form a complex pole. The damping factor of the complex pole is very small. Moreover, there is no control of the damping factor as C_{m2} is absent. As shown in Fig. 3, the small damping factor causes a frequency 'peak' to appear near the unity-gain frequency of the amplifier, and this prohibits stable close-loop operation.

In order to obtain a larger bandwidth and stabilize the amplifier at the same time, DFCFC is used. The structure and the equivalent circuit are shown in Fig. 4. There are two additional building blocks: 1) the feed-forward transconductance stage (FTS) and 2) the damping-factor-control (DFC) block. The function of the FTS is to implement a push–pull output stage to improve the slewing performance. The DFC block is used to control the damping factor of the nondominant complex pole to make the amplifier stable. The resultant open-loop frequency response of the DFCFC amplifier is shown in Fig. 3. The DFCFC bandwidth is wider than that of the NMC amplifier.

For the details of the two additional blocks, the DFC block is simply a negative gain stage with transconductance g_{m4}, output resistance R_4, and lumped parasitic capacitance C_{p4}. The dc gain of this stage must be greater than one to validate the mathematical derivation of the transfer function shown in next section. The FTS block is merely a transistor with transconductance $-g_{mf2}$. The input signal of the FTS is from the output of the first stage (V_1 in Fig. 4). As will be explained in detail in the following sections, the two additional building blocks significantly improve the bandwidth and transient response.

B. Transfer Function

To analyze the stability of the DFCFC amplifier, the small-signal transfer function should be investigated. Solving the circuit network shown in Fig. 4 by setting $C_{m2} = C_{m1}$ to simplify the expression and with the following assumptions. 1) The dc gain of the DFC block is greater than one; 2) C_{p1} and C_{p4} are smaller than the compensation capacitances, loading capacitance, and C_{p2} (C_{p2} is generally larger than other parasitic capacitances as it depends on the size of the transistor of the output stage), the transfer function is given by (6), shown at the bottom of the page, where $A_{\rm dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the dc gain, and $p_{-3\ {\rm dB}} = (C_{m1}g_{m2}g_{m3}R_1R_2R_3)^{-1}$ is the dominant pole. It should be noted that the effect of C_{m2} is canceled in the transfer function, so it is not always necessary to set $C_{m2} = C_{m1}$. The above transfer function holds true as long as $C_{m2} \gg C_{p2}$. If C_{m1} is small, C_{m2} should be set to equal C_{m1}; otherwise, set $C_{m1} > C_{m2} > C_{p2}$ to further optimize the size of the compensation capacitors.

From (6), shown at the bottom of the page, it is obvious that the damping factor and location of the complex pole can be controlled by an optimum value of g_{m4}, and the gain-bandwidth

$$A_{v(\rm DFCFC)}(s) = \frac{A_{dc}\left(1 + s\dfrac{C_{p2}g_{mf2} - C_{m1}g_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} - s^2\dfrac{C_{p2}C_{m1}}{g_{m2}g_{m3} + g_{mf2}g_{m4}}\right)}{\left(1 + \dfrac{s}{p_{-3\ {\rm dB}}}\right)\left(1 + s\dfrac{C_Lg_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{m3} + g_{mf2}g_{m4}}\right)}$$
$$\approx \frac{1 + s\dfrac{C_{p2}g_{mf2} - C_{m1}g_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} - s^2\dfrac{C_{p2}C_{m1}}{g_{m2}g_{m3} + g_{mf2}g_{m4}}}{s\dfrac{C_{m1}}{g_{m1}}\left(1 + s\dfrac{C_Lg_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{m3} + g_{mf2}g_{m4}}\right)} \quad (6)$$

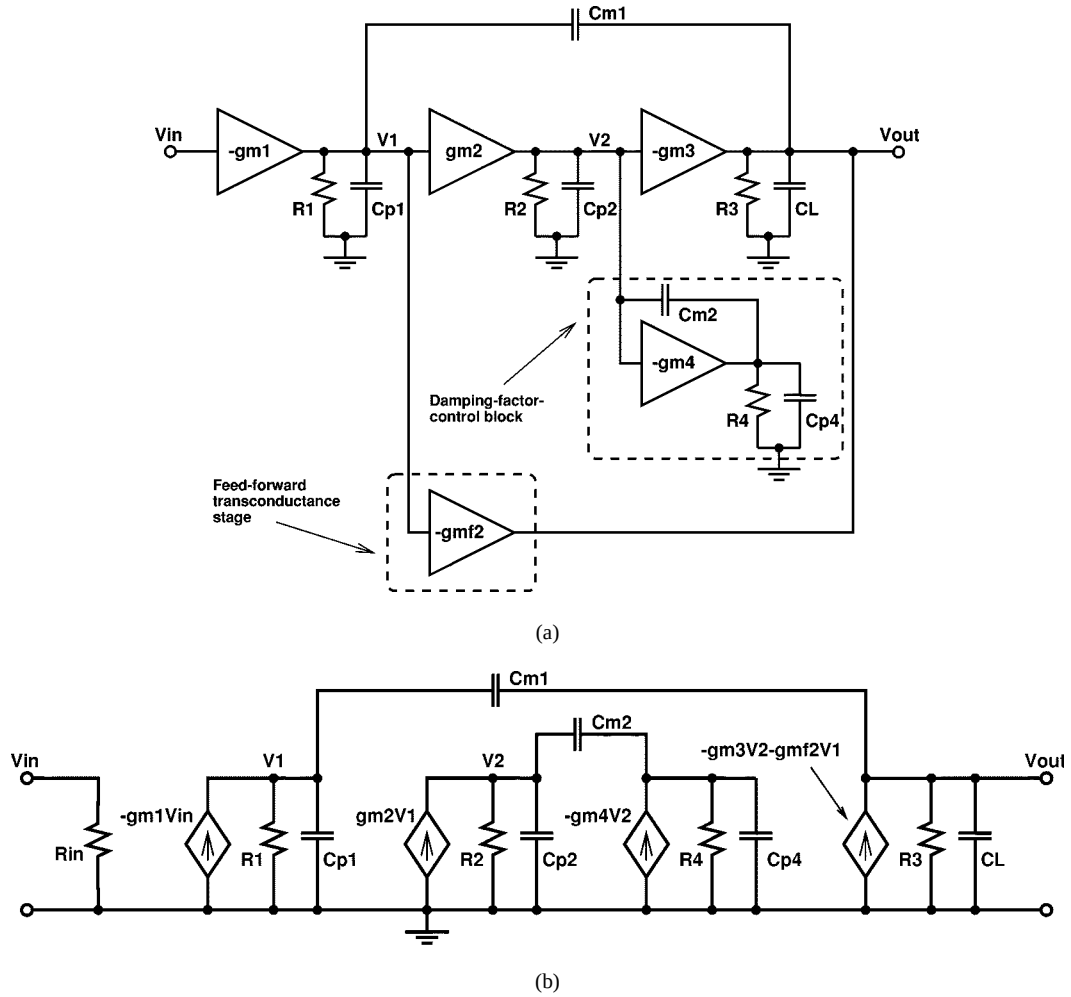

Fig. 4. (a) Structure of a DFCFC amplifier. (b) Equivalent small-signal circuit of the DFCFC amplifier.

product is controlled by C_{m1}. Moreover, the nondominant poles locate at higher frequencies as the second-order function depends on the parasitic capacitance C_{p2} instead of C_{m2}, which is loading capacitance dependent in NMC topology.

C. Stability Criteria, Gain-Bandwidth Product, and Phase Margin

From the previous section, it is known that the stability of the amplifier can be controlled by appropriate values of C_{m1} and g_{m4}. In this section, the dimension conditions are calculated.

We model the transfer function with ideal function first and then apply the results. To begin, assuming that the effect of the zeros is negligible and considering that the poles of the DFCFC amplifier in unity-feedback configuration have third-order Butterworth frequency response [9], the transfer function in unity-gain feedback $H(s)$ with cut-off frequency (ω_o) is given by

$$H(s) = \frac{A_{v(\mathrm{DFCFC})}(s)}{1 + A_{v(\mathrm{DFCFC})}(s)} = \frac{1}{1 + s\left(\frac{2}{\omega_o}\right) + s^2\left(\frac{2}{\omega_o^2}\right) + s^3\left(\frac{1}{\omega_o^3}\right)}. \quad (7)$$

To obtain (7), the open-loop transfer function should be in the following format:

$$A_{v(\mathrm{DFCFC})}(s) = \frac{1}{s\frac{2}{\omega_o}\left[1 + s\left(\frac{1}{\omega_o}\right) + s^2\left(\frac{1}{2{\omega_o}^2}\right)\right]} \quad (8)$$

$$= \frac{1}{s\frac{2}{\omega_o}\left[1 + s\left(\sqrt{2}\right)\left(\frac{1}{\sqrt{2}\omega_o}\right) + s^2\frac{1}{(\sqrt{2}\omega_o)^2}\right]}. \quad (9)$$

Considering a typical second-order function $S(s)$ with damping factor (ζ) and corner frequency (ω_n), $S(s)$ is given by

$$S(s) = 1 + s\left(2\zeta\right)\left(\frac{1}{\omega_n}\right) + s^2\left(\frac{1}{{\omega_n}^2}\right). \quad (10)$$

By comparing the denominator of (9) with (10), it is proven that the damping factor of the nondominant complex pole in open loop is $1/\sqrt{2}$ if the amplifier has third-order Butterworth frequency response in unity-feedback configuration. Therefore, the magnitude plot of the amplifier in open loop has no frequency "peak." The position of the nondominant complex pole $|p_{2,3}|$

is obtained by solving the second-order function in (8) and is given by

$$|p_{2,3}| = \sqrt{2}\omega_o. \tag{11}$$

The gain-bandwidth product $\mathrm{GBW}_{(\mathrm{DFCFC})}$ of the amplifier is given by

$$\mathrm{GBW}_{(\mathrm{DFCFC})} = \frac{\omega_o}{2} \tag{12}$$

and the phase margin $\mathrm{PM}_{(\mathrm{DFCFC})}$ [16] is expressed by

$$\begin{aligned}\mathrm{PM}_{(\mathrm{DFCFC})} &= 180^\circ - \tan^{-1}\left[\frac{\mathrm{GBW}_{(\mathrm{DFCFC})}}{p_{-3\ \mathrm{dB}}}\right] \\ &\quad - \tan^{-1}\left[\frac{2\zeta\left(\dfrac{\mathrm{GBW}_{(\mathrm{DFCFC})}}{|p_{2,3}|}\right)}{1-\left(\dfrac{\mathrm{GBW}_{(\mathrm{DFCFC})}}{|p_{2,3}|}\right)^2}\right] \\ &= 180^\circ - \tan^{-1}\left(\frac{A_{\mathrm{dc}}\cdot p_{-3\ \mathrm{dB}}}{p_{-3\ \mathrm{dB}}}\right) \\ &\quad - \tan^{-1}\left[\frac{2\left(\dfrac{1}{\sqrt{2}}\right)\left(\dfrac{\omega_o/2}{\sqrt{2}\omega_o}\right)}{1-\left(\dfrac{\omega_o/2}{\sqrt{2}\omega_o}\right)^2}\right] \\ &\approx 60^\circ. \end{aligned} \tag{13}$$

By applying the above modeling on DFCFC, three equations are obtained by comparing the coefficients of the denominator of (8) with those of (6).

$$\frac{2}{\omega_o} = \frac{C_{m1}}{g_{m1}} \tag{14}$$

$$\frac{1}{\omega_o} = \frac{C_L g_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} \tag{15}$$

$$\frac{1}{2{\omega_o}^2} = \frac{C_{p2}C_L}{g_{m2}g_{m3} + g_{mf2}g_{m4}}. \tag{16}$$

By substituting (15) into (16) to eliminate ω_o, a quadratic equation of g_{m4} is derived.

$$\left(\frac{C_L}{C_{p2}}\right) g_{m4}^2 - (2g_{mf2})g_{m4} - 2g_{m2}g_{m3} = 0. \tag{17}$$

By solving the above equation and rejecting the negative solution of g_{m4}, the dimension condition of g_{m4} in DFCFC is given by

$$g_{m4} = g_{mf2}\left(\frac{C_{p2}}{C_L}\right)\left[1+\sqrt{1+2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2}g_{m3}}{g_{mf2}^2}\right)}\right]. \tag{18}$$

For the dimension condition of C_{m1}, it can be obtained by firstly substituting (15) into (14) to acquire

$$C_{m1} = \frac{2g_{m1}g_{m4}C_L}{g_{m2}g_{m3} + g_{mf2}g_{m4}} \tag{19}$$

and then substituting (18) into (19) to obtain

$$C_{m1} = \frac{4}{1+\sqrt{1+2\left(\dfrac{C_L}{C_{p2}}\right)\left(\dfrac{g_{m2}g_{m3}}{g_{mf2}^2}\right)}}\left(\frac{g_{m1}}{g_{mf2}}\right)C_L. \tag{20}$$

Since it is preferable to have the same output current capability for both the p- and the n-transistor of the output stage, the sizes of the p- and n-transistor are used in the ratio of 3 to 1 to compensate for the difference in the mobilities of the carriers. Thus, it is reasonable to set $g_{mf2} = g_{m3}$, and (18) and (20) are rewritten as

$$g_{m4} = \beta\cdot\left(\frac{C_{p2}}{C_L}\right)g_{m3} \tag{21}$$

$$C_{m1} = \frac{1}{\beta}\cdot\left[4\left(\frac{g_{m1}}{g_{m3}}\right)C_L\right] \tag{22}$$

where

$$\beta = 1+\sqrt{1+2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2}}{g_{m3}}\right)}. \tag{23}$$

Since the dimension conditions of C_{m1} and g_{m4} depend on the ratios of transconductances and capacitances, the stability of the DFCFC amplifier is less sensitive to global variations of circuit parameters.

From (23), β is larger for a larger C_L to C_{p2} ratio, and the value can be much greater than one in some cases. The required C_{m1} is reduced by β times when compared to (2) for NMC. In addition, since the product of β and C_{p2}/C_L in (21) is a decreasing function with C_L, the required g_{m4} is small and only a small amount of power is dissipated in the DFC block.

As the zeros of the amplifier depend on C_{m1} (which is small as proven previously) and C_{p2}, they are at higher frequencies than the poles of the amplifier and the effect from the zeros can be neglected. Therefore, the previously stated assumption is valid, and the presence of zeros does not invalidate the stability criteria.

From (12) to (14), the gain-bandwidth product and phase margin of the DFCFC amplifier are given by

$$\begin{aligned}\mathrm{GBW}_{(\mathrm{DFCFC})} &= \frac{g_{m1}}{C_{m1}} \\ &= \beta\cdot\left[\frac{1}{4}\left(\frac{g_{m3}}{C_L}\right)\right] \\ &= \beta\cdot\mathrm{GBW}_{(\mathrm{NMC})}\end{aligned} \tag{24}$$

$$\mathrm{PM}_{(\mathrm{DFCFC})} \approx 60^\circ. \tag{25}$$

It can be shown from (24) that the bandwidth of a DFCFC amplifier is β times that of an NMC amplifier. The improvement by DFCFC is greater for a larger β (i.e., a larger loading capacitance). Referring to Fig. 1, the bandwidth of the DFCFC amplifier may be even larger than a single-stage amplifier when β is larger than 4. Also, there is no degradation on the phase margin when using DFCFC. If the required phase margin is less than 60° in some applications, a smaller C_{m1} can be used to decrease the phase margin and further increase the bandwidth of the amplifier.

D. Slew Rate

After the analysis on AC behavior, the transient behavior is studied in this section and the next section. Assuming that the output stage is of push–pull or class-AB type, the slew rate is not limited by the output stage. Thus, the slew rate of a multistage amplifier depends on two factors. One is the value of the compensation capacitor C_m, and the other is the amount of current to charge the compensation capacitor $I_{\rm charge}$ [10]–[15]. In mathematical expression, the slew rate $(\rm SR)$ is expressed as

$$SR = \frac{I_{\rm charge}}{C_m}. \tag{26}$$

From the above expression, the increase in the slew rate can be achieved by either increasing the bias current or reducing the value of the compensation capacitor. Increasing the bias current will increase the static power consumption, so it is not preferred in low-power design. Therefore, the most efficient method to increase the slew rate is to reduce the value of the compensation capacitor. However, the compensation capacitor cannot be reduced arbitrarily; otherwise, the amplifier will be unstable in the close-loop operation.

By comparing (22) with (2), as the required value of the compensation capacitor in DFCFC is reduced by β times, the improvement on the slew rate using DFCFC is improved by β times. Similar to the frequency response, the improvement by DFCFC on the slew rate is larger for a large C_L to C_{p2} ratio. Therefore, the slew rate of a DFCFC amplifier is better than that of the NMC counterpart, especially when driving a large capacitive load.

E. Settling Time

Settling behavior of an amplifier is very essential in analog design since it directly affects the performance of the circuits using the amplifier. To enhance the settling behavior, the first thing to investigate is its dependence. Neglecting the short duration of the small-signal response before slewing, the settling time (T_s) can be mainly divided into two periods. They are the slewing period $(T_{\rm slew})$ and quasi-linear period $(T_{\rm quasi})$ [10], [11]. The dependence of the slew rate has been discussed in the previous section, and the slew rate is proven to be greatly improved by DFCFC. For the quasi-linear period, it is a strong function of the phase margin [17], and it also depends on how compressed pole–zero doublet is below the unity-gain frequency of the amplifier [1], [3].

In the case of using DFCFC, as there is no pole–zero doublet, the quasi-linear period only depends on the phase margin. By using the stability criteria stated before, the phase margin of the DFCFC amplifier is approximately 60°, which is a very reasonable value to obtain a short quasi-linear period. As a result, there are not many decaying sinusoidal cycles, and the output voltage can settle within a very short duration.

F. Power Supply Rejection Ratio

The power supply rejection ratio $(\rm PSRR)$ of a single-stage cascode amplifier is excellent as the cascode configuration provides a good isolation between the supply and the output of the amplifier. However, the $\rm PSRR$ in a noncascode multistage amplifier is inferior due to the poorer isolation barrier of a single transistor. Moreover, when the compensation network is required, the compensation capacitors are short-circuited at high frequencies, and the high-frequency supply variations easily bypass through the compensation capacitor to the output of the amplifier.

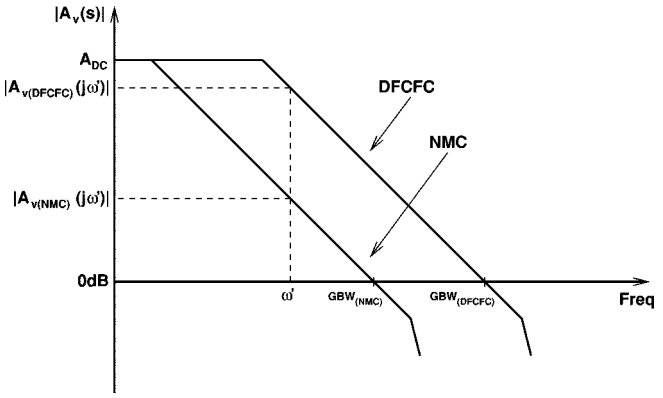

Fig. 5. High-frequency gain of the NMC and DFCFC amplifiers.

The $\rm PSRR$ is defined by the following expression [15]:

$$\rm PSRR = 20\ \log_{10}\left[\frac{|A_v(j\omega)|}{|A_{\rm supply}(j\omega)|}\right] \tag{27}$$

where $|A_v(j\omega)|$ is the open-loop input-to-output voltage gain, and $|A_{\rm supply}(j\omega)|$ is the supply-to-output voltage gain. It can be shown from the above equation that the $\rm PSRR$ can be improved by obtaining a larger $|A_v(j\omega)|$ and a smaller $|A_{\rm supply}(j\omega)|$. A larger $|A_v(j\omega)|$ can be achieved by increasing the gain-bandwidth product of the amplifier. As illustrated in Fig. 5, at a particular frequency ω', the gain obtained from the DFCFC amplifier is $|A_{v(\rm DFCFC)}(j\omega')|$, which is much larger than $|A_{v(\rm NMC)}(j\omega')|$ of the NMC amplifier. Therefore, compared with NMC, the signal from the input of the DFCFC amplifier is amplified larger, and the output signal appearing at the output is stronger. As a result, the relative effect of the supply noise is less significant.

A reduction in $|A_{\rm supply}(j\omega)|$ can be accomplished by using smaller values of compensation capacitors or completely eliminating the capacitors. In the DFCFC topology, as no inner compensation capacitor is required, the resulting $|A_{\rm supply}(j\omega)|$ is much smaller.

Taking into account both the above-mentioned advantages, the $\rm PSRR$ given by DFCFC is better than that of NMC.

G. Physical Dimension of the DFCFC Amplifier

In the design of multistage amplifiers that drive large capacitive loads, most of the chip area is occupied by the compensation capacitors. As the proposed topology requires smaller compensation capacitors to achieve stability, the required dimension of the whole amplifier is significantly reduced.

IV. Implementation of the Proposed Structure

Low-power 2-V DFCFC and NMC amplifiers, illustrated in Fig. 6, driving two capacitive loads, 100 and 1000 pF, were fabricated using a double-metal double-poly 0.8-μm CMOS process with $V_{\rm tn} = 0.72$ V and $V_{\rm tp} = -0.75$ V from

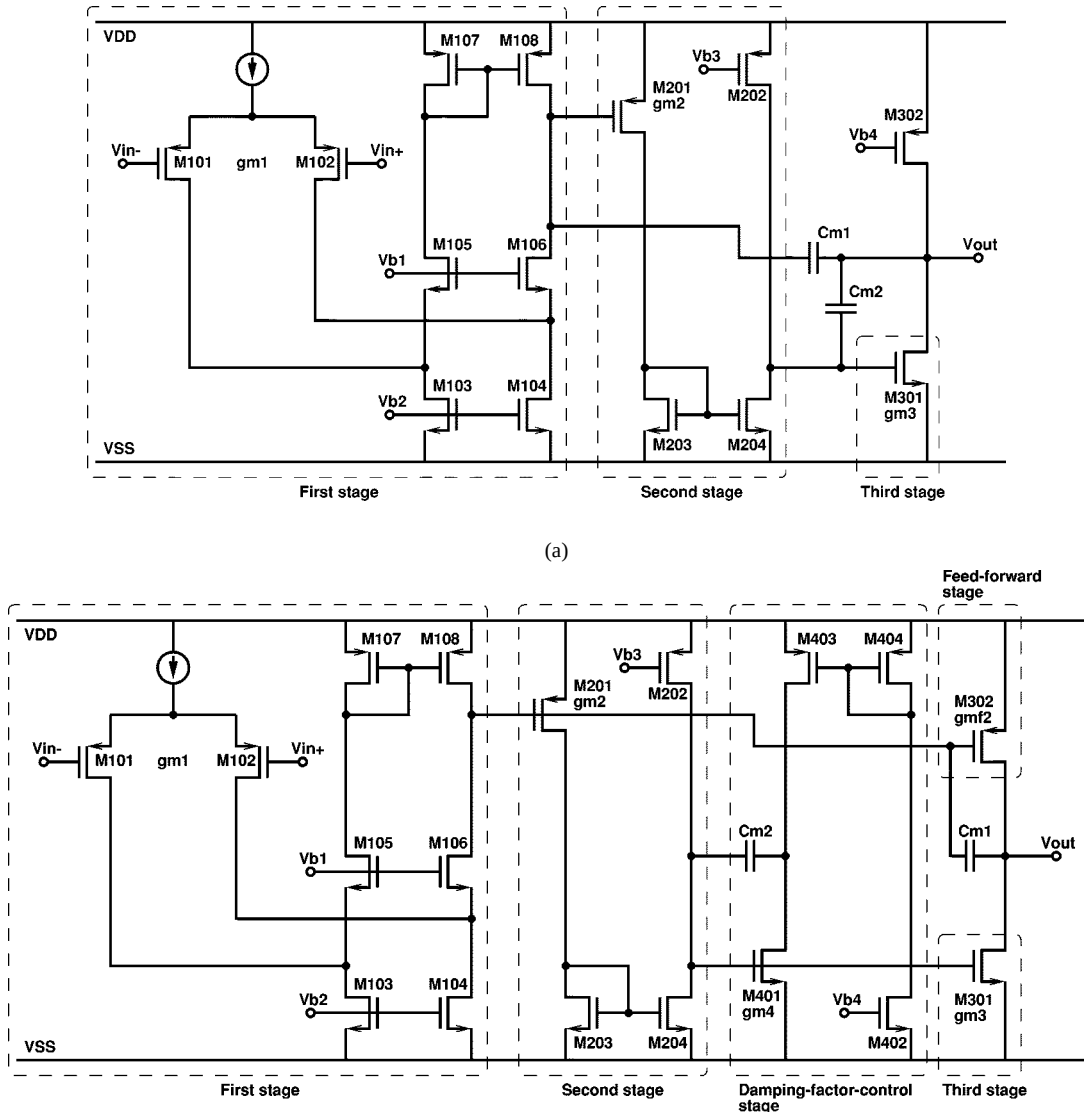

Fig. 6. Circuit diagram of the (a) NMC amplifier and (b) DFCFC amplifier.

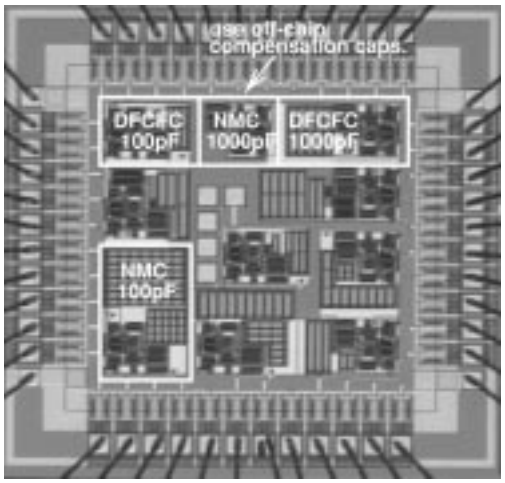

Fig. 7. Micrograph of the amplifiers.

AMS.[1] The micrograph is shown in Fig. 7. For the NMC amplifiers, the first, second and third stages are implemented by M101-M108, M201-M204, and M301, respectively. For the DFCFC counterparts, the additional M302 is the FTS, and M401-M404 is the DFC block. It should be noted that since the circuits are to demonstrate the proposed frequency compensation structure, the circuit structure displayed in Fig. 6 is one of many methods to implement the proposed structure. Additional circuitry to control the dc operating point of the DFC block and to implement a class-AB output stage with feedback control can be added to the circuit structure to build a higher performance amplifier.

To optimize the values of the compensation capacitors in the DFCFC amplifiers, the values of C_{m2} are 3 pF for both 100 and 1000 pF loading conditions. The values of C_{m1} in both cases are obtained from the previous analysis and are fine-tuned to optimize the tradeoff between the bandwidth and phase margin. As shown in Table I, since the values of the compensation capacitors are much smaller for DFCFC, the sizes of the DFCFC

[1] Austria Mikro Systeme International AG, A-8141 Unterpremstatten, Austria.

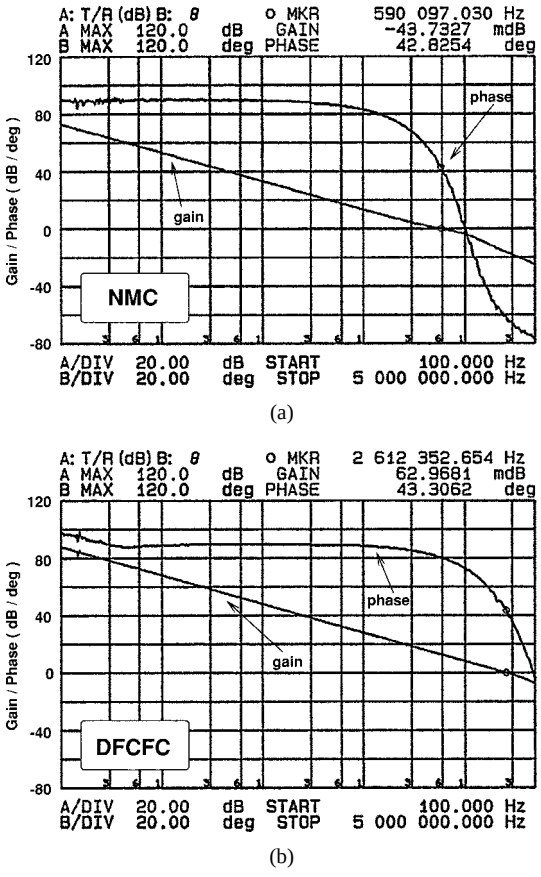

Fig. 8. Frequency responses of the (a) NMC and (b) DFCFC amplifier with 100-pF loading capacitance (only the frequencies near the unity-gain frequency are shown).

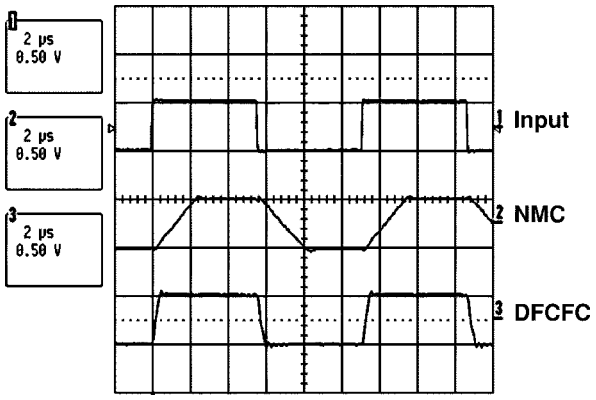

Fig. 9. Transient responses of the amplifiers driving 100 pF.

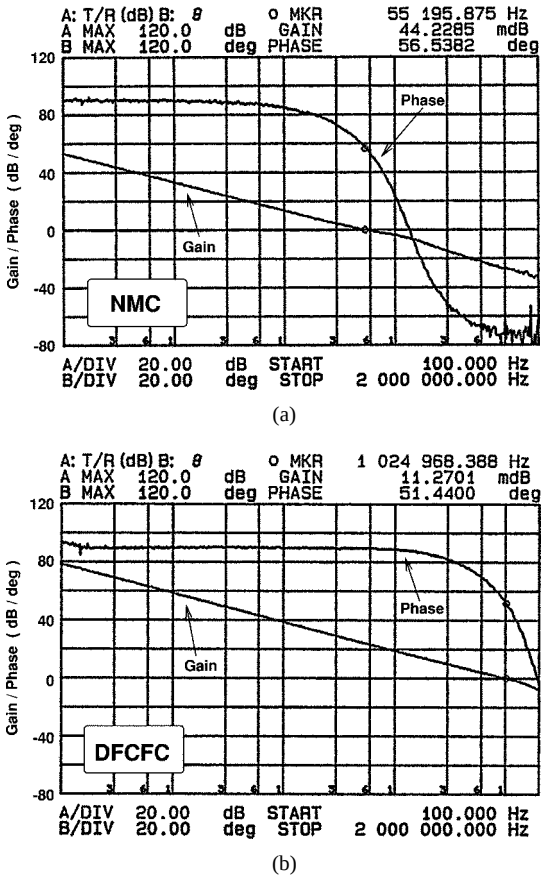

Fig. 10. Frequency responses of the (a) NMC and (b) DFCFC amplifier with 1000-pF loading capacitance (only the frequencies near the unity-gain frequency are shown).

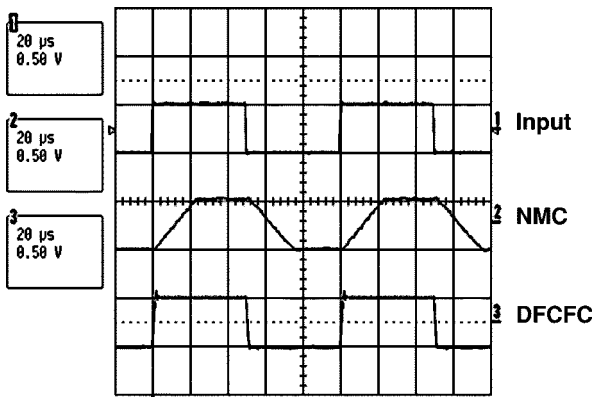

Fig. 11. Transient responses of the amplifiers driving 1000 pF.

amplifiers are small and easy to integrate. On the other hand, the NMC amplifier driving a 1000-pF load requires unrealistic large compensation capacitors ($C_{m1} = 1000$ pF and $C_{m2} = 240$ pF), and thus integration is impossible.

V. Experimental Results

The frequency responses measured with the HP4194A impedance/gain-phase analyzer are shown in Figs. 8 and 10, while the transient responses measured with the LeCroy 9354A oscilloscope are shown in Figs. 9 and 11. The performances are tabulated in Table I.

As shown in the figures and table, by comparing the DFCFC amplifier to the NMC counterpart, DFCFC improves the gain-bandwidth product by 4 times, the slew rate by 6 times, the settling time by 3 times, and the negative power supply rejection ratio by at least 40 dB for the case driving 100 pF. For a larger loading capacitance of 1000 pF, the improvement is more significant. The gain-bandwidth product is improved by 18 times. The slew rate and settling time are improved by 14 and 9 times, respectively. In addition, the negative power supply rejection ratio is enhanced by at least 60 dB. However, there is only negligible increase on the power consumption.

TABLE I
MEASURED RESULTS OF THE NMC AND DFCFC AMPLIFIERS

	NMC	DFCFC	NMC	DFCFC
Loading Condition	100pF//25kΩ		1000pF//25kΩ	
DC Gain	>100dB			
GBW	0.59MHz	2.60MHz	0.055MHz	1.00MHz
PM	43°	43°	56°	51°
SR^+/SR^- (V/μs)	0.23/0.23	1.36/1.27	0.023/0.022	0.33/0.39
T_S^+/T_S^- (μs) (to 1%)	4.25/4.36	0.96/1.37	32.02/32.92	3.54/3.55
$PSRR^+$@1kHz	85.80dB	108.86dB	47.52dB	98.41dB
$PSRR^+$@10kHz	64.10dB	91.93dB	24.49dB	80.63dB
$PSRR^-$@1kHz	53.66dB	93.92dB	18.05dB	85.76dB
$PSRR^-$@10kHz	35.61dB	82.55dB	1.31dB	65.39dB
Output Swing	$-0.85V \leq V_{out} \leq 0.85V$			
Power Consumption	400μW	420μW	400μW	426μW
Power Supply	±1V			
C_{m1}	99pF	18pF	1000pF	55pF
C_{m2}	27pF	3pF	240pF	3pF
Area of the amplifier	0.23mm^2	0.11mm^2	0.08mm^2 (off-chip C_{m1}&C_{m2})	0.14mm^2

Note: Slew rate and settling time were measured at unity-gain configuration with a 0.5V step input.

TABLE II
COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

	Gain (dB)	GBW (MHz)	SR (V/μs)	Power (mW@Vdd)	C_L (pF)	FOM_S ($\frac{MHz \cdot pF}{mW}$)	FOM_L ($\frac{V/\mu s \cdot pF}{mW}$)	Technology
NMC [3]	100	60	20	76@8	100	79	26	3GHz f_t BJT
MNMC [3]	100	100	35	76@8	100	132	46	3GHz f_t BJT
HMC [4]	120	2	5	0.450@1.5	10	44	111	0.8μm CMOS
		0.2	0.2	0.0225@1.5	10	89	89	
MHMC [4]	120	6	13	0.450@1.5	10	133	289	0.8μm CMOS
		0.6	0.7	0.0225@1.5	10	267	311	
NGCC [5]	100	1	5	1.4@2	20	14	71	2μm CMOS
ETC [6]	102	47	69	6.9@3	40	272	400	0.6μm CMOS
This work	>100	2.6	1.32	0.420@2	100	619	314	0.8μm CMOS
		1	0.36	0.426@2	1000	2347	845	

Since the bandwidth improvement by DFCFC with a 1000-pF load is 18 times, which is much greater than 4, the bandwidth provided by the amplifier is even wider than a single-stage amplifier under nearly the same power consumption.

To provide a clearer picture on the improvements by DFCFC, a comparison table for some published amplifiers using different compensation topologies is shown in Table II. Two figures of merit, FOM_S [6] and FOM_L, are defined for small-signal and large-signal performances.

$$\mathrm{FOM}_S = \frac{\mathrm{GBW} \cdot C_L}{\mathrm{power}} \tag{28}$$

$$\mathrm{FOM}_L = \frac{SR \cdot C_L}{\mathrm{power}}. \tag{29}$$

The units of FOM_S and FOM_L are MHz · pF/mW and V/μs · pF/mW, respectively. An average SR is used in the calculation. A larger figure of merit implies a better frequency compensation topology. From Table II, it is clear that DFCFC is better than all existing topologies, especially for the case of 1000-pF loading capacitance.

VI. CONCLUSION

In this paper, DFCFC which is targeted for amplifiers driving large capacitive loads has been presented. Theoretical analysis on frequency response, transient response, and power supply rejection ratio have been firstly discussed. Then, the experimental results have demonstrated that a DFCFC amplifier is significantly better than an NMC amplifier and a single-stage amplifier when driving large capacitive loads. Finally, comparison with other published topologies has been presented, and DFCFC shows better small-signal and large-signal performances.

ACKNOWLEDGMENT

The authors would like to thank Prof. W. T. Ng from the University of Toronto, Toronto, ON, Canada, for his valuable suggestions, and they also would like to thank S. F. Luk and J. Chan from HKUST for their technical assistance.

REFERENCES

[1] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Boston, MA: Kluwer, 1995.
[2] J. H. Huijsing, R. Hogervorst, and K.-J. de Landen, "Low-power low-voltage VLSI operational amplifier cells," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 841–852, Nov. 1995.
[3] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1709–1717, Dec. 1992.
[4] R. G. H. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6 MHz UGF," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1497–1504, Dec. 1994.
[5] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G_m-C compensation," *J. Solid-State Circuits*, vol. 32, pp. 2000–2011, Dec. 1997.
[6] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 339–347, Mar. 1999.
[7] R. J. Widlar, "Design techniques for monolithic operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-4, pp. 184–191, Aug. 1969.
[8] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Damping-factor-control frequency compensation technique for low-voltage low-power large capacitive load applications," in *ISSCC'99 Dig. Tech. Papers*, 1999, pp. 158–159.
[9] G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*, 1st ed. New York: McGraw-Hill, 1977.
[10] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifier," *IEEE J. Solid-State Circuits*, vol. SCS-9, pp. 347–352, Dec. 1974.
[11] C. T. Chuang, "Analysis of the settling behavior of an operational amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-17, pp. 74–80, Feb. 1982.
[12] R. Klinke, B. J. Hosticka, and H.-J. Pfleiderer, "A very-high-slew-rate CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 24, pp. 744–746, June 1989.
[13] B. W. Lee and B. J. Sheu, "A high slew-rate CMOS amplifier for analog signal processing," *IEEE J. Solid-State Circuits*, vol. 25, pp. 885–889, June 1990.
[14] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1984.
[15] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, 1st ed. New York: Wiley, 1986.
[16] J. W. Nilsson, *Electric Circuits*. Reading, MA: Addison-Wesley, 1993.
[17] H. C. Yang and D. J. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 326–334, Mar. 1990.

Ka Nang Leung received the B.Eng. and M.Phil. degrees from the Department of Electrical and Electronic Engineering at the Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, in 1996 and 1998, respectively. He is now working toward the Ph.D. degree in the same department.

During the B.S. studies, he joined Motorola, Hong Kong, to develop a PDA system as his final year project. His research interests include the development of novel frequency compensation techniques for low-voltage low-power multistage amplifiers, design of low-dropout regulators, and implementation of PWM dc–dc converters for telecommunication systems.

In 1996, he received a Best Teaching Assistant Award from the Department of Electrical and Electronic Engineering at the Hong Kong University of Science and Technology.

Philip K. T. Mok (S'86–M'95) received the B.A.Sc., M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1986, 1989, and 1995, respectively.

While at the University of Toronto, he was a Teaching Assistant in both the Electrical Engineering and Industrial Engineering Departments from 1986 to 1992. He taught courses in circuit theory, IC engineering, and engineering economics. He was also employed as a Research Assistant in the Integrated Circuit Laboratory at the University of Toronto from 1992 to 1994. He joined the Department of Electrical and Electronic Engineering, the Hong Kong University of Science and Technology, Hong Kong, in January 1995 as an Assistant Professor, where he is now also the Associate Director of the Computer Engineering Program. His research interests include semiconductor devices, processing technologies, and circuit designs for power electronics and telecommunications applications, with current emphasis on power integrated circuits and low-voltage analogue integrated circuits design.

Dr. Mok received the Henry G. Acres Medal, the W.S. Wilson Medal and Teaching Assistant Award from the University of Toronto, and the Teaching Excellence Appreciation Award from the Hong Kong University of Science and Technology.

Wing-Hung Ki (S'86–M'92) received the B.Sc. degree from the University of California, San Diego, the M.Sc. degree from the California Institute of Technology (Caltech), Pasadena, the Engineer degree and the Ph.D. degree from the University of California, Los Angeles, in 1984, 1985, 1990, and 1995, respectively, all in electrical engineering.

From 1985 to 1986, he was a Research Assistant in the Power Electronics Group at Caltech, helping to develop the software SCAMP (Switching Converter Analysis and Measurement Program). In 1992, he joined Micro Linear Corporation, San Jose, CA, as a Senior Design Engineer in the Department of Power and Battery Management, working on the design of power converter controllers. In 1995, he joined the Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong. His research interests are design and modeling of dimmable electronic ballasts, switch mode and switched-capacitor power converters, IC controller design for power converters, and fundamental research in analog integrated circuits.

Dr. Ki is the recipient of the 1997–1998 Asia Innovator Award of the Year granted by EDN Asia.

Johnny K. O. Sin (S'79–M'88–SM'96) was born in Hong Kong. He received the B.A.Sc. degree in 1981, the M.A.Sc. degree in 1983, and the Ph.D. degree in 1988, all in electrical engineering, from the University of Toronto, Toronto, ON, Camada.

Upon completion of the Ph.D. degree, he joined Philips Laboratories, New York, where he was a Senior Member of the Research Staff from 1988 to 1991. He joined the Department of Electrical and Electronic Engineering, the Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, in August 1991, as an assistant professor and was promoted to Associate Professor in 1996. He is one of the founding members of the Department and has been serving as the Director of the Undergraduate Studies program since the fall of 1998. He holds three U.S. patents and has four patents pending. He has published over 130 papers in technical journals and refereed conferences in the above areas. His research interests lie in the general area of microelectronic devices and fabrication technology and is currently working in the areas of power semiconductor devices and IC's, thin-film transistors, field emission devices, integrated sensors, Silicon-On-Insulator RF, and power devices and technology.

Dr. Sin is a member of the EDS Power Devices and IC's Technical Committee. He served as Technical Committee Member of the International Conference on Microelectronics Test Structures (ICMTS). He is also a Technical Committee Member of the International Symposium on Power Semiconductor Devices and IC's (ISPSD). Dr. Sin was made an Honorary Visiting Professor of the Dalian University of Technology, Dalian, R.O.C., in 1996. He is an Editor for IEEE ELECTRON DEVICE LETTERS. He was awarded the Teaching Excellence Appreciation Award by the School of Engineering, the Hong Kong University of Science and Technology, in 1998.