Self-biased cross-coupled low-cost fully-differential CMOS operational amplifier

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A low-cost fully-differential operational amplifier (opamp) using a novel self-biased cascode output stage and cross-coupled input stage is proposed. Fabricated in only an $84 \times 67\ \mu m^2$ area with TSMC 0.35 µm technology, and loaded with more than 100 pF capacitance, the opamp possesses 60 dB DC gain, 3 V/µs slew rate, 7.8 MHz unity-gain bandwidth, and −48 dB total harmonic distortion.

Introduction: To obtain such high-performance requirements as high driving ability, low output resistance, high-frequency bandwidth, and effective gain enhancement via gain boosting for a specific application, an amplifier usually comprises a large area of phase compensation and biasing circuits configured with large aspect-ratio transistors and large area passives. Therefore in a mixed-signal SoC the analogue part usually occupies a large portion of the die area. However the cost, i.e. as in [1–3], limit their range of application in various fields. In this Letter we propose an opamp with high quality of performance regarding issues such as DC gain, slew rate, settling time, total harmonic distortion (THD) and phase-margin, while the area cost of the opamp is much less than that of state-of-the-art opamps. The proposed opamp can, generically, have greater application to different fields, especially for mixed-signal SoCs.

Proposed circuit: The proposed high-quality small-area opamp uses class-AB architecture (see Fig. 1). Transistors M1 to M4 constitute the class-AB cross-coupled input stage. We use a gain stage [4, 5] comprising transistors M5 to M12 to enhance the current gain of the input stage rather than using level shifters with diode-connected load that consumes large quiescent current and dissipates much power. In the proposed circuit, the gate-to-source voltage differences of transistor pairs (M6, M7) and (M10, M11) are the differential inputs to the cross-coupled input stage constituted by M1 to M4. Therefore, the gate-to-source voltage (V_{gs}) differences of pairs (M1, M4) and (M2, M3) are increased to obtain high differential transconductances (g_m's) of the input stage and thus high voltage gain is obtained when these differential currents flow through the cascoded output stage constituted by transistors M13 to M20. To control the quiescent current and to reduce power dissipation, the biasing voltage at the gates of M5 and M9 are tuned to obtain small quiescent currents $I_{ds6} = I_{ds7}$ and $I_{ds10} = I_{ds11}$ [4]. For the output cascoded transistors, M13 and M17 dominate the total power consumption. With careful biasing and aspect-ratio tuning, the objective of low cost and high performance is achieved.

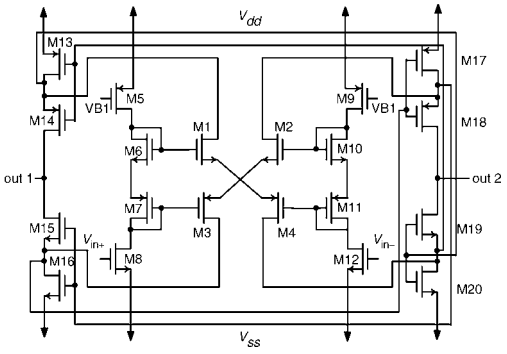

Fig. 1 *Proposed self-biased opamp circuit*

For the output resistance, seen from one output end is a cascoded configuration. Using the half circuit concept, the common source node of input devices M1(M2) and M4(M3) is virtual grounded. In this way, we have the output resistance as follows:

$$\begin{aligned} R_{\text{out}} = {} & \{[1 + (g_{m18} + g_{mb18})r_{o18}](r_{o17} // r_{o2}) + r_{o18}\} // \\ & \{[1 + (g_{m19} + g_{mb19})r_{o19}]r_{o20} + r_{o19}\} + \\ & \{[1 + (g_{m19} + g_{mb19})r_{o19}](r_{o20} // r_{o4}) + r_{o19}\} // \\ & \{[1 + (g_{m18} + g_{mb18})r_{o18}](r_{o17}) + r_{o18}\} \end{aligned} \quad (1)$$

For the total transconductance G_m, both the serial connections of M1, M4 and M2, M3 contribute to the output end out1. Since $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$, we have the total transonductance as

$$G_m = 2(g_{m1} + g_{m4}) \quad (2)$$

By the linear circuit lemma [6], the DC gain of the proposed opamp is

$$A_v = G_m \cdot R_{\text{out}} \quad (3)$$

We see that the transconductance is quadrupled if g_{m1} $(g_{m2}) \cong g_{m4}$ (g_{m3}). Consequently, the total voltage gain obtained in one end is about four times greater than the voltage gain of a cascode common source configuration. Therefore, an additional 12 dB is obtained from the proposed configuration compared with a cascode common source amplifier. To save the circuit area occupied by biasing circuits, we configure the opamp as in Fig. 1 so that internal nodes can provide gate voltages of cascode output stages (M13 to M20) at both ends, we call this 'self-biasing'. In this way, the linearity of the self-biasing circuit configuration is increased. Compared with [1] and [2], we find that even using small and fewer devices, the proposed opamp performs DC gain just as well and even better regarding some characteristics. In our circuit configuration, the channel widths of cross-coupled input devices M1 and M2 are 240 µm, and those of M3 and M4 are 150 µm. The gain stage for level shifting and outputs use transistors smaller than 60 µm in width. The other transistors are all smaller than 30 µm wide, the smallest being 4 µm wide. The total area of the fabricated chip is $84 \times 67\ \mu m^2$, which is less than one-tenth of the state-of-art opamp's. In other words, with small circuit area and small bias current, the proposed operational amplifier is very cost-effective.

Table 1: Comparisons of characteristics of proposed opamp with state-of-the-art opamps

	Proposed 1 external biasing	Proposed 2 internal biasing	[7]	[1]	[3]
Power supply	$V_{dd} = 3.3$ V $V_{ss} = 0$ V	$V_{dd} = 3.3$ V $V_{ss} = 0$ V	$V_{dd} = 1.5$ V, $V_{ss} = -1.5$ V	$V_{dd} = 1.5$ V, $V_{ss} = 0$ V	$V_{dd} = 5$ V $V_{ss} = 0$ V
Gain	66 dB	60 dB	>63 dB	65 dB	71 dB*
Bandwidth	11.5 MHz at 100 pF load	7.8 MHz at 100 pF load	8 MHz at 35 pF	300 kHz at 100 pF load	13 MHz at 20 pF load
Phase margin	50°	67°	N/A	80°	73°
THD	−40 dB at 1V_{p-p}1 kHz (100 pF load)	−48 dB at 1V_{p-p}1 kHz (100 pF load)	N/A	−48 dB at 1V_{p-p}1 kHz (100 pF load)	−59 dB at 1 kHz (10 pF load)
Slew rate at 20 pF	34.5 V/µs	28.1 V/µs	N/A	N/A	10 V/µs
At 35 pF	19.9 V/µs	16.3 V/µs	>10.2 V/µs	N/A	N/A
At 100 pF	7 V/µs	5.7 V/µs	N/A	0.4 V/µs	N/A
Settling time at 20 pF	427 ns at ±0.1%	458 ns at ±0.1%	N/A	N/A	N/A
At 35 pF	713 ns at ±0.1%	776 ns at ±0.1%	<220 ns at ±0.1%	N/A	N/A
At 100 pF	1.78 ns at ±0.1%	2.1 µs at ±0.1%	N/A	N/A	N/A
Die area µm^2	<100 × 100 (10000)	84 × 67 (5628)	280 × 218 (61040)	N/A	~300 × 180 (54000)
Process	0.35 µm	0.35 µm	1.2 µm	N/A	1 µm
Power	2.9 mW	2.2 mW	0.7 mW	0.2 mW	1 mW

Measurement results and comparisons: To measure the transient response of the proposed opamp, we configure the input and output connections with adequate passives outside the dual-in-line package of the test chip. In addition to the capacitances from the pad package, the probe, and the breadboard, the output of the proposed opamp has 20, 35 and 100 pF explicit capacitance loads, respectively. As summarised in Table 1, the experiments relating to the proposed opamp are classified into 'external' and 'self-biasing' categories. With 100 pF load, the external biased opamp has a DC gain of 66 dB and unity-gain frequency of 11.5 MHz. The measured performance of the self-biased opamp is close to that in [3] but it is much higher in slew rate. Using 3 V_{p-p} 2 kHz as input and with additive 20 pF capacitance, the measured slew rate is 16.5 V/µs, which outperforms the one in [3]. When 100 pF explicit capacitance is used as load in addition to the package and environmental parasitics, the driving ability shown in Fig. 2*c* is more than 3 V/µs and the proposed opamp still outperforms that of 0.4 V/µs in [1]. We further make comparison with [7], which utilises level shifters to save power consumption and to obtain high

current output. In addition to circuit area, the unity-gain bandwidth and slew rate of the proposed amplifier are superior to those in [7]. For the measurement results of the unit-gain configuration, given 1.5 V ± 1 $V_{p\text{-}p}$ 4 kHz sine wave as input for $V_{in}-$ and DC 1.5 V for $V_{in}+$, without additive capacitance load, the measured sine wave is as shown Fig. 2*a* and the FFT spectrum is as in Fig. 2*b*.

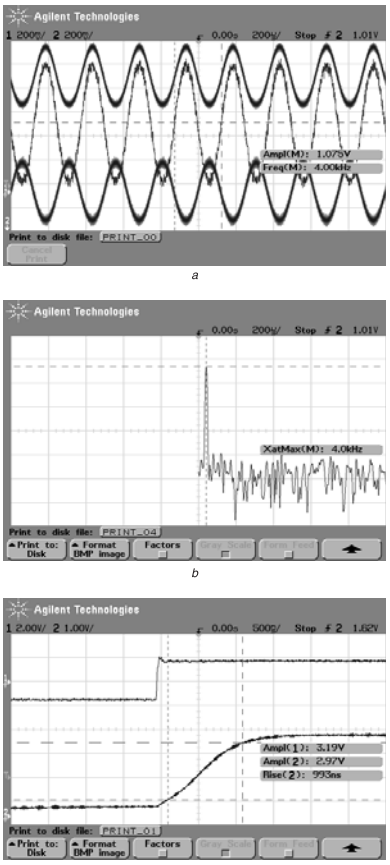

Fig. 2 *Measurement of unity gain configuration*

a When V_{in} input fed with 1.5 V ± 1 Vp-p sin wave and $V_{in}+$ fixed at DC 1.5 V Outputs measured at Vout − and Vout + pins are as upper and lower waveforms, respectively; the middle is the differential waveform of the two outputs, response being same as input

b FFT spectrum of differential output in *a*

c Given 3 $V_{p\text{-}p}$ 2 kHz square wave as input and with 100 pF capacitance load, measured slew rate is higher than 3 V/μs. Waveform names 'Ampl(1)', 'Ampl(2)', and 'Rise(2)' represent amplitude of input square wave, 10–90% voltage difference of rising edge, and rising time, respectively

Conclusion: In this Letter we propose a very cost-effective opamp which is much more applicable regarding modern mixed-signal SoCs. The proposed high-quality small area opamp uses symmetrically self-biased, class-AB, cross-coupled, and fully differential architecture to obtain very small circuit area and high transconductance advantages. The measured results show high DC gain and high driving ability whereas other performance features are not reduced. Using two layers of metal and occupying only 84 × 67 μm^2 silicon area, the proposed self-biased opamp achieves 60 dB DC gain, 3 V/μs slew rate, 7.8 MHz unity-gain bandwidth, −48 dB THD when 100 pF capacitance is as the load. Therefore, the cost-effectiveness of the proposed opamp is far superior compared with state-of-the-art opamps.

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