the transmitter system application including the DAC. The power consumption is 61 mW for a 40 MHz output signal at 200 MS/s from a 3 V supply. The measured differential nonlinearity and integral nonlinearity are ± 0.3 LSB and ± 0.7 LSB, respectively.

The dynamic performance is measured according to clock frequency in Fig. 4. A SFDR of more than 70 dBc has been achieved for low output frequency. An SFDR of 65 dBc is achieved for 40 MHz output signals at 200 MS/s which is the maximum usable data rate with the HP16700 pattern generator and the waveforms are shown in Fig. 5.

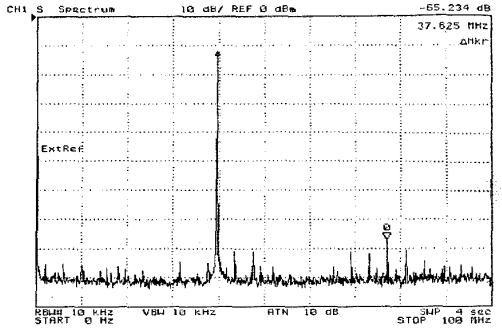

Fig. 5 *Output spectrum of 40MHz signal at 200MS/s*

9 September 2002
Electronics Letters Online No: 20021013
DOI: 10.1049/el:20021013

Seung-Chul Lee, Min-Hyung Cho and Hyun-Kyu Yoo (*Electronics and Telecommunications Research Institute, 161 Kajong-dong, Yusong-gu, Taejon, 305-350, Korea*)

E-mail: schlee@etri.re.kr

References

1 BOSCH, A.V., STEYEART, M., and SANSEN, W.: 'SFDR-bandwidth limitations for high-speed high-resolution current-steering CMOS D/A converters'. proc. IEEE Int. Conf. Electronics, Circuits and Systems (ICECS), Sept. 1999, pp. 1193–1196

2 BOSCH, A.V., BORREMANS, M., STEYAERT, M., and SANSEN, W.: 'A 10-bit 1-G Sample/s nyquist current-steering CMOS D/A converter', *IEEE J. Solid-State Circuits*, 2001, **36**, (3), pp. 315–324

3 LIN, C.H., and BULT, K.: 'A 10-b 500-MSample/s CMOS DAC in 0.6 mm^2', *IEEE J. Solid-State Circuits*, 1998, **33**, (12), pp. 1948–1958

4 SUN, Y.J., *et al.*: 'Current switch for a high speed DAC', U.S. Patent No. 6,295,012 Aug. 25, 1999

Continuous time common mode feedback technique for sub 1 V analogue circuits

M. Maymandi-Nejad and M. Sachdev

A continuous time common mode feedback technique for sub 1 V analogue circuits using the bulk PMOS dynamic threshold (BP-DTMOS) technique is presented. The proposed method is used in a 0.8 V folded cascode amplifier in 0.18 μm CMOS technology. The schematic and the post-layout simulation results show that this technique is effective in reducing common mode errors caused by process or environmental variations. It also improves the CMRR of the amplifier.

Introduction: Common mode feedback (CMFB) is very important in fully differential analogue circuits. In case of sub 1 V circuits, CMFB becomes more critical. In an analogue amplifier typically transistors are biased in the saturation region. However, in low voltage applications, the operating point of a transistor is not very far away from the linear region. This has two consequences. First, the performance of the circuit is degraded and hence it is difficult to obtain high gain and CMRR. Secondly, any small perturbation from the designed values can cause transistors to operate in the linear region. These perturbations can happen during the fabrication of the circuit or it can be due to environmental effects such as temperature variation. The effect of these perturbations and variations should be minimised by using suitable circuit techniques.

Fabrication variations can lead to common mode errors. A CMFB circuit can improve the CMRR of the amplifier, therefore reducing the effects of fabrication variations. However, the design of CMFB for low voltage circuits is nontrivial [1, 2]. Continuous time CMFB techniques [3, 4] and switched mode CMFB techniques [5, 6] have been reported to realise CMFB circuits. We propose a new continuous time CMFB technique which is suitable for sub 1 V applications.

Proposed technique: It is possible to use the body voltage of a PMOS transistor in standard CMOS technology to change the threshold voltage, and hence the current of the transistor. We have used this technique in the feedback loop of the CMFB circuit to control the bias current of the differential amplifier. Using this CMFB technique, the effect of any perturbation resulting to a common mode error at the output of the amplifier is reduced and the CMRR is increased.

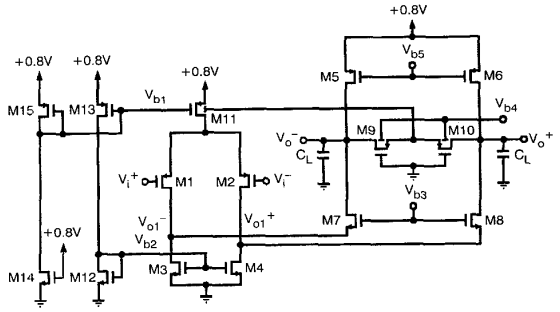

Fig. 1 *Folded cascode amplifier with proposed CMFB*

Fig. 1 shows a folded cascode differential pair with the proposed CMFB circuit. The amplifier is designed to operate with a single power supply voltage of 0.8 V. The input transistors (M1, M2) and the active load transistors (M3, M4) are biased in the saturation region. Therefore, it is necessary to adjust the current of the current source transistor M11 to twice that of the current passing through M3 or M4. Any kind of perturbation in V_{b1} or V_{b2} causes a larger voltage change at the output of the first and second stage. This will change the operating point of transistors and may cause some of them to operate in the linear region. The two transistors (M9, M10) connected between the two outputs act as two resistors and sample the output common mode voltage. The sources of these two transistors are used to change the body voltage of the current source transistor M11. This CMFB method tries to compensate any perturbation in V_{b1} or V_{b2} by changing the body voltage of M11. To make this point more clear, suppose that V_{b2} is increased from its designed value. This causes the current of the active load transistors (M3 and M4) to increase. Therefore, the output voltage of the first stage as well as the output voltage of the second stage is lowered. This lowers the body voltage of M11 which increases its current and causes the output voltage to be increased. This way the feedback compensates for perturbations of V_{b2}. Hence, the amplifier can tolerate larger parameter variations during fabrication.

It is worth noting that the equivalent static resistance of the feedback transistors (M9, M10) should be as large as possible because the CMFB circuit should have the least effect on the differential gain of the amplifier. Using a transistor as a large resistor is not a simple task in low voltage circuits because there is not enough voltage overhead to turn the transistor on. To overcome this problem we have biased the body of the PMOS transistors (M9, M10) at 0.4 V to lower the threshold voltage.

Simulation results: Fig. 2 shows the DC transfer characteristic of the folded cascode amplifier with and without CMFB. The dashed lines are for the ideal case (without any perturbation in W/L ratio of M12) and the solid lines are for the case of 5% perturbation in the W/L ratio of M12 which causes V_{b2} to be changed. As can be seen, when the CMFB is present the change in operating point is less which shows

the effectiveness of the proposed CMFB. Fig. 3 shows the percentage voltage change at the output of the first stage (V_{o1}^+, V_{o1}^-) due to a change in V_{b2} for two cases: when the CMFB is not active and when the CMFB is active. Clearly, the proposed CMFB is very effective in reducing the effect of some of the parameter variations during the fabrication process.

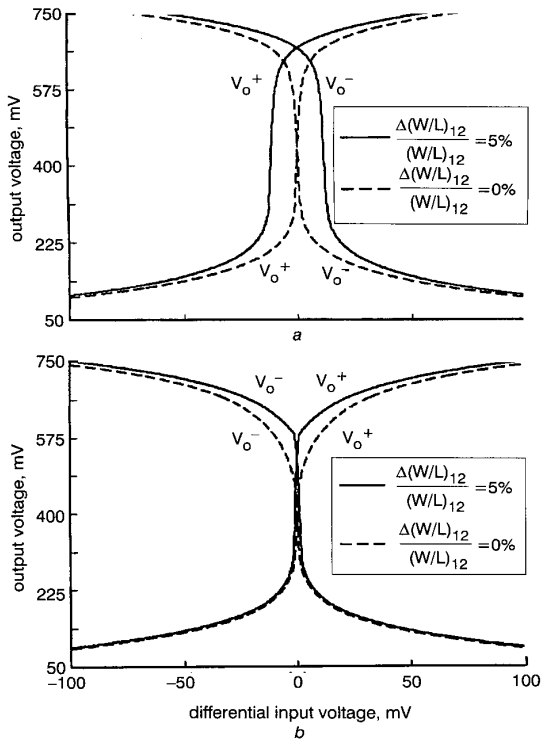

Fig. 2 *DC transfer characteristic of folded cascode amplifier*
a Without CMFB
b With CMFB

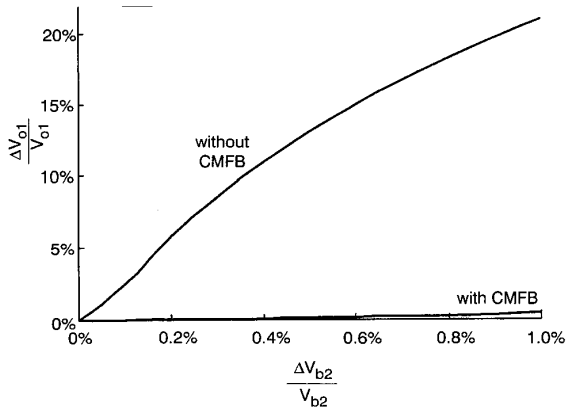

Fig. 3 *Percentage change in V_{o1} due to change in V_{b2}*

Table 1: Performance parameters of amplifier (V_{dd} = 0.8 V)

	Schematic simulation		Post-layout simulation	
	Without CMFB	With CMFB	Without CMFB	With CMFB
DC differential gain	52.05 dB	51.95 dB	52.19 dB	52.17 dB
CMRR	36.0 dB	47.4 dB	35.9 dB	51.8 dB
Unity gain BW (C_L = 1 pf)	40.44 MHz	40.44 MHz	43.16 MHz	41.53 MHz
Phase margin	69°	69°	71.9°	71.4°
Die area	–	–	3165 (μm)^2	3825 (μm)^2

In the case of low voltage amplifiers, obtaining a high CMRR is not very simple. For the above amplifier the output resistance of the current source M11 affects the CMRR. Using the proposed CMFB circuit the output resistance of current source M11 is increased and the CMRR is improved. Table 1 shows some of the performance parameters of the amplifier obtained from schematic and post-layout simulations. As can be seen, the proposed CMFB circuit has increased the CMRR of the amplifier while it has a negligible effect on the differential mode parameters.

Conclusion: A 0.8 V fully differential folded cascode amplifier with a new continuous time common mode feedback has been presented. The circuit has been simulated and laid out using 0.18 μm CMOS technology. The proposed CMFB technique is effective for reducing parameter perturbations during fabrication. It also improves the CMRR of the amplifier. This technique is especially suitable for low-voltage applications where it is not possible to use several transistors in series between the supply rails and there is not enough voltage overhead to tolerate parameter variations. Even though the proposed technique is used in the folded cascode amplifier, it can be used for other kinds of differential amplifiers as well.

10 September 2002
Electronics Letters Online No: 20021010
DOI: 10.1049/el:20021010

M. Maymandi-Nejad and M. Sachdev (*Dept. of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, N2L 3G1, Canada*)

E-mail: maymandi@vlsi.uwaterloo.ca

References

1 MALOBERTI, F., FRANCESONL, F., MALCOVATI, P., and NYS, O.J.A.P.: 'Design considerations on low-voltage low-power data converters', *IEEE Trans. Circuits Syst.-I: Fundamental Theory and Applications*, 1995, **42**, (11)
2 PELUSO, V., VANCORELAND, P., MARQUES, A.M., STEYAERT, M.S.J., and SANSEN, W.: 'A 900-mV low-power delta-sigma A/D converter with 77-dB dynamic range', *IEEE J. Solid-State Circuits*, 1998, **33**, (12), pp. 1887–1897
3 WHATLY, R.A.: 'Fully differential operational amplifiers with DC common mode feedback', US Patent No. 4573020, Feb. 1986
4 DUQUE-CARILLO, J.F.: 'Control of common mode component in CMOS continuous time fully differential signal processing', *Analog Integr. Circuits Signal Process. An International Journal*, (Kluwer Academic Publisher, Sept. 1993)
5 CALLIAS, F., SALCHLI, F.H., and GIRARD, D.: 'A set of four IC's in CMOS technology for a programmable hearing aid', *IEEE J. Solid-State Circuits*, 1989, **20**, pp. 301–302
6 CASTELLO, R., and GRAY, P.R.: 'A high performance micropower switched capacitor filter', *IEEE J. Solid-State Circuits*, 1985, **SC-20**, pp. 1122–1132

Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps

J. Ramirez-Angulo and M. Holmes

A simple modification to a one-stage op-amp for operation as a class AB amplifier leads to significant slew rate and bandwidth enhancement with essentially equal silicon area and static power dissipation requirements. Experimental results of a prototype in 0.5 μm CMOS verify SR and bandwidth enhancement factors of almost one order of magnitude.

Introduction: It is well known that the maximum gain-bandwidth (GB) product of a one stage operational amplifier (Fig. 1*a*) is limited by the internal pole(s) of the amplifier, mainly, by those associated to the internal mirror (nodes A and B in Fig. 1*a*). Typically the condition $GB < 2\omega_{PA}$ is used as a practical design guideline in order to provide enough phase margin [1, 2]. Wireless and other battery powered systems require high GB values, high slew rates (SR), and at the same