Analysis of Multistage Amplifier–Frequency Compensation

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***Abstract*—Frequency-compensation techniques of single-, two- and three-stage amplifiers based on Miller pole splitting and pole–zero cancellation are reanalyzed. The assumptions made, transfer functions, stability criteria, bandwidths, and important design issues of most of the reported topologies are included. Several proposed methods to improve the published topologies are given. In addition, simulations and experimental results are provided to verify the analysis and to prove the effectiveness of the proposed methods.**

***Index Terms*—Damping-factor-control frequency compensation, multipath nested Miller compensation, multipath zero cancellation, multistage amplifier, nested Gm-C compensation, nested Miller compensation, simple Miller compensation.**

I. Introduction

MULTISTAGE amplifiers are urgently needed with the advance in technologies, due to the fact that single-stage cascode amplifier is no longer suitable in low-voltage designs. Moreover, short-channel effect of the sub-micron CMOS transistor causes output-impedance degradation and hence gain of an amplifier is reduced dramatically. Therefore, many frequency-compensation topologies have been reported to stabilize the multistage amplifiers [1]–[26]. Most of these topologies are based on pole splitting and pole–zero cancellation using capacitor and resistor. Both analytical and experimental works have been given to prove the effectiveness of these topologies, especially on two-stage Miller compensated amplifiers. However, the discussions in some topologies are focused only on the stability criteria, but detailed design information such as some important assumptions are missing. As a result, if the provided stability criteria cannot stabilize the amplifier successfully, circuit designers usually choose the parameters of the compensation network by trial and error and thus optimum compensation cannot be achieved.

In fact, there are not many discussions on the comparison of the existing compensation topologies. Therefore, the differences as well as the pros and cons of the topologies should be investigated in detail. This greatly helps the designers in choosing a suitable compensation technique for a particular design condition such as low-power design, variable output capacitance or variable output current.

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Moreover, practical considerations on the compensation techniques of N-stage amplifiers are questionable since any extra stage consumes more power, requires more complicated circuit structure and may reduce the bandwidth dramatically. In fact, the three-stage amplifier provides sufficient dc gain for most applications, and, therefore, frequency-compensation techniques for amplifiers with up to three stages are sufficient and worthwhile to develop.

Regarding these issues, this paper firstly gives a review on single-stage amplifier in Section III and then addresses some published topologies for two- and three-stage amplifiers from Sections IV to VIII, including simple Miller compensation (SMC), multipath zero cancellation (MZC), nested Miller compensation (NMC), multipath NMC (MNMC), nested Gm-C compensation (NGCC), and damping-factor-control frequency-compensation (DFCFC). Especially, single-end amplifiers are used to discuss the compensation topologies. The assumptions made, transfer functions, stability criteria, and design considerations are given. Several proposed methods to eliminate some design problems are also included with the support of simulations and experimental results. A summary, a comparison and some important issues of the studied topologies are given in Section IX. Finally, a discussion on the robustness of the studied compensation techniques is included.

II. Notations Declaration and Assumptions

In this section, the general notations used in this paper are firstly defined, then the common assumptions in all topologies are stated.

1) Notations Declaration: g_{mi}, R_{oi}, and C_{pi} are defined as the transconductance, output resistance and lumped output parasitic capacitance of the ith gain stage, respectively. Particularly, g_{mL} is the output stage transconductance, R_L is the loading resistance and C_L is the loading capacitance. The compensation capacitor is denoted by C_{mi}. The voltage-gain transfer function is defined as $A_v(s) = V_{\rm out}(s)/V_{\rm in}(s)$ where $V_{\rm in}$ and $V_{\rm out}$ are the input and output signal voltage, respectively. Moreover, GBW stands for the gain-bandwidth product and PM for the phase margin.

2) Assumptions: Due to the complicated compensation structures, the transfer functions are generally very complicated and cannot be analyzed easily. In this case, analysis with numerical method using computers is feasible. However, this loses the insight on some critical parameters to improve the frequency response. Therefore, some assumptions are made here to simplify the transfer functions without losing the

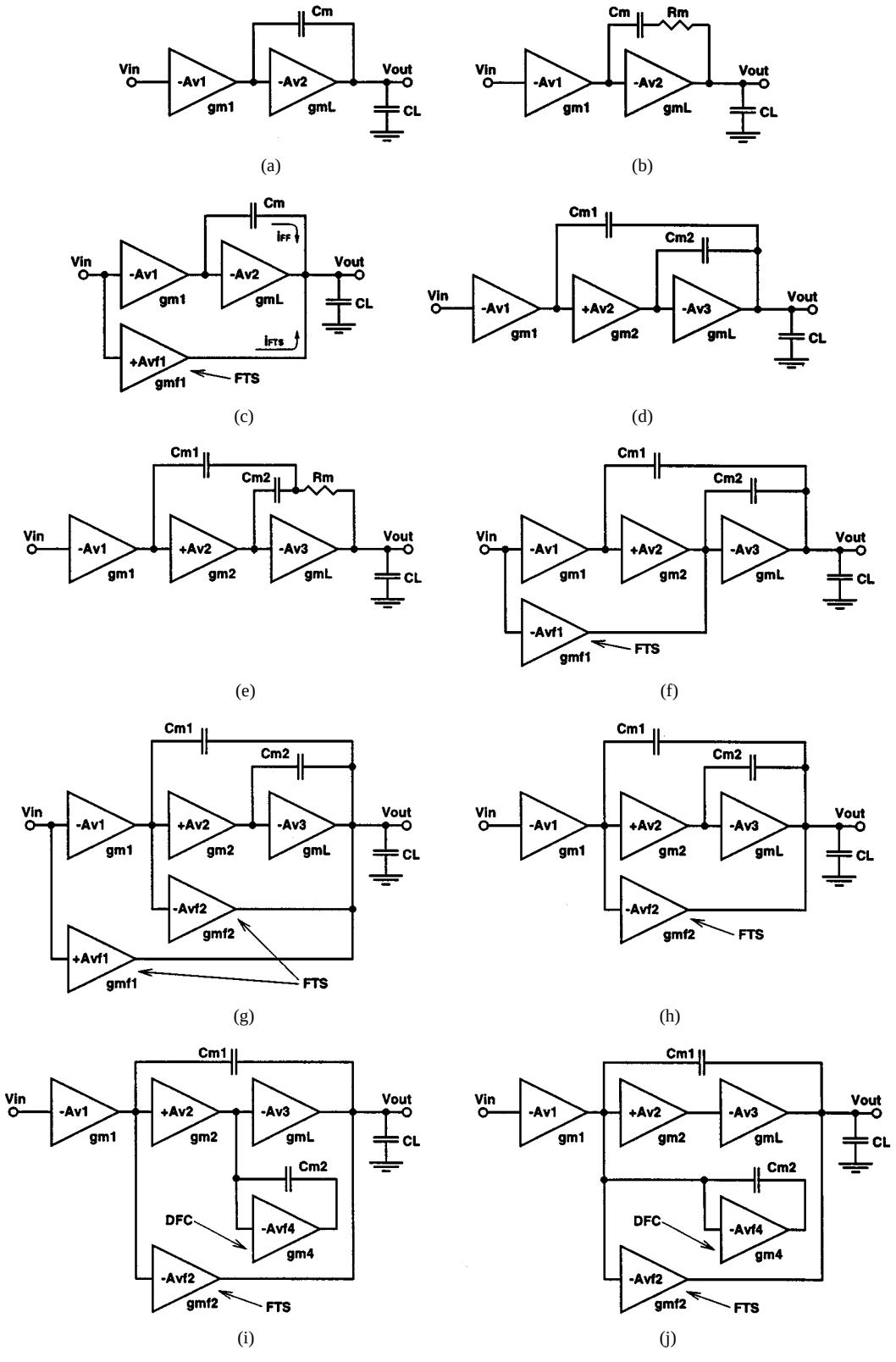

Fig. 1. Studied and proposed frequency-compensation topologies. (a) SMC. (b) SMCNR. (c) MZC. (d) NMC. (e) NMCNR. (f) MNMC. (g) NGCC. (h) NMCF. (i) DFCFC1. (j) DFCFC2.

accuracy. In this paper, there are three common assumptions made for all studied and proposed topologies.

1) The gains of all stages are much greater than one (i.e., $g_{mi}R_{oi} \gg 1$ and $g_{mL}R_L \gg 1$).
2) The loading and compensation capacitances are much larger than the lumped output parasitic capacitances of each stage (i.e., C_L and $C_m \gg C_p$).
3) Interstage coupling capacitances are negligible.

Assumption 1 holds true in amplifier designs for most amplifiers except those driving small load resistance. If this assumption cannot be satisfied, numerical analysis using computers is required. Moreover, the parasitic capacitances of the tiny-geometry transistors in advanced technologies are small and this validates assumptions 2) and 3).

III. Review on Single-Stage Amplifier

The single-stage amplifier is said to have excellent frequency response and is widely used in many commercial products. In fact, the advantages can be illustrated by its transfer function

$$A_{v_{\text{single}}}(s) = \frac{g_{mL}R_L}{1+sC_LR_L}. \tag{1}$$

From (1), the amplifier has only one left-half-plane (LHP) pole ($p_{-3\text{ dB}} = 1/C_LR_L$) and no zero, so the amplifier is always stable. In fact, C_L itself is the compensation capacitor of the amplifier. The GBW is obtained from (1) as the following:

$$\text{GBW} = \frac{g_{mL}}{C_L} \tag{2}$$

and the PM is 90° due to the single pole, assuming that GBW $>$ $10p_{-3\text{ dB}}$ (i.e., $g_{mL}R_L > 10V/V$). From (2), the GBW can be increased by increasing the transconductance of the input stage and decreasing the loading capacitance. Nevertheless, there are many parasitic poles and zeros (denoted as p_{par} and z_{par}) which may affect the stability of the amplifier. The locations of p_{par} and z_{par} highly depend on the size and bias current of the transistors in the signal path. As a rule of thumb, the GBW should be set at most at half of the lowest frequency of p_{par} and z_{par}. In other words, there is a maximum g_{mL} and minimum C_L for a single-stage amplifier such that GBW $< 1/2\min(p_{\text{par}}, z_{\text{par}})$. Therefore, a higher bias current and smaller size for all transistors in the signal path are required to locate p_{par} and z_{par} to higher frequencies in order to extend the bandwidth.

The dc gain is small, only $g_{mL}R_L$, so many advanced gain-boosting techniques have been reported [26] to increase R_L. These techniques not only require a large supply voltage, a more complicated circuit structure, and additional power, but also reduce the output swing. However, the GBW is not affected since it is independent of R_L.

IV. SMC

Although single-stage cascode amplifier is excellent on both dc gain and frequency response, cascode configuration is no longer suitable in low-voltage design. To overcome this problem, two-stage SMC amplifier is commonly used [1]–[3]. The structure is shown in Fig. 1(a) and it is important to note that the gain of the output stage is negative so that the capacitive feedback by C_m is negative. With the stated assumptions, the transfer function of a SMC amplifier is given by

$$A_{v_{(\text{SMC})}}(s) = \frac{g_{m1}g_{mL}R_{o1}R_L(1-s\frac{C_m}{g_{mL}})}{(1+sC_mg_{mL}R_{o1}R_L)(1+s\frac{C_L}{g_{mL}})}. \tag{3}$$

There are two LHP poles and one right-half-plane (RHP) zero. The dominant pole is $p_{-3\text{ dB}} = 1/C_mg_{mL}R_{o1}R_L$, the non-dominant pole is $p_2 = g_{mL}/C_L$ and the RHP zero is $z_1 = -g_{mL}/C_m$. To ensure the closed-loop stability of a SMC amplifier, both p_2 and z_1 should be placed at higher frequencies than the unity-gain frequency. This can be achieved by using a large C_m to move $p_{-3\text{ dB}}$ to a lower frequency. However, the GBW $= g_{m1}/C_m$ is reduced simultaneously, so it is suggested not to overcompensate the amplifier. Thus, GBW is generally set to be half of p_2 to obtain a good PM (i.e., $g_{mL}/C_L = 2g_{m1}/C_m$) and the dimension condition of C_m is therefore obtained as the following:

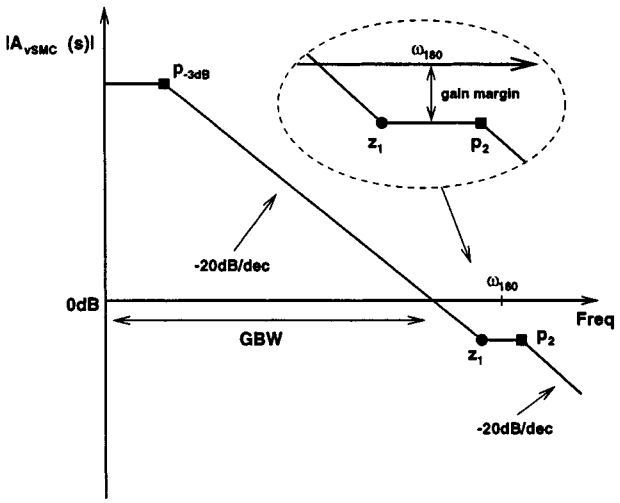

Fig. 2. Frequency response of a two-stage SMC amplifier (z_1 locates before p_2).

$$C_m = 2\left(\frac{g_{m1}}{g_{mL}}\right)C_L. \tag{4}$$

This dimension condition of C_m is based on the assumption that p_2 locates at a lower frequency than z_1. It is shown in (4) that C_m is large and comparable to C_L if g_{m1}/g_{mL} is large. In this case, z_1 locates at a frequency close to or before p_2. The frequency response of the SMC amplifier with z_1 locating before p_2 are shown in Fig. 2. If z_1 locates before p_2, the gain margin is small and the amplifier may be unstable under the effect of the parasitic poles and zeros. Therefore, z_1 should be located after p_2 in order to obtain a good gain margin.

From (3) and (4), the GBW is given by

$$\text{GBW} = \frac{g_{m1}}{C_m} = \frac{1}{2}\left(\frac{g_{mL}}{C_L}\right) \tag{5}$$

which is half of that of a single-stage amplifier. From (4) and (5), it can be realized that the GBW of a SMC amplifier cannot be increased by increasing g_{m1}. It is due to the fact that the required C_m is increased proportionally with g_{m1}, so g_{m1}/C_m is always a constant. Instead, the GBW can be enhanced by increasing the output transconductance and decreasing the loading capacitance. The PM is evaluated by the following expression:

$$\begin{aligned}\text{PM} =& 180^\circ - \tan^{-1}\left(\frac{\text{GBW}}{p_{-3\text{ dB}}}\right) - \tan^{-1}\left(\frac{\text{GBW}}{p_2}\right) \\ & - \tan^{-1}\left(\frac{\text{GBW}}{|z_1|}\right) \approx \quad 63^\circ - \tan^{-1}\left(\frac{g_{m1}}{g_{mL}}\right).\end{aligned} \tag{6}$$

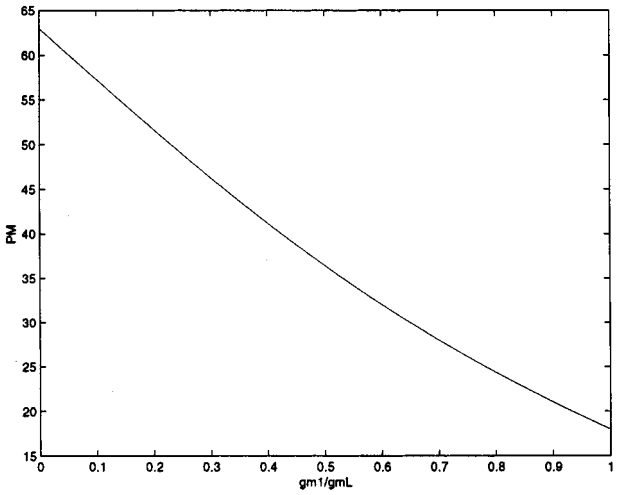

Fig. 3. PM versus g_{m1}/g_{mL} of a SMC amplifier.

From (6) and Fig. 3, the PM of a SMC amplifier strongly depends on the g_{m1} to g_{mL} ratio and this, in fact, shows the RHP zero effect on the PM. Physically, the presence of the RHP zero is due to the feedforward small-signal current flowing through the compensation capacitor to the output [1]–[11]. If g_{mL} is large, the small-signal output current is larger than the feedforward current and the effect of the RHP zero appears only at very high frequencies. Thus, a small g_{m1}/g_{mL} gives a better PM, so a smaller g_{m1} is preferable. However, g_{m1} is limited by the bias current and size of the input differential pair. To have a good slew rate, the bias current cannot be small. In addition, to have a small offset voltage, the size of input differential pair cannot be too small. Emitter/source degeneration technique is also not feasible to reduce g_{m1} since it reduces the limited input common-mode range in low-voltage design. Therefore, a small g_{m1} cannot be obtained easily.

From the previous analysis, it is known that the RHP zero degrades the stability significantly. There are many methods to eliminate the RHP zero and improve the bandwidth. The methods involve using voltage buffer [4]–[6] and current buffer [7], [8], a nulling resistor [2], [3], [9]–[11], and MZC technique [12]. In this paper, the techniques to be discussed are: 1) SMC using nulling resistor (SMCNR) and 2) SMC using MZC.

A. SMCNR

The presence of the RHP zero is due to the feedforward small-signal current. One method for reducing the feedforward current and thus eliminating the RHP zero is to increase the impedance of the capacitive path. This can be done by inserting a resistor, called nulling resistor, in series with the compensation capacitor, as shown in Fig. 1(b). Most published analyses only focus on the effect of the nulling resistor to the position of the zero but not to the positions of the poles. In fact, when the nulling resistor is increased to infinity, the compensation network is open-circuit and no pole splitting takes place. Thus, the target of this section is to investigate the limit of the nulling resistor.

The transfer function of the SMNCR (R_m), is as shown as (7) at the bottom of the page. Now, the dominant pole, nondominant pole and zero are given by $p_{-3\text{ dB}}$=$1/C_m(R_m$+$g_{mL}R_{o1}R_L)$, $p_2 = (R_m + g_{mL}R_{o1}R_L)/C_L(R_{o1} + R_m)R_L$ and $z_1 = 1/C_m\,(R_m - 1/g_{mL})$, respectively. It is well-known that when $R_m = 1/g_{mL}$, z_1 is completely eliminated. In addition, as $R_m = 1/g_{mL}$ is generally much smaller than R_{o1}, $p_{-3\text{ dB}}$ and p_2 are approximately the same as in SMC without the nulling resistor. Therefore, the value of C_m is determined by (4). The GBW is also given by (5) and the PM is about 63° due to the absence of the RHP zero.

However, many designers prefer to use a nulling resistor with value larger than $1/g_{mL}$ since an accurate value of R_m is difficult to obtain and a LHP zero, which increases the PM, is created. In fact, from (7), when R_m is increased, the positions of the poles will be changed accordingly and moved to lower frequencies. The pole-splitting effect is destroyed if R_m is too large. In other words, there is a limit of R_m and suggested to be $1/g_{mL} \le R_m < (1/10)R_{o1}$. This upper limit is based on the compromise that R_m in both the expressions of $p_{-3\text{ dB}}$ and p_2 are negligible.

B. SMC Using MZC

In many high-performance two-stage amplifiers driving resistive load, a Class-AB output stage is used to obtain a good control of the quiescent-to-maximum output current ratio. Since the output current changes during the operation, g_{mL} is not a constant and a precise cancellation of the RHP zero by a fixed R_m is not possible. The amplifier may not be stable at certain output current level, so SMC using MZC was introduced [12]. MZC is a simple but effective method to eliminate the RHP zero. It has an additional advantage that the positions of the poles are not affected by the additional circuitry. As shown in Fig. 1(c), a feedforward transconductance stage (FTS) is added and it produces an out-of-phase small-signal current ($i_{\text{FTS}} = -g_{mf1}V_{\text{in}}$) to cancel the feedforward small-signal current ($i_{\text{FF}} = g_{m1}V_{\text{in}}$) which passes through C_m at high frequencies. Theoretically, when $g_{mf1} = g_{m1}$, i_{FF} is completely canceled by i_{FTS}. This can be shown by the transfer function

$$A_{v_{(MZC)}}(s) = \frac{g_{m1}g_{mL}R_{o1}R_L\left[1 + s\frac{C_m(g_{mf1}-g_{m1})}{g_{m1}g_{mL}}\right]}{(1 + sC_mg_{mL}R_{o1}R_L)\left(1 + s\frac{C_L}{g_{mL}}\right)}. \quad (8)$$

From the transfer function, the cancellation of $z_1 = g_{m1}g_{mL}/C_m(g_{mf1} - g_{m1})$ is achieved, as stated before, by setting $g_{mf1} = g_{m1}$, which is independent of g_{mL}.

$$A_{v_{(\text{SMCNR})}}(s) = \frac{g_{m1}g_{mL}R_{o1}R_L\left[1 + sC_m\left(R_m - \frac{1}{g_{mL}}\right)\right]}{[1 + sC_m(R_m + g_{mL}R_{o1}R_L)]\left[1 + s\frac{C_L(R_{o1}+R_m)R_L}{R_m+g_{mL}R_{o1}R_L}\right]} \quad (7)$$

Moreover, since MZC does not change the positions of the poles, the same dimension condition of C_m stated in (4) is used. The GBW is also given by (5) and the PM is increased to about 63° which is obtained by neglecting the RHP zero phase shifting term in (6). Besides, when the output current is increased, g_{mL} is increased accordingly. The nondominant pole ($p_2 = g_{mL}/C_L$) will move to a higher frequency and a larger PM is obtained. Thus, this compensation topology can stabilize the amplifier within the quiescent to maximum loading current range.

In some applications, C_L is a constant and a larger g_{mf1} can be used to create a LHP zero to cancel p_2 [12]. Defining $r_g = g_{mf1}/g_{m1}$ where $r_g > 1$, the expression of the zero is re-written as $z_1 = g_{mL}/(r_g - 1)C_m$. The dimension of C_m is obtained by setting $z_1 = p_2$ and is therefore given by $C_m = C_L/(r_g - 1)$. The GBW is given by GBW $= g_{m1}/C_m$ and the PM is about 90° due to the effective one-pole system. In this case, the GBW is no longer dependent on g_{mL} and C_L but is dependent on g_{m1} and C_{m1}. Apparently, the GBW can be increased to infinity by decreasing C_m to zero. However, the C_m must be much larger than C_{p1} to validate the assumptions on deriving (8), so the following condition is required as a compromise:

$$C_m = \frac{C_L}{r_g - 1} \geq 10C_{p1}. \tag{9}$$

Since the performances of the SMC amplifier using MZC can be enhanced by a larger g_{mf1} so that C_m is small and the GBW is large, the tradeoffs between the extra power consumption on the FTS and the GBW should be considered carefully. For IC implementation, r_g can be obtained accurately by transistor layout and bias current in ratio. This ensures a closely-compressed pole–zero doublet.

The implementation of the FTS can be done by an additional input differential stage (MF1 and MF2) as shown in Fig. 4 [12]. However, the circuit becomes more complicated if rail-to-rail constant-Gm input stage is required since the FTS needs to be rail-to-rail and constant-Gm simultaneously. Moreover, the FTS introduces additional offset voltage and input capacitance.

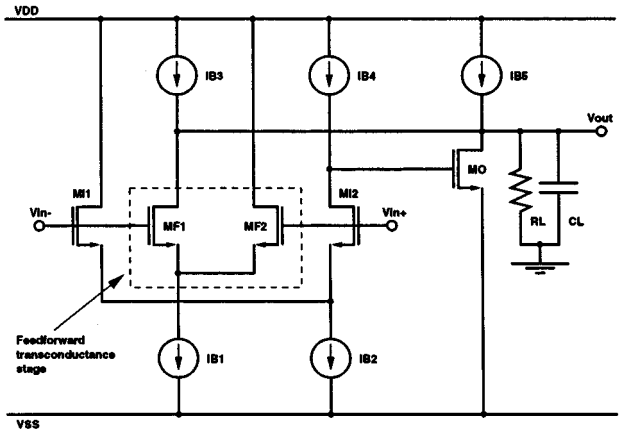

Fig. 4. Example circuit to implement MZC.

V. NMC

The voltage gain can be further increased by additional gain stages. In this case, NMC, which is an extended version of SMC, is used to achieve the stability [12]–[18], [26]. Theoretically, NMC can be extended to infinite number of stages. Nevertheless, no more than four stages have been reported because of the reduction of bandwidth [12], [16], [26], impractical large dc gain and higher power consumption required. Thus, only three-stage NMC amplifier is discussed in this section. The NMC structure is shown in Fig. 1(d) and the transfer function of a three-stage NMC amplifier is given in (10) at the bottom of the page. Besides, with an additional condition that $g_{mL} \gg g_{m1}$ and g_{m2}, the transfer function is rewritten as (11), shown at the bottom of the page. The dominant pole is $p_{-3\text{ dB}} = 1/C_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$, and the two nondominant poles (p_2 and p_3) are governed by the second-order function in the denominator of (11). The arrangement of the two nondominant poles leads to two stability methods: 1) separate-pole approach [18] and 2) complex-pole approach [12], [16], and [26].

For separate-pole approach, the poles can be separated by the condition, GBW $\leq (1/2)p_2 \leq (1/4)p_3$ and this is achieved by

$$\frac{g_{m1}}{C_{m1}} \leq \frac{1}{2}\frac{g_{m2}}{C_{m2}} \leq \frac{1}{4}\frac{g_{mL}}{C_L}. \tag{12}$$

$$A_{v_{\text{NMC}}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1 - s\frac{C_{m2}}{g_{mL}} - s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{C_{m2}(g_{mL} - g_{m2})}{g_{m2}g_{mL}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{10}$$

$$\begin{aligned} A_{v_{\text{NMC}}}(s) &= \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \\ &\approx \frac{1}{s\frac{C_{m1}}{g_{m1}}\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \end{aligned} \tag{11}$$

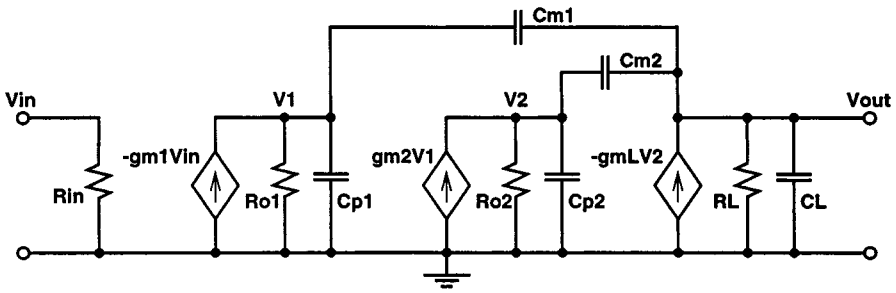

Fig. 5. Equivalent small-signal model of three-stage NMC.

From the above equation, GBW $= g_{m1}/C_{m1} \leq 1/4(g_{mL}/C_L)$ and PM $\geq 90° - \tan^{-1}(1/2) - \tan^{-1}(1/4) = 50°$. Assuming g_{m1}, g_{m2} and g_{mL} are fixed for a given power consumption, large C_{m1} and C_{m2} are required. This increases the PM but it reduces the GBW and also increases the capacitor values and the required chip area simultaneously.

For the complex-pole approach, the NMC amplifier in unity-feedback configuration should have the third-order Butterworth frequency response. Let $H_{\rm NMC}(s)$ be the closed-loop transfer function and ω_o be the cut-off frequency, the standard form with the third-order Butterworth coefficients [27] is given by

$$H_{\rm NMC}(s) = \frac{A_{v_{\rm NMC}}(s)}{1 + A_{v_{\rm NMC}}(s)} = \frac{1}{1 + s\left(\frac{2}{\omega_o}\right) + s^2\left(\frac{2}{{\omega_o}^2}\right) + s^3\left(\frac{1}{{\omega_o}^3}\right)}. \quad (13)$$

To obtain this response, $A_{v_{\rm NMC}}(s)$ should be in the following format:

$$A_{v_{\rm NMC}}(s) = \frac{1}{s\frac{2}{\omega_o}\left[1 + s\left(\frac{1}{\omega_o}\right) + s^2\left(\frac{1}{2{\omega_o}^2}\right)\right]}. \quad (14)$$

Comparing the coefficients of (11) with (14), the following dimension conditions of C_{m1} and C_{m2} are obtained:

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right) C_L \quad (15)$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right) C_L. \quad (16)$$

With (15) and (16), the open-loop nondominant complex poles are $p_{2,3} = (g_{mL}/2C_L) \pm j(g_{mL}/2C_L)$ (or $|p_{2,3}| = (g_{mL}/\sqrt{2}C_L)$) and the damping factor of the complex pole is $1/\sqrt{2}$ (i.e., $\zeta = 1/\sqrt{2}$) which implies no frequency peak in the magnitude Bode plot. The GBW is then given by

$$\text{GBW} = \frac{g_{m1}}{C_{m1}} = \frac{1}{4}\left(\frac{g_{mL}}{C_L}\right) \quad (17)$$

which is one-fourth the bandwidth of a single-stage amplifier. This shows the bandwidth reduction effect of nesting compensation. Similar to SMC, the GBW can be improved by a larger g_{mL} and a smaller C_L but not by a larger g_{m1} and a smaller C_{m1}. The PM under the effect of a complex pole [28] is given by

$$\text{PM} = 180° - \tan^{-1}\left(\frac{\text{GBW}}{p_{-3\text{ dB}}}\right) - \tan^{-1}\left[\frac{2\zeta\left(\frac{\text{GBW}}{|p_{2,3}|}\right)}{1 - \left(\frac{\text{GBW}}{|p_{2,3}|}\right)^2}\right] \approx 60°. \quad (18)$$

Comparing the required compensation capacitors, the GBW and PM under the same power consumption (i.e., same g_{m1}, g_{m2} and g_{mL}) of the two approaches, it is concluded that the complex-pole approach is better. Moreover, from (15) and (16), smaller C_{m1} and C_{m2} are needed when $g_{mL} \gg g_{m1}$ and g_{m2}. This validates the previous assumption on neglecting the zeros since the coefficients of the function of zero in (10) are small and the zeros locate at high frequencies. From another point of view, the required C_{m1} and C_{m2} are small, so the feedforward small-signal current can pass to the output only at very high frequencies. In addition, the output small-signal current is much larger than the feedforward current as $g_{mL} \gg g_{m1}$ and g_{m2}. Thus, the zeros give negligible effect to the stability. If the separate-pole approach is applied, the stability is doubtful since larger compensation capacitors are required and this generates zeros close to the unity-gain frequency of the amplifier.

To further prove that $g_{mL} \gg g_{m1}$ and g_{m2} is necessary in NMC, a HSPICE simulation using the equivalent small-signal model of NMC, which is shown in Fig. 5, is performed. The circuit parameters are $g_{m1} = 100\mu$A/V, $g_{m2} = 50$ μA/V, $g_{mL} =$ 1 m A/V ($g_{mL} \gg g_{m1}$ and g_{m2} is satisfied) and $C_L = 10$ pF. C_{m1} and C_{m2}, which is set according to (15) and (16), are 4 pF and 1 pF, respectively. The simulation result is shown in Fig. 6 by the solid line. A GBW of 4.2 MHz and a PM of 58° are obtained. Increasing g_{m1} from 100 μA/V to 1 mA/V (g_{mL} is not much larger than g_{m1}), the required C_{m1} is changed from 4 pF to 40 pF, according to (15). The frequency response is shown by the dotted line in Fig. 6. A RHP zero appears before the unity-gain frequency and causes the magnitude plot to curve upwards. The PM is degraded to 30°. In another case, g_{m2} is changed from 50 μA/V to 1 mA/V (g_{mL} is not much larger than g_{m2}) and C_{m2} is changed from 1 pF to 20 pF according to (16). As shown by the dashed line in Fig. 6, a frequency peak, due to small damping factor of the complex pole, appears and makes the amplifier unstable. The phenomenon can be explained from (10). When g_{mL} is not much larger than g_{m2}, the term $(g_{mL} - g_{m2})$ of the second-order function in the denominator is small and this causes the complex poles to have a small

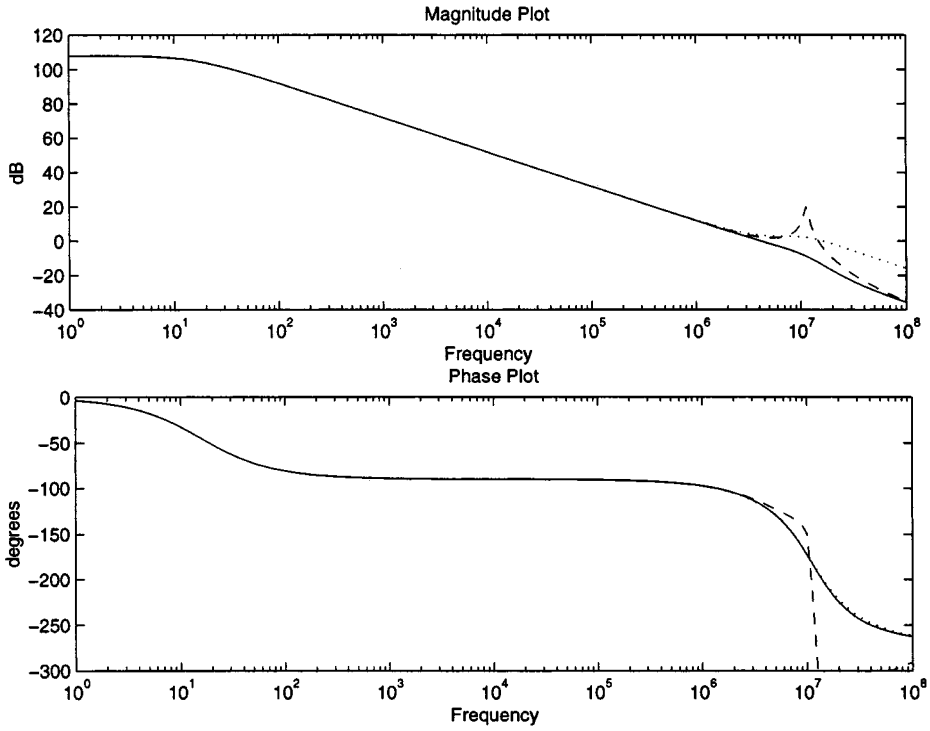

Fig. 6. HSPICE simulation of NMC (solid: $g_{mL} \gg g_{m1}$ and g_{m2}; dotted: g_{mL} is not much larger than g_{m1}; dash: g_{mL} is not much larger than g_{m2}).

damping factor. If $g_{mL} < g_{m2}$, RHP poles appear and cause the amplifier to be unstable in any close-loop operation.

From the previous analysis, the condition that $g_{mL} \gg g_{m1}$ and g_{m2} is very important and critical to the stability of an NMC amplifier. However, this condition is very difficult to achieve, especially in low-power design. If $g_{mL} \gg g_{m1}$ and g_{m2} does not hold true, the analysis should be re-started from (10). From this equation, since the s^2 term is negative, there are one RHP zero and one LHP zero. The RHP zero locates at a lower frequency as the s term is also negative. The LHP zero increases the PM while the RHP zero does the reverse, so just eliminating the RHP zero is sufficient. To do so, a modified structure of NMC using nulling resistor (NMCNR), is proposed [25] and is shown in Fig. 1(e). The transfer function is shown in (19) at the bottom of the page. The RHP zero can be eliminated by setting $R_m = 1/g_{mL}$ and only a LHP zero $z_1 = g_{mL}/C_{m1}$ is left. In fact, an exact value of R_m is difficult to obtain in IC design but it is not important since the function of R_m is not to create a LHP zero for pole–zero cancellation. Thus, the tolerance of the nulling resistor, same as in SMC, may be as high as $\pm 50\%$ and any value closed to $1/g_{mL}$ is able to locate the RHP zero to a high frequency. By defining $k_g = g_{m2}/g_{mL}$ and setting $R_m = 1/g_{mL}$, the transfer function is rewritten as (20) shown at the bottom of the page. It is noted that k_g must be smaller than 1, otherwise, the amplifier is unstable due to the RHP poles. In other words, the condition $g_{mL} > g_{m2}$ is required. The dimension conditions of C_{m1} and C_{m2} are obtained as in NMC using complex-pole approach and are given by

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right) C_L \tag{21}$$

$$C_{m2} = \frac{2}{1-k_g}\left(\frac{g_{m2}}{g_{mL}}\right) C_L. \tag{22}$$

By using the above conditions, the nondominant poles are $p_{2,3} = (g_{mL}/2(1-k_g)C_L) \pm j(g_{mL}/2(1-k_g)C_L)$ (i.e.,

$$A_{v\mathrm{NMCNR}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left\{1 + s\left[C_{m1}R_m + C_{m2}\left(R_m - \frac{1}{g_{mL}}\right)\right] + s^2\frac{C_{m1}C_{m2}(g_{mL}R_m - 1)}{g_{m2}g_{mL}}\right\}}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{C_{m2}(g_{mL} - g_{m2})}{g_{m2}g_{mL}} + s^2\frac{(1 - g_{m2}R_m)C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{19}$$

$$A_{v\mathrm{NMCNR}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1 + s\frac{C_{m1}}{g_{mL}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{(1-k_g)C_{m2}}{g_{m2}} + s^2\frac{(1-k_g)C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{20}$$

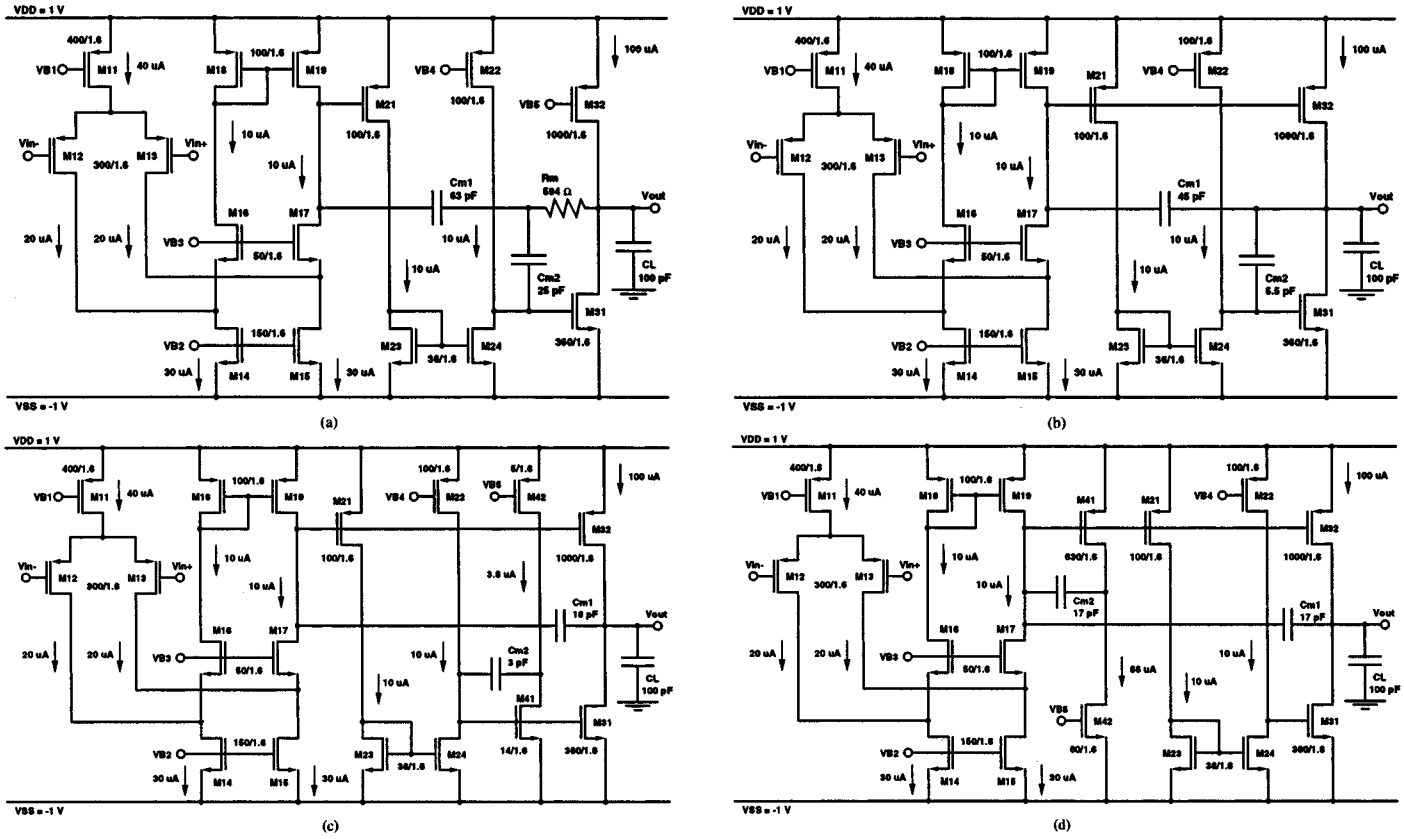

Fig. 7. Circuit diagram of the amplifiers (a) NMCNR. (b) NMCF. (c) DFCFC1. (d) DFCFC2.

$|p_{2,3}| = (g_{mL}/\sqrt{2}(1-k_g)C_L))$. The GBW is given by GBW $= g_{m1}/C_{m1} = 1/4(g_{mL}/C_L)$ and the PM is larger than 60° due to the LHP zero. A larger GBW can be obtained by slightly reducing C_{m1} but this reduces the PM.

To prove the proposed structure, NMC and NMCNR amplifiers were implemented in AMS[1] 0.8 μm double-metal double-poly CMOS process. The sheet resistance of the poly resistor is 23 Ω/sq. and the poly–poly capacitance is 1.77 fF/μm^2. The circuit diagram of the NMCNR amplifiers are shown in Fig. 7(a) and the NMC counterpart has the same circuitry without the nulling resistor. The chip micrograph is shown in Fig. 8. Both amplifiers drive a 100 pF//25 kΩ load and the first, second and output stage are implemented by M11–M19, M21–M24 and M31–M32. In addition, a 594 Ω nulling resistor, which is made of poly, is used in the NMCNR amplifier. In NMC, the required C_{m1} is 99 pF, but C_{m1} in NMCNR is 63 pF. As presented before, the PM of NMCNR amplifier is larger, so a smaller C_{m1} is used in the implementation to obtain a similar PM as in NMC and a larger GBW. Moreover, this greatly reduces the chip area from 0.23 mm^2 to 0.18 mm^2.

The measured results and improvement comparison are tabulated in Tables I and II, respectively. Both amplifiers have $\pm$ 1-V supply voltage, 400 μW power consumption and >100 dB dc gain. Since the power consumption of the NMC amplifier is low, the RHP zero affects the stability and hence the PM is poor. Comparing the NMCNR amplifier to the NMC counterpart, the GBW, PM, slew rate (SR) and settling time (T_s) are improved by +39%, +3°, +46%, and -30%, respectively. The improvement of the SR is due to the charging and discharging of smaller compensation capacitors during slewing while T_s is improved

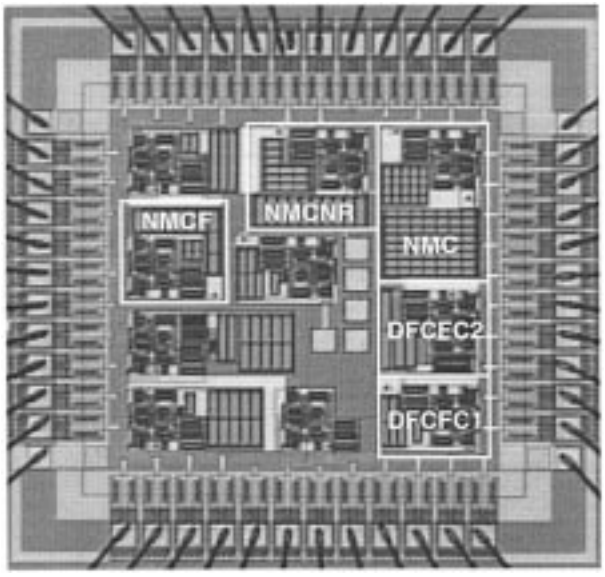

Fig. 8. Chip micrograph.

[1]Austria Miko Systeme International AG, Schloss Premstätten, A-8141 Unterpremstätten, Austria.

TABLE I
MEASURED RESULTS OF THE AMPLIFIERS

	NMC	NMCNR	NMCF	DFCFC1	DFCFC2
Supply Voltage (V)	±1				
Loading Condition	100 pF//25 kΩ				
Output Swing (V)	$-0.85 \le V_{out} \le 0.85$				
dc Gain (dB)	>100				
GBW (MHz)	0.59	0.82	1.22	2.60	2.60
PM (°)	43	46	62	43	48
SR^+/SR^- (V/μs)	0.23/0.23	0.36/0.31	0.50/0.50	1.36/1.27	1.13/0.95
T_s^+/T_s^- (μs) (to 1%)	4.25/4.36	3.03/3.04	1.49/1.53	0.96/1.37	1.12/0.77
$PSRR^+$@1kHz (dB)	85.80	92.61	93.81	108.86	103.32
$PSRR^+$@10kHz (dB)	64.10	75.62	75.75	91.93	85.35
$PSRR^-$@1kHz (dB)	53.66	106.44	127.47	93.92	122.19
$PSRR^-$@10kHz (dB)	35.61	84.62	90.60	82.55	110.17
Power (μW)	400	400	406	420	676
C_{m1} (pF)	99	63	45	18	17
C_{m2} (pF)	27	25	5.5	3	17
R_m (Ω)	-	594	-	-	-
Area (mm^2)	0.23	0.18	0.14	0.11	0.14

Note: Slew rate and settling time were measured in unity-gain non-inverting configuration with a 0.5 V step input, and ac response was measured with input common-mode level of -0.5 V.

TABLE II
IMPROVEMENT OF THE PROPOSED AND PUBLISHED TOPOLOGIES WITH NMC (†AVERAGE VALUE IS USED)

	NMCNR vs NMC [25] 0.8-μm CMOS C_L=100pF	NMCF vs NMC 0.8-μm CMOS C_L=100pF	DFCFC1 vs NMC [22], [23] 0.8-μm CMOS C_L=100pF	DFCFC2 vs NMC [24] 0.8-μm CMOS C_L=100pF	MNMC vs NMC [16] 3GHz f_t NPN C_L=100pF	NGCC vs NMC [20] 2.0-μm CMOS C_L=20pF
GBW	+39%	+107%	+341%	+341%	+67%	+64%
PM	+3°	+19°	same	+5°	-7°	-2°
SR	†+46%	†+117%	†+472%	†+352%	+75%	+100%
T_s	†-30%	†-65%	†-73%	†-78%	-14%	-
Power	same	+1.5%	+5%	+69%	same	+106%
Area	-22%	-39%	-52%	-39%	same	same

by the better PM and SR [29], [30]. The power-supply rejection ratio (PSRR), especially for the negative PSRR, is significantly improved since NMCNR uses smaller compensation capacitors and has larger high-frequency input-to-output voltage gain. Moreover, the nulling resistor increases the impedance and helps to block the noise from the supplies at high frequencies.

From the analysis and experimental results, it is proven that the proposed NMCNR structure greatly improves the GBW, PM, SR, T_s, and the chip area.

VI. MNMC

Besides increasing the power, the multipath technique can be used to increase the bandwidth of an amplifier. In MNMC [12], [16], [19], and [26], a feedforward transconductance stage (FTS) is added to the NMC structure to create a low-frequency LHP zero. This zero, called multipath zero, cancels the second nondominant pole to extend the bandwidth. The structure of MNMC is shown in Fig. 1(f) and it is limited to three-stage amplifiers but it has potential to extend to more stages. However, power consumption and circuit complexity are increased accordingly since a feedforward input differential stage, as same as MZC, is needed, so this will not be discussed here. The input of the FTS, with transconductance g_{mf1}, is V_{in} and the output is connected to the input of the output stage. Again, with the condition that $g_{mL} \gg g_{m1}$ and g_{m2}, the transfer function is given by (23) at the bottom of the next page. The nondominant poles are given by $p_2 =$

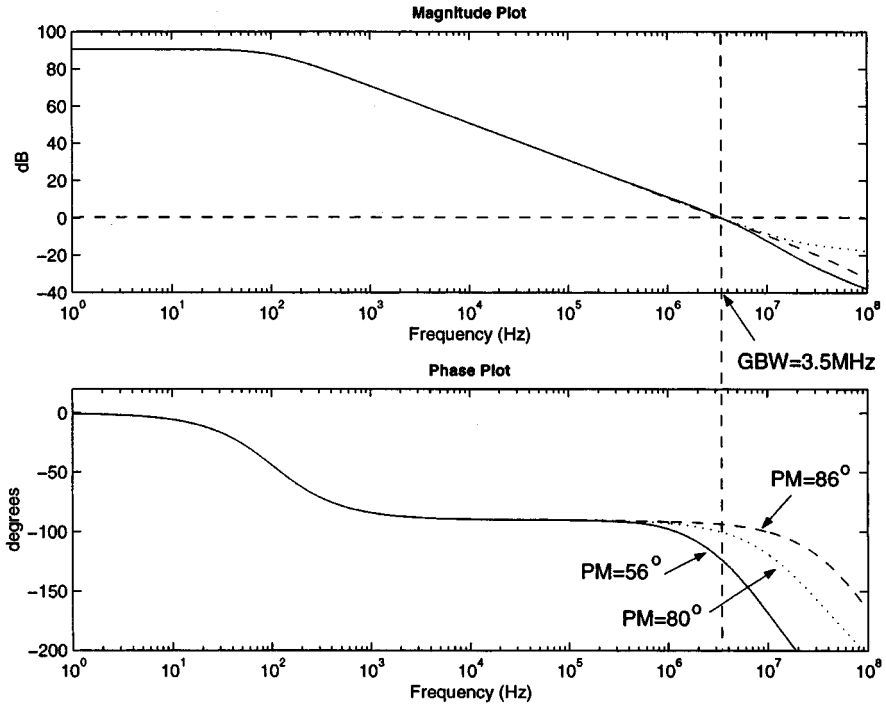

Fig. 9. Simulation results of an MNMC amplifier using equivalent small-signal circuit under the change of g_{mL} and C_L (solid: $g_{mL} = 1$ mA/V and $C_L = 20$ pF; dash: $g_{mL} = 10$ mA/V and $C_L = 20$ pF; dotted: $g_{mL} = 1$ mA/V and $C_L = 1$ pF).

$g_{mL}/2C_L - (g_{mL}/2C_L)\sqrt{1-(4g_{m2}/(g_{mL}/C_L)C_{m2})}$ and $p_3 = g_{mL}/2C_L + (g_{mL}/2C_L)\sqrt{1-(4g_{m2}/(g_{mL}/C_L)C_{m2})}$ while the multipath zero is given by $z_1 = g_{m1}g_{m2}/C_{m1}g_{mf1}$. It is clear that g_{mf1} controls the position of z_1 and pole–zero cancellation is achieved by setting $z_1 = p_2$. Moreover, the GBW of the MNMC amplifier after pole–zero cancellation depends on the position of p_3, so it is very important to move p_3 to a frequency as high as possible. Thus, the square-root term in the expression of p_3 should be set as close to one as possible. As proposed by Eschauzier *et al.* [16], it is achieved by setting $g_{m2}/C_{m2} = 0.1(g_{mL}/C_L)$. The explicit dimension condition of C_{m2} is, therefore, given by

$$C_{m2} = 10\left(\frac{g_{m2}}{g_{mL}}\right)C_L. \tag{24}$$

It is important to note that C_{m2} in MNMC is much larger than that in NMC. This increases the required chip area and reduces the SR dramatically. Therefore, emitter degeneration technique was used in the design of [16]. This can reduce the effective g_{m2} so that the g_{m2}/g_{mL} in (24) is smaller and the required C_{m2} is, as a result, smaller. With (24), the positions of p_2 and p_3 are changed to $p_2 = 0.11(g_{mL}/C_L)$ and $p_3 = 0.89(g_{mL}/C_L)$, respectively. The GBW is set to be half of p_3, so it is given by

$$\text{GBW} = \frac{g_{m1}}{C_{m1}} = 0.445\left(\frac{g_{mL}}{C_L}\right). \tag{25}$$

By comparing with the GBW of NMC in (17), the GBW of an MNMC amplifier is increased by 78%. Thus, MNMC overcomes the bandwidth reduction of nesting compensation. From (25), the dimension condition of C_{m1} is the following:

$$C_{m1} = 2.25\left(\frac{g_{m1}}{g_{mL}}\right)C_L \tag{26}$$

which is smaller than that in NMC. Another issue for concern is the cancellation of p_2 by z_1. As mentioned before, this requires $z_1 = p_2$ (i.e., $g_{m1}g_{m2}/C_{m1}g_{mf1} = 0.11g_{mL}/C_L$). Using (26) on this condition, the dimension condition of g_{mf1} is therefore

$$g_{mf1} = 4.45g_{m2}. \tag{27}$$

Since there are effectively two poles and $p_3 = 2 \cdot \text{GBW}$, the PM is approximately 63°. The above analysis gives the required values of C_{m1}, C_{m2} and g_{mf1} once g_{m1}, g_{m2}, g_{mL} and C_L are known. However, the above analysis is based on the condition that $g_{mL} \gg g_{m1}$ and g_{m2}. In fact, if this assumption does not hold true, the positions of the poles and the LHP zero are not those previously stated. Moreover, a RHP zero exists and the stability is greatly affected.

The analysis and dimension conditions are obtained in static state. Since there is a pole–zero doublet before the unity-gain frequency, the dynamic-state stability should also be considered. Since, in practice, the loading current and capacitance

$$A_{v_{\text{MNMC}}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1+s\frac{C_{m1}g_{mf1}}{g_{m1}g_{m2}}\right)}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \tag{23}$$

may change in some general-purpose amplifiers with Class-AB output stage, it is necessary to consider the stability of the MNMC amplifier when g_{mL} is increased and C_L is decreased. From (23), if either case occurs, the coefficient of the s^2 term in the function of the nondominant poles will be decreased. This function can be then approximated as a first-order function if the changes are too large. As a result, only one pole is left and is given by $p_2' = g_{m2}/C_{m2} = 4.44(g_{m1}/C_{m1})$, where the ratio is obtained from (24) and (26). Besides, the multipath zero is not changed when g_{mL} and C_L are changed and it is re-written as $z_1 = 4.45(g_{m1}/C_{m1})$ with the condition in (27). It is obvious that $z_1 \approx p_2'$, so MNMC is not affected by changing the loading current and capacitance.

To prove the above arguments, a simulation using HSPICE is performed with the equivalent small-signal circuit of an MNMC amplifier. The circuit parameters are $g_{m1} = 50\ \mu$ A/V, $g_{m2} =$ 25 mAV, $g_{mL} = 1$ mA/V, $R_{o1} = 1$ MΩ, $R_{o2} = 1$ MΩ, $R_L =$ 25 kΩ, C_{p1} =100 fF, $C_{p2} = 100$ fF, $C_L = 20$ pF. Thus, $C_{m1} =$ 2.25 pF, $C_{m2} = 5$ pF and $g_{mf1} = 111.25\ \mu$A/V are required, according to (24), (26), and (27). After the static-state dimensions are fixed, two cases are considered: 1) g_{mL} is changed from 1 mA/V to 10 mA/V; and 2) C_L is changed from 20 to 1 pF. From the simulation results shown in Fig. 9, it is proven that z_1 matches well with p_2 in spite of the changes of g_{mL} and C_L. Thus, both cases are stable. Moreover, the PM is increased as p_3 moves to a higher frequency when either g_{mL} is increased or C_L is decreased.

VII. NGCC

In both NMC and MNMC structures, the condition that $g_{mL} \gg g_{m1}$ and g_{m2} are required. This condition not only improves the stability but it also simplifies the transfer function. In fact, as mentioned before, this condition is difficult to achieve in low-power design, so You *et al.* introduced NGCC [20]. NGCC is an N-stage amplifier compensation structure which uses MZC on NMC repeatedly. The feedforward small-signal current through the compensation capacitors are all canceled by the out-of-phase small-signal current from the FTSs and this makes a zero-free amplifier. In addition, the function of poles is simplified by the structure and is systematic for N-stage NGCC amplifier. With the condition that $g_{mfi} = g_{mi}$ where $i = 1$ to $N-1$, the general form of an N-stage NGCC amplifier is given by (28) shown at the bottom of the page. From (28), NGCC provides a more systematic and simpler transfer function for N-stage amplifier than NMC.

In the stability conditions proposed by You *et al.*, the separated-pole approach is used and the nondominant poles are set to some frequencies such that the GBW, T_S and power consumption are all optimized. Undoubtedly, this is complicated to do optimization analytically, so numerical analysis using MATLAB is required. However, questions are raised on practical considerations, since it is preferable to use as minimum stages as possible. As stated before, three stages is an optimum number on dc gain, bandwidth, and power consumption. Therefore, the analysis in this section is focused on the three-stage NGCC amplifier. The structure of a three-stage NGCC amplifier is shown in Fig. 1(g) and the transfer function is given by (29) shown at the bottom of the page. As stated before and also from the numerator of (29), the zeros can all be eliminated by setting $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$. The transfer function is then simplified to (30) shown at the bottom of the page. The arrangement of the poles can use either the separate-pole or complex-pole approach but the latter one is preferred. It is obvious that the denominator of (30) is the same as (11) but the difference is that $g_{mL} \gg g_{m1}$ and g_{m2} is not required in NGCC. Thus, $C_{m1} = 4(g_{m1}/g_{mL})C_L$ and $C_{m2} = 2(g_{m2}/g_{mL})C_L$ are used. The GBW is given by GBW $= (1/4)(g_{mL}/C_L)$ and the PM is approximately 60°.

Although NGCC is good in low-power designs, the input-stage FTS (i.e., g_{mf1}) is complicated in circuit implementation (same argument as stated previously in Section IV B, and consumes more power, especially when rail-to-rail input stage is needed. Moreover, it is not necessary to eliminate all zeros as

$$A_{v_{NGCC}N}(s) = \frac{g_{mL}R_L\prod_{i=1}^{N-1} g_{mi}R_{oi}}{\left(1+sC_{m1}g_{mL}R_{o1}R_L\prod_{i=2}^{N-1} g_{mi}R_{oi}\right)\left[1+\sum_{i=1}^{N-2} s^i\left(\prod_{j=2}^{i+1}\frac{C_{mj}}{g_{mj}}\right)+s^{N-1}\frac{C_L}{g_{mL}}\prod_{i=2}^{N-1}\frac{C_{mi}}{g_{mi}}\right]} \tag{28}$$

$$A_{v_{NGCC}3}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left[1+s\frac{C_{m2}(g_{mf2}-g_{m2})}{g_{m2}g_{mL}}+s^2\frac{C_{m1}C_{m2}(g_{mf1}-g_{m1})}{g_{m1}g_{m2}g_{mL}}\right]}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}(g_{mf2}-g_{m2}+g_{mL})}{g_{m2}g_{mL}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{29}$$

$$A_{v_{NGCC}3}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \tag{30}$$

some of them are LHP zeros which, in fact, help to increase the PM. With regard to the above considerations, a new structure, called NMC with feedforward Gm stage (NMCF), is proposed and shown in Fig. 1(h). There are only two differences between NMCF and NGCC: 1) the input-stage FTS is removed and 2) g_{mf2} is larger than g_{m2}. By defining $m = (g_{mf2}/g_{m2}) > 1$ and $k_g = g_{m2}/g_{mL}$, the transfer function of an NMCF amplifier is given by (31) shown at the bottom of the page. The dimension conditions of C_{m1} and C_{m2} are obtained using the complex-pole approach and they are given by

$$C_{m1} = \frac{4}{1+k_g(m-1)}\left(\frac{g_{m1}}{g_{mL}}\right)C_L \tag{32}$$

$$C_{m2} = \frac{2}{[1+k_g(m-1)]^2}\left(\frac{g_{m2}}{g_{mL}}\right)C_L. \tag{33}$$

The required compensation capacitors, especially C_{m2}, are smaller than those in NMC, MNMC and NGCC since $[1+k_g(m-1)]$ is always larger than one in NMCF. By using the conditions, the nondominant complex pole is given by $|p_{2,3}| = (1+k_g(m-1)/\sqrt{2})\,(g_{mL}/C_L)$.

The second-order function of zeros implies two zeros in the amplifier. Since the s term is positive and the s^2 term is negative, the LHP zero

$$z_1 = \frac{(m-1)g_{m2}}{2C_{m1}}\left\{\sqrt{1+\frac{8[1+k_g(m-1)]g_{m1}g_{mL}}{(m-1)^2 g_{m2}^2}}-1\right\}$$

locates before the RHP zero

$$z_2 = -\frac{(m-1)g_{m2}}{2C_{m1}}\left\{\sqrt{1+\frac{8[1+k_g(m-1)]g_{m1}g_{mL}}{(m-1)^2 g_{m2}^2}}+1\right\}.$$

The LHP zero should be located after $|p_{2,3}|$ for stability purpose, so the following condition is required:

$$g_{mL} \geq (\sqrt{2}-1)(g_{mf2}-g_{m2}) + 4g_{m1}. \tag{34}$$

The condition states the minimum value of g_{mL} to obtain an optimum control of LHP zero.

From (31) to (33), the GBW and PM are given by

$$\text{GBW} = \frac{g_{m1}}{C_{m1}} = \frac{1}{4}\left(\frac{g_{mf2}-g_{m2}+g_{mL}}{C_L}\right) \tag{35}$$

and

$$\text{PM} = 60^\circ + \tan^{-1}\left(\frac{\text{GBW}}{z_1}\right) - \tan^{-1}\left(\frac{\text{GBW}}{|z_2|}\right) > 60^\circ. \tag{36}$$

It is shown in (35) that the bandwidth is improved by the presence of g_{mf2}. Moreover, since the required compensation capacitors are smaller and the bandwidth of the amplifier is extended when using NMCF, the occupied chip area is reduced and the PSRR is also improved.

Again, experimental works implemented in AMS 0.8 μm CMOS process was done to prove the proposed structure. The NMCF amplifier is shown in Fig. 7(b) and it is basically the same as the NMC amplifier. It is noted that the gate of M32, which is the FTS, is connected to the output of the first stage. The output stage is of push-pull type and g_{mf2} is set to be the same as g_{mL}, from (35), to double the GBW.

The measured results and improvement comparison are shown in Tables I and II, respectively. It is obvious that the improvement of NMCF over NMC on GBW ($+107\%$), PM ($+19^\circ$), SR ($+117\%$), T_s (-65%) and occupied chip area (-39%) are much larger than those in MNMC and NGCC in other designs, which are shown in Table II. The power consumption is only increased by 6 μW($+1.5\%$).

VIII. DFCFC

From the previous analysis, the GBW of nesting compensated amplifiers are directly proportional to g_{mL} and inversely proportional to C_L. Obviously, higher power consumption is required to have a large GBW for a large C_L. To tackle this problem, DFCFC, which is targeted for three-stage amplifiers driving large capacitive loads, has been proposed [22]–[24].

Since the bandwidth reduction of the previous topologies is due to the nesting of the compensation capacitors [12], [16], [21], [26], C_{m2} is removed and the bandwidth of the amplifier can be extended substantially. However, the damping factor of the nondominant complex poles, which is originally controlled by C_{m2}, cannot be controlled and a frequency peak, which causes the closed-loop amplifier to be unstable, appears in the magnitude Bode plot [23]. To control the damping factor and make the amplifier stable, a damping-factor-control (DFC) block is added. The DFC block is basically a gain stage with dc gain greater than one (i.e., $g_{m4}R_{o4} > 1$) and a feedback capacitor C_{m2}. The DFC block functions as a frequency-dependent capacitor and the amount of the small-signal current injected into the DFC block depends on the value of C_{m2} and g_{m4} (transconductance of the gain stage inside the DFC block). Hence, the damping factor of the nondominant complex poles can be controlled by optimum C_{m2} and g_{m4} and this makes the amplifier stable. There are two possible positions to add the DFC block and they are shown in Fig. 1(i) for DFCFC1 and Fig. 1(j) for DFCFC2. In addition, both structures have a feedforward transconductance stage to form a push-pull output stage for improving large-signal slewing performance.

For DFCFC1, the transfer function is given by (37) shown at the bottom of the next page. It can be seen from (37) that the damping factor of the nondominant poles can be controlled by g_{m4}. Moreover, the effect of C_{m2} and R_{o4} is canceled in the

$$A_{v_{\text{NMCF}}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left[1+s\frac{(m-1)C_{m2}}{g_{mL}}-s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right]}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{[1+k_g(m-1)]C_{m2}}{g_{m2}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{31}$$

transfer function but C_{m2} is limited to $C_{m1} \geq C_{m2} > C_{p2}$ to validate (37). Since C_{m2} is small, the amplifier is not slowed down by C_{m2}. From (37), there are three poles, so the complex-pole approach is used. Moreover, since it is preferable to have the same output current capability for both the p- and n-transistor of the output stage, the sizes of the p- and n-transistor are used in ratio of 3 to 1 to compensate for the difference in the mobilities of the carriers. Thus, it is reasonable to set $g_{mf2} = g_{mL}$, so the dimension conditions are given by

$$C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right) C_L \tag{38}$$

$$g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right) g_{mL} \tag{39}$$

where

$$\beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2}}{g_{mL}}\right)}. \tag{40}$$

A large β is obtained when the amplifier drives a large capacitive load (i.e., large C_L). The required C_{m1} is much smaller than that in the previous nesting topologies, so the SR is also greatly improved, assuming that the SR is not limited by the output stage. Moreover, g_{m4} is a decreasing function of C_L, so the power consumption is not large for a large C_L. With (38) and (39), the GBW is given by

$$GBW = \frac{g_{m1}}{C_{m1}} = \frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right) \tag{41}$$

and the PM is about 60°. From (41), it is shown that the GBW is larger than NMC by β times. If β is set to a value larger than 4, the GBW is even better than that of a single-stage amplifier with similar power consumption. Thus, DFCFC1 is especially suitable for amplifiers driving large capacitive loads. Furthermore, the GBW can be further increased by reducing C_{m1} a little, but this reduces the PM as a tradeoff.

For DFCFC2, by setting $g_{mf2} = g_{mL}$ with the same reason stated previously, the transfer function is given by (42) shown at the bottom of the page. Similar to DFCFC1, the complex-pole approach is used to achieve the stability. Therefore, the dimension conditions are given by

$$C_{m1} = C_{m2} = g_{m1}\sqrt{\frac{8C_{p2}C_L}{g_{m2}g_{mL}}} \tag{43}$$

$$g_{m4} = 4g_{m1}. \tag{44}$$

From (44), the required g_{m4} is a fixed value and is four times of g_{m1}. Thus, the power consumption of DFCFC2 amplifier with certain value of C_L may be larger than that of the DFCFC1 counterpart.

From (42) to (44), the GBW is given by

$$\text{GBW} = \frac{g_{m1}}{C_{m1}} = \sqrt{\frac{g_{m2}g_{mL}}{8C_{p2}C_L}} \tag{45}$$

and the PM is about 60°. Although it is difficult to compare the GBW of DFCFC2 with other topologies since the format is different, it is in general better than others. It is due to the fact that the GBW is inversely proportion to the geometric mean of C_L and C_{p2}, which gives a smaller value than C_L alone.

Similar to the proposed NMCNR and NMCF, DFCFC1, and DFCFC2 amplifiers were implemented in AMS 0.8 μm double-metal double-poly CMOS process. The circuit diagrams are shown in Fig. 7(c) for DFCFC1 and Fig. 7(d) for DFCFC2. The micrograph is, again, shown in Fig. 8. In both amplifiers, M41 and C_{m2} form the DFC block and M32 is the FTS. Moreover, from Table II, the GBW, PM, SR, T_s and chip area with a large C_L are much better than NMC, NMCNR, MNMC, NGCC, and NMCF.

On the implementation of DFCFC1 and DFCFC2, since the DFC block is basically a gain stage, there is a high impedance node which is outside the feedback loop. The node voltage may pull up to VDD or pull down to ground if process variations exists. Thus, a local feedback circuitry, as shown in Fig. 10, can be added to control the dc operating point of the high impedance node. The loop gain of the control circuitry must be smaller than the gain of the DFC block. Otherwise, the high impedance node will be set to a stable dc voltage and the signal will be null. Thus, source degeneration is used in the control circuitry.

Although DFCFC can improve the ac and transient responses, it is effective only when driving large capacitive load. For small capacitive load applications, other compensation techniques are more appropriate.

$$A_{v_{\text{DFCFC1}}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1 + s\frac{C_{p2}g_{mf2} - C_{m1}g_{m4}}{g_{m2}g_{mL} + g_{mf2}g_{m4}} - s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{mL} + g_{mf2}g_{m4}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1 + s\frac{C_L g_{m4}}{g_{m2}g_{mL} + g_{mf2}g_{m4}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL} + g_{mf2}g_{m4}}\right)} \tag{37}$$

$$A_{v_{\text{DFCFC2}}}(s) = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1 + s\frac{C_{p2}g_{mL}R_2 - C_{m1}}{g_{m2}g_{mL}R_{o2}} - s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{mL}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{C_{p2}\left(1 + \frac{C_L g_{m4}}{C_{m1}g_{mL}}\right)}{g_{m2}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right]} \tag{42}$$

TABLE III
SUMMARY OF THE STUDIED AND PROPOSED FREQUENCY COMPENSATION TOPOLOGIES

Topology	dc gain	Stability conditions	GBW	PM
single	$g_{mL}R_L$	GBW $< \frac{1}{2}min(p_{par}, z_{par})$	$\frac{g_{mL}}{C_L}$	90^o
SMC	$g_{m1}g_{mL}R_{o1}R_L$	$C_m = 2\left(\frac{g_{m1}}{g_{mL}}\right)C_L$	$\frac{1}{2}\left(\frac{g_{mL}}{C_L}\right)$	$63^o - \tan^{-1}\left(\frac{g_{m1}}{g_{mL}}\right)$
SMCNR	$g_{m1}g_{mL}R_{o1}R_L$	$C_m = 2\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $\frac{1}{g_{mL}} \le R_m < \frac{1}{10}R_{o1}$	$\frac{1}{2}\left(\frac{g_{mL}}{C_L}\right)$	63^o
MZC1	$g_{m1}g_{mL}R_{o1}R_L$	$C_m = 2\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $g_{mf1} = g_{m1}$	$\frac{1}{2}\left(\frac{g_{mL}}{C_L}\right)$	63^o
MZC2 (fixed C_L)	$g_{m1}g_{mL}R_{o1}R_L$	$C_m = \frac{C_L}{r_g - 1} \ge 10C_{p1}$ where $r_g = \frac{g_{mf1}}{g_{m1}} > 1$	$\frac{g_{m1}}{C_{m1}}$	90^o
NMC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mL} \gg g_{m1}$ and g_{m2} $C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right)C_L$	$\frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$	60^o
NMCNR	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$R_m = \frac{1}{g_{mL}}$ $C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = \frac{2}{1-k_g}\left(\frac{g_{m2}}{g_{mL}}\right)C_L$ where $k_g = \frac{g_{m2}}{g_{mL}}$	$\frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$	$>60^o$
MNMC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mL} \gg g_{m1}$ and g_{m2} $C_{m1} = 2.25\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = 10\left(\frac{g_{m2}}{g_{mL}}\right)C_L$	$0.445\left(\frac{g_{mL}}{C_L}\right)$	63^o
NGCC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$ $C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right)C_L$	$\frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$	60^o
NMCF	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mf2} > g_{m2}$ $g_{mL} \ge (\sqrt{2}-1)(g_{mf2} - g_{m2}) + 4g_{m1}$ $C_{m1} = \frac{4}{1+k_g(m-1)}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = \frac{2}{[1+k_g(m-1)]^2}\left(\frac{g_{m2}}{g_{mL}}\right)C_L$ where $m = \frac{g_{mf2}}{g_{m2}}$ and $k_g = \frac{g_{m2}}{g_{mL}}$	$\frac{1}{4}\left(\frac{g_{mf2}-g_{m2}+g_{mL}}{C_L}\right)$	$>60^o$
DFCFC1	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mf2} = g_{mL}$ $C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m1} \ge C_{m2} > C_{p2}$ $g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right)g_{mL}$ where $\beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2}}{g_{mL}}\right)}$	$\frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right)$	60^o
DFCFC2	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L$	$g_{mf2} = g_{mL}$ $C_{m1} = C_{m2} = g_{m1}\sqrt{\frac{8C_{p2}C_L}{g_{m2}g_{mL}}}$ $g_{m4} = 4g_{m1}$	$\sqrt{\frac{g_{m2}g_{mL}}{8C_{p2}C_L}}$	60^o

IX. SUMMARY OF STUDIED FREQUENCY COMPENSATION TOPOLOGIES

A summary on the required stability conditions, resultant GBW and PM for all studied and proposed topologies are given in Table III. Comparisons on the topologies are tabulated in Table IV. Moreover, some important points derived from the previous analyzes are summarized as follows.

1) The stability-dimension conditions of all topologies are based on the assumptions stated in Section II. If the assumptions cannot be met, numerical method should be used to stabilize the amplifiers.
2) With the exception of the single-stage amplifier, a larger C_L causes the amplifier to be more unstable.
3) The stability dimension conditions must be set in the worst case scenario (i.e., smallest g_{mL} and largest C_L).
4) The GBW, except MZC with fixed C_L, can be increased by increasing g_{mL} and reducing C_L. Thus, increasing the transconductance of the input stage, except the single-stage amplifier, does not help to improve the GBW and PM.
5) Smaller compensation capacitances can be achieved by a smaller g_{m1} to g_{mL} ratio and a smaller g_{m2} to g_{mL} ratio.
6) For high-speed applications, a larger bias current should be applied to the output stage to increase g_{mL}.

TABLE IV
COMPARISON ON THE STUDIED AND PROPOSED FREQUENCY COMPENSATION TOPOLOGIES

	Single	SMC	SMCNR	MZC1	MZC2	NMC	NMCNR	MNMC	NGCC	NMCF	DFCFC1	DFCFC2
dc Gain	-	o	o	o	o	++	++	++	++	++	++	++
Low Voltage	-	+	+	+	+	++	++	++	++	++	++	++
Low Power	++	-	o	+	+	-	o	-	++	++	++	++
GBW/PM@Small C_L	++	o	o	o	+	o	o	+	o	+	-	-
GBW/PM@Large C_L	++	o	o	o	++	-	-	o	-	o	++	++
SR/T_s	++	o	o	o	o	-	o	-	o	+	++	++
Capacitor Values	++	o	o	o	+	-	o	o	o	+	++	++
Pole-zero Doublet	++	++	++	++	o	++	++	o	++	++	++	++

++=excellent +=good o=moderate -=poor

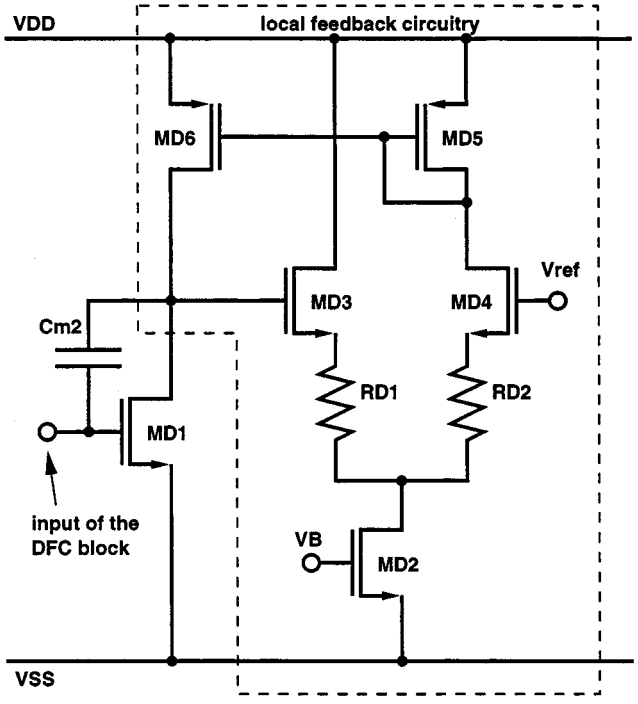

Fig. 10. Local feedback circuitry to control the dc operating point of the DFC block.

X. ROBUSTNESS OF THE STUDIED FREQUENCY COMPENSATION

In IC technologies, the circuit parameters such as transconductance, capacitance and resistance vary from run to run, lot to lot and also according to temperature. The robustness of frequency compensation is very important to ensure the stabilities of multistage amplifiers.

From the summary in Table III, the required values of compensation capacitors depend on the ratio of transconductances of gain stages explicitly for SMC, SMCNR, MZC1, MZC2, NMC, NMCNR, MNMC, NGCC, NMCF, and DFCFC1 and implicitly for DFCFC2. The ratio maintains constant for any process variation and temperature effect with good bias current matching and transistor size matching (due to design). One important point is that the value of C_L is the worst case capacitance at the output of the amplifier (stated in Section IX). Thus, it is important for the designers to estimate the worst case C_L to ensure the stabilities of the amplifiers. In addition, the requirements of transconductances are also in ratio and stability is also free from the effect of process variations.

In SMCNR and NMCNR, the function of the nulling resistor is to eliminate the RHP zero or move it to a higher frequency but not to perform pole–zero cancellation (unlike in [21] where multiple pole–zero cancellations are needed and so tracking bias circuitry is required). As a results, process variation on the value of the nulling resistor, up to $\pm 50\%$, in general is not significant to the stability.

In MNMC, pole–zero cancellation is used. However, the superior tracking technique in MNMC is due to the pole–zero cancellation based on the ratios of transconductances and compensation capacitances. Thus, process variations do not affect the compression of the pole–zero doublet.

Although the robustness of the studied topologies are good, the exact value of the GBW will be affected by process variations. Referring to Table III, the GBW's of all topologies, including commonly used single-stage and Miller-compensated amplifiers, depend on the transconductance of the output stage. Thus, the GBW will change under the effect of process variations and temperature.

XI. CONCLUSION

Several frequency-compensation topologies have been investigated analytically. The pros and cons as well as the design requirements are discussed. To improve NMC and NGCC, NMCNR, and NMCF are proposed and the improved performance is verified by experimental results. In addition, DFCFC has been introduced and it has much better frequency and transient performances than the other published topologies for driving large capacitive loads. Finally, robustness of the studied topologies has been discussed.

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