Low-Voltage Analog Circuit Design Based on Biased Inverting Opamp Configuration

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***Abstract*—Analog circuit designs that use inverting opamp configuration can be converted into low-voltage designs by biasing the opamp input common-mode voltage to near one of the supply rails. This is achieved by introducing a current source or a resistor between the opamp negative input terminal and one of the supply rails. Hence, in this technique, opamps with limited input common-mode range can be used. In addition, switches can be incorporated in these circuits to allow a wide range of applications. This technique also allows large input and output signal swings (close to rail-to-rail), even at a very low-voltage supply. To demonstrate the proposed technique, four track-and-hold amplifiers (THA's) and a 10-bit digital-to-analog converter (DAC) have been designed in a conventional 1.2 μm CMOS process and tested at a 1-V supply. The DAC consumes less than 0.45 mW and has a maximum throughput of 1 MS/s, with close to rail-to-rail output (0.1 –0.9 V). The maximum differential nonlinearity error and integral nonlinearity error were measured to be 1.7 least significant bits (LSB's) and 3.0 LSB's, respectively. Each THA dissipates less than 0.35 mW and achieves a hold mode total harmonic distortion of less than −61 dB for a 100 kHz, 1.4 $V_{p\text{-}p}$ differential input signal, sampled at a rate of 1 MS/s.**

***Index Terms*—Digital-to-analog converter, low voltage, sample-and-hold, track-and-hold amplifier.**

I. Introduction

INCREASING demand for battery-operated systems and the reduction of IC supply voltage due to technology scaling, force the need to find circuit techniques that can operate at power supply voltages in the range of 1–2 V, with low power consumption. For digital circuit design, it is capable to operate them at such low voltage even using the technologies available today [1]. However, scaling the supply voltage down presents a formidable challenge to design analog circuits. This challenge comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges. For future standard CMOS processes, the threshold voltages may not decrease much below what is available today [2]. Although low-voltage analog circuit design can be achieved using low threshold voltage devices [3], [4], it is a high-cost solution due to the requirement of nonstandard processing. Another solution is to use on-chip dc-to-dc converters or other bootstrapping techniques to increase the internal supply voltage. However, a high internal supply voltage may not be tolerable for scaled-down technologies. Therefore, circuit techniques must be developed to operate analog circuits at a low supply voltage using relatively high threshold voltage devices. It should be noted that these techniques will offer the potential for the best utilization of a given technology at any voltage range, even if low threshold voltage technologies become standard.

One of the most common building blocks in analog circuit design is the opamp. To achieve low supply voltages with rail-to-rail signal swings, opamp input stages with rail-to-rail input common-mode ranges have been developed [5]–[7] in standard CMOS process with a supply voltage in the range of 1.2–3 V. The supply voltage can go as low as 1 V if the input differential stage of an opamp is realized using bulk-driven MOSFET's [8] or depletion devices available in some specialized BiCMOS process [9]. Using these opamps, many low-voltage analog circuits such as active resistance–capacitance (*RC*) filters can be realized. However, designing analog circuits that require switches such as sample-and-hold amplifiers at low supply voltages still remains a challenge. When the supply voltage is less than the sum of the threshold voltages of pMOS and nMOS, the switches will fail to pass voltages in the mid-range of the power supply even if transmission gates are used [10]. To deal with this problem, switched-opamp technique has been proposed [11]. This technique avoids the use of critical switches to pass voltages in the mid-range by turning on or off the opamps, and hence, it can be used effectively whenever the output of an opamp drives the capacitors connected to the inputs of another opamps. However, there are two disadvantages of this technique. First, at the front end, critical switches connected to off-chip input signals cannot be avoided and direct input through MOSFET switches usually result in a low signal input range [10], [12]. Furthermore, the outputs of the opamps in a switched-opamp circuit are always required to swing from one of the supply voltage during one of the clock phases, and hence, the output signals may be slew-rate limited. Despite these disadvantages, switched-opamp technique is a very effective technique to implement low-voltage discrete-time analog circuits. Many switched-capacitor circuits can be implemented using switched-opamp technique such as discrete-time filter [10] and sigma–delta modulator [13].

In this paper, an alternative low-voltage analog circuit technique is proposed. Similar to switched-opamp technique, it avoids the need to have a wide common-mode input range opamp. At the same time, no critical switches for passing voltage signals are needed. Using the proposed technique, a 10-bit DAC and several track-and-hold amplifiers (THA's)

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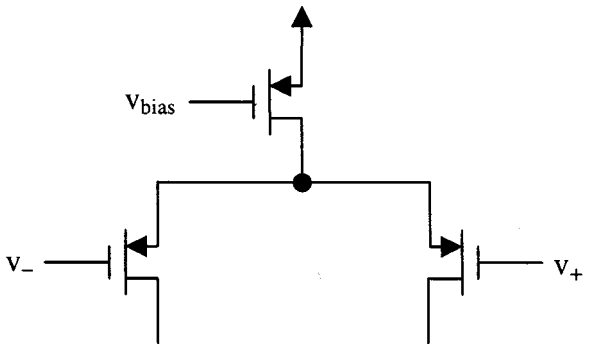

Fig. 1. A pMOS differential input stage.

using a 1-V supply were implemented in a conventional 1.2-μm CMOS process with $V_{tn} \approx 0.6$ V and $V_{\rm tp} \approx -0.8$ V, as described in this paper.

II. Proposed Technique

Fig. 1 illustrates a conventional CMOS opamp input stage utilizing a pMOS differential pair. The maximum input common-mode voltage is limited to $V_{\rm DD} - 2V_{\rm SDsat} - |V_{\rm tp}|$. For a conventional inverting opamp circuit, which has a structure similar to that shown in Fig. 2(a), but without the current source I_B, the output voltage can be written as

$$v_o = v_x\left(1 + \frac{R_f}{R_{\rm eq}}\right) - R_f\left(\frac{1}{R_1}v_1 + \cdots + \frac{1}{R_n}v_n\right) \quad (1)$$

where $R_{\rm eq} = R_1//\cdots//R_n$. To maximize the signal swing, the input/output quiescent voltage is normally set at $V_{\rm DD}/2$, and hence, v_x is required to be set at $V_{\rm DD}/2$. Owing to the limited opamp input common-mode range, the supply voltage is required to be greater than $2 \times (2V_{\rm SDsat} + |V_{\rm tp}|)$. Therefore, the circuit cannot operate at a 1-V supply for $|V_{\rm tp}|$ greater than 0.4 V. To reduce the supply voltage, the opamp input common-mode voltage v_x has to be biased to a voltage close to ground, independent of the input and output quiescent voltage. To achieve this, we propose a simply technique that may have been known for years but has not been applied effectively to design low-voltage analog circuits. In this technique, a current source I_B is introduced as shown in Fig. 2(a). If the input and output quiescent voltages are equal to $V_{\rm DD}/2$, the required value for I_B can be determined as

$$I_B = \left(\frac{V_{\rm DD}}{2} - v_x\right)\left(\frac{1}{R_f} + \frac{1}{R_{\rm eq}}\right). \quad (2)$$

Since I_B is most conveniently realized using an nMOS, the value of v_x has to be greater than $V_{\rm DSsat}$, and hence, the minimum supply voltage for the circuit is $V_{\rm DSsat} + 2V_{\rm SDsat} + |V_{\rm tp}|$. Without the addition of the current source, the minimum supply voltage has to be approximately doubled. If the input stage of the opamp is realized using nMOS differential pair, setting v_x close to $V_{\rm DD}$ with a pMOS current source I_B connected between the opamp negative input terminal and $V_{\rm DD}$ will minimize the supply voltage.

Based on the same principle, another approach to bias the opamp input common-mode voltage is to use a resistor or a MOSFET operating in the triode region as shown in Fig. 2(b). The resistance R_B can be determined as

$$R_B = \frac{v_x}{\frac{V_{\rm DD}}{2} - v_x}(R_f//R_{\rm eq}). \quad (3)$$

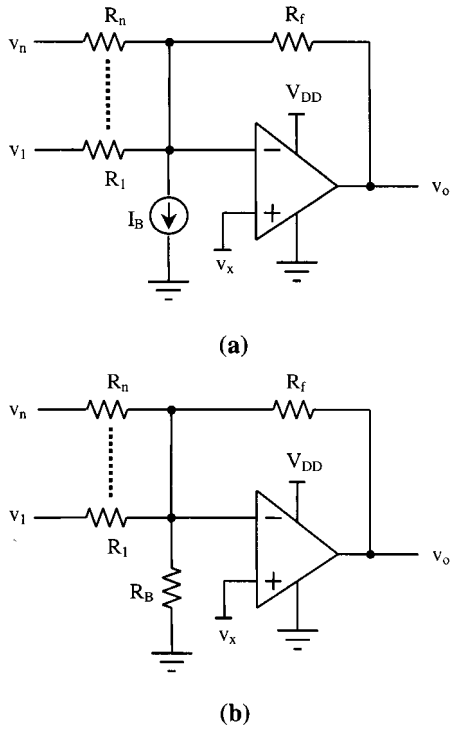

Fig. 2. Proposed biasing schemes that use (a) a current source and (b) a resistor.

The second approach has an advantage of setting v_x to a value lower than one $V_{\rm DSsat}$ (but greater than ground). Both approaches can also be extended to convert a fully differential inverting opamp configuration into a low-voltage design. In this case, two current sources or two resistors are required to connect to the fully differential opamp inputs, and the values of the current sources or the values of the resistors can be determined based on the input and output common-mode voltages.

Addition of the current source or the resistor will induce minimal effects on the low frequency ac response since they are connected to the virtual ground of the opamp. However, at high frequency, the bandwidths of the two schemes are different. The feedback factor β_i for the biasing scheme that uses current source can be determined as

$$\beta_i = \frac{R_{\rm eq}//r_{\rm ds}}{R_{\rm eq}//r_{\rm ds} + R_f} \quad (4)$$

where $r_{\rm ds}$ is the output resistance of the current source. The feedback factor β_r for the resistor scheme can also be expressed similar to (4), with $r_{\rm ds}$ changed to R_B. As observed from (3), R_B is usually smaller than $R_{\rm eq}$ and $r_{\rm ds}$. Thus β_i will be larger than β_r and therefore, the scheme that uses current source will have a higher bandwidth given by $\beta_i \cdot f_t$, where f_t is the unity-gain frequency of the opamp. Nevertheless, using the proposed biasing schemes, any circuit that uses inverting opamp configuration such as continuous time active *RC* filters

can be converted into a low-voltage design with a minimum supply voltage approximately equal to $3V_{\rm DSsat} + V_t$. This reduction in supply voltage, however, comes with a price of increasing the overall noise. The mean squared output noise $v_{\rm no}^2$ for both circuits shown in Fig. 2 can be written as

$$v_{\rm no}^2 = \left(I_{\rm neq}^2 + I_{nf}^2 + I_n^2\right) R_f^2 + v_{na}^2 \left(1 + \frac{R_f}{R_{\rm eq}//R_x}\right)^2 \quad (5)$$

where $I_{\rm neq}, I_{nf}$ and v_{na} are the equivalent noise currents of $R_{\rm eq}$ and R_f and the equivalent input noise voltage of the opamp, respectively. When compared to the case without the addition of R_B and I_B, additional terms I_n^2 and R_x are presented in (5). For Fig. 2(a), R_x is equal to $r_{\rm ds}$, and I_n^2 is due to the equivalent noise current of I_B. With $v_x = V_{\rm DSsat}, I_n^2$ can then be derived using (2) as

$$I_n^2 = \frac{16}{3} KT \frac{\frac{V_{\rm DD}}{2} - v_x}{v_x (R_f // R_{\rm eq})} \quad (6)$$

where only thermal noise is considered. For Fig. 2(b), R_x is equal to R_B, and I_n^2 is due to the equivalent noise current of R_B that can also be described using (6) except that the scaling factor $16/3$ is now equal to 4. For most cases, the term due to the opamp noise v_{na}^2 is usually the domain factor. Since $R_B < R_{\rm eq} < r_{\rm ds}$, the circuit shown in Fig. 2(a) has lower noise than the circuit shown in Fig. 2(b). Furthermore, due to the term I_n^2, it has a slightly higher noise than the case when either R_B or I_B is omitted. For example, if $v_{na} = 50$ nV/$\sqrt{\rm Hz}$, $R_{\rm eq} = R_f = 20$ kΩ, $V_{\rm DD} = 1$ V, $v_x = 0.1$ V, $r_{\rm ds} = 100$ kΩ and $T = 300$°K, $v_{\rm no}$, with I_B will be equal to 128 nV/$\sqrt{\rm Hz}$, and $v_{\rm no}$ without I_B or R_B will be equal to 103 nV/$\sqrt{\rm Hz}$. This corresponds to about 1.9 dB losses in signal-to-noise ratio (SNR). Therefore, to minimize I_n^2, v_x cannot be too small. As a result, there is a slight tradeoff between the supply voltage and the noise performance.

Nevertheless, the proposed technique can be used for interfacing circuits that require higher supply voltage. This is possible since there is no limit on the voltage range at the input of the resistor, except the limit posed by the input protection diodes in the ESD structure. However, these diodes can be omitted if necessary. To keep the quiescent output voltage at $V_{\rm DD}/2$, proper values for the current source I_B or the resistor R_B need to be re-determined for the new quiescent input voltage.

If a bulk-driven differential pair is used as an input stage for an opamp [8], v_x can be set at $V_{\rm DD}/2$ and analog circuits based on inverting opamp configuration, such as active *RC* filters can be realized even at 1 V. However, analog circuits that require switches such as THA's amplifiers are still not realizable using this type of opamp, with v_x set to $V_{\rm DD}/2$. This is due to the fact that voltage signal at the mid-range of the supply voltage cannot pass through the switches [10]. In general, critical switches for passing voltage signals must be avoided in low-voltage design. If the proposed technique is used, nMOS switches can be added to the opamp negative input at three possible locations as shown in Fig. 3. In this case, the switches are not used to pass large voltage signals but for passing current signals. For a given current, the switches (except for the switch S_3, which only affects the settling time of the circuit) need to be sized such that the voltage drops across the switches are minimized. If the sizes of the switches are selected appropriately, the drain voltages and the source voltages of the switches are approximately equal to v_x, which is only 1 $V_{\rm DSsat}$ from ground. Therefore, the switches will have sufficient overdrive voltages $V_{\rm ov}$, which is given by

$$V_{\rm ov} = V_{\rm DD} - V_{tn} - v_x. \quad (7)$$

For a 1-V supply, the overdrive voltage is between 0.2 V and 0.3 V for $V_{tn} \approx 0.6$ V. Using these current switches, analog circuits such as DAC's and THA's can be realized at low supply voltage as discussed in Sections IV and V.

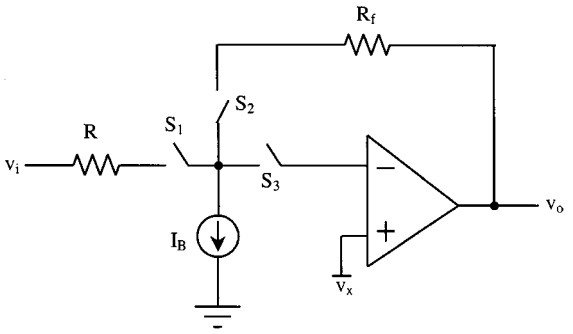

Fig. 3. Possible switch locations.

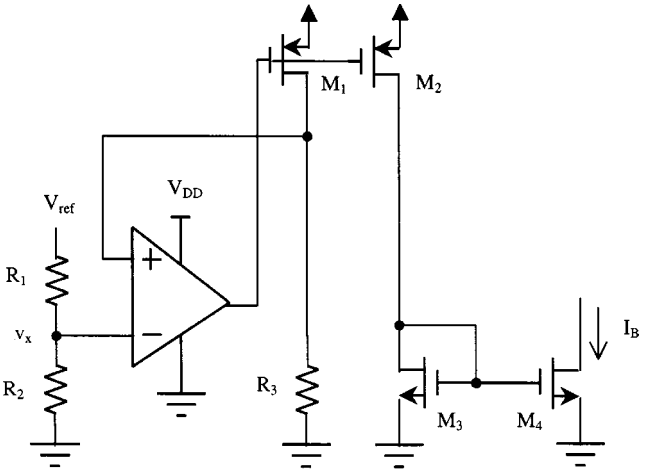

Fig. 4. Biasing circuit for generating I_B.

III. Biasing Current Generation

In the proposed technique, a current source or a resistor is required to allow the opamp input common-mode voltage set to v_x. As long as v_x is generated from a reference voltage, the proposed technique that uses resistor for biasing the opamp will track with process variations as indicated in (2). However, the technique that uses current source for biasing the opamp requires a biasing circuit for generating I_B (Fig. 4) that can track with variations on the resistor values. Assume that a reference voltage $V_{\rm ref}$ is available. The required voltage v_x can be generated using a resistor divider R_1 and R_2. Due to the feedback loop consisting of the opamp and M_1, the positive input of the opamp is equal to v_x and the drain current of M_1 is equal to v_x/R_3. Assume that M_1 matches M_2 and M_3 matches M_4, the biasing current I_B is therefore equal to $V_{\rm ref} \times R_2/R_3/(R_1 + R_2)$. As a result, I_B will track with variations on resistor values.

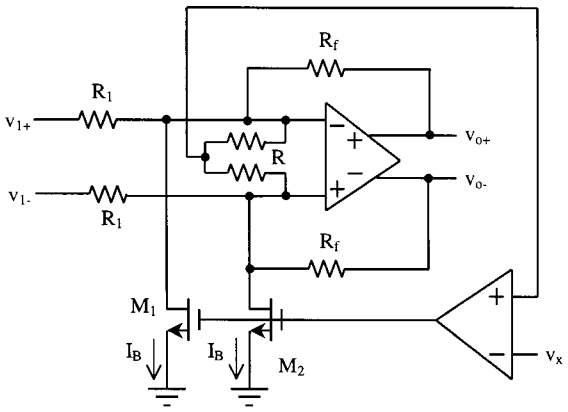

Fig. 5. I_B generation using input common-mode feedback.

For fully differential inverting opamp configurations, the same biasing circuit shown in Fig. 4 can also be used for generating the required I_B's if the input common-mode voltage is held at a constant value, and the output common-mode voltage is fixed by the fully differential opamp. If the input common-mode voltage can vary significantly, the biasing current I_B's are required to change according to the input common-mode voltage such that the opamp input common-mode voltage is limited within the input common-mode range. Therefore, a common-mode feedback circuit is required at the opamp inputs, as shown in Fig. 5. Resistors (R's) are used to detect the opamp input common-mode voltage, which is compared with the desired value v_x using a single-ended opamp or a simple differential stage. Due to the feedback loop consisting of the single-ended opamps, M_1 and M_2, the opamp input common-mode voltage will be held at v_x and the biasing currents I_B's will be set according to R_1, R_f and the input and output common-mode voltages. As a result, the proposed input common-mode circuit not only allows the inverting opamp configuration tracked with process variations, but also allows the circuit to be useful for interfacing other circuits, which may require higher supply voltages, without coupling capacitors. The range of the input common-mode voltage for the circuit shown in Fig. 5 is determined by the values of the resistors R_1's and R_f's and the W/L ratios of M_1 and M_2. From simulation results, an input common-mode voltage range between -0.5 and 10 V can be achieved for $v_x = 100$ mV, $V_{\rm DD} = 1$ V, $R_1 = R_f = 20$ kΩ and $(W/L)_1 = (W/L)_2 = 100/1.2$. The designs of the single-ended opamp and the fully differential opamp are discussed in Sections IV and VI.

IV. 1-V DAC Design

In the literature, different techniques have been proposed to implement DAC's, including the use of resistor strings, switched-capacitor techniques, current-mode approaches, and R-2R techniques [14]. If current-mode approaches are to be used, a cascode current source is usually required in each DAC cell to increase the output resistance. Due to the limited area for each DAC cell in a thermometer code DAC, relatively small transistors have to be used for the cascode current sources and hence, a small output signal swing will result. For other DAC techniques except R-2R techniques, voltage switches are usually required. Unless the signal swing is limited, the switches will not have sufficient overdrive voltage for low supply voltage. Although switched-opamp techniques can be used for designing low-voltage DAC's, the output of the opamp has to be switched to one of the supply rails during one of the clock phases. Hence, the output of the DAC is only valid at one clock phase.

To design a low-voltage DAC, a conventional R-2R DAC design can be converted into a low-voltage design by applying the proposed technique discussed in Section II. A 10-bit DAC architecture is shown in Fig. 6. In this design, the biasing scheme that uses current source is adapted. Although a fully differential DAC can be designed based on the structure shown in Fig. 5, two single-ended opamps are used to simplify the generation of I_B's. Since the switches are connected between the resistors and the opamp negative input terminals, they are used for passing current signals and will have sufficient overdrive voltage as discussed before. The sizes of the switches are scaled to accommodate different resistor current levels to minimize the overall DAC nonlinearity. To relax the matching requirement of the resistors and to minimize the magnitude of glitches, the two most significant bit (MSB) resistors are realized in one segment from three equal resistors using thermometer coding.

When the input digital code is 1000000000, the positive output voltage V_{o+} is desired to be at $V_{\rm DD}/2$. For the input digital code equal to 1111111111 and 0000000000, V_{o+} is desired to be close to rail-to-rail (0.9 V and 0.1 V, respectively). Based on these requirements, all resistor values can be found, and I_B's can be determined using (1) if $V_{\rm ref}, v_x$ and R_f are given. In this design, they were chosen to be 1 V, 50 mV, and 20 kΩ, respectively.

The design of the opamps that are used in the DAC is shown in Fig. 7. It is a two-stage architecture that consists of a pMOS differential pair, a low-voltage current mirror and a common source second stage as discussed in [15]. The output voltage can have a large signal swing close to rail-to-rail (from $V_{\rm DSsat}$ to $V_{\rm DD} - V_{\rm SDsat}$). Since the opamp is required to drive resistive load, the second stage does not have a large voltage gain. Thus, most of the gain has to be provided by the first stage. The opamp was designed based on a conventional 1.2-$= \mu$m CMOS process. The unity-gain bandwidth was simulated to be 10 MHz with a dc gain of about 60 dB for a 20 pF capacitance load and a 10 kΩ resistive load. The power consumption for a 1-V supply and the settling time for 0.1% accuracy are about 150 $= \mu$W and 120 ns, respectively.

V. 1-V Track-and-Hold Amplifier Design

In general, THA's can be implemented based on either an open-loop architecture, a closed-loop architecture, or using switched-capacitor techniques. For low supply voltage, the main challenge is again the design of switches and amplifiers. As a result, these architectures may not be suitable for a low-voltage (1 V) supply. Fig. 8 shows the architectures of the two proposed 1-V THA's. The first scheme is a direct conversion of a traditional THA (found in many texts, e.g., in [14]) into a low-voltage design using the proposed technique

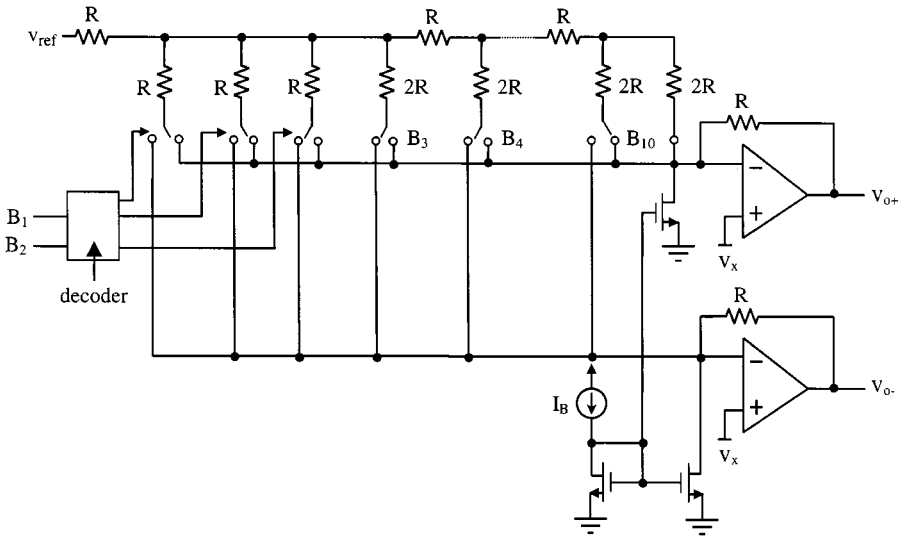

Fig. 6. Proposed 1-V 10-bit DAC architecture.

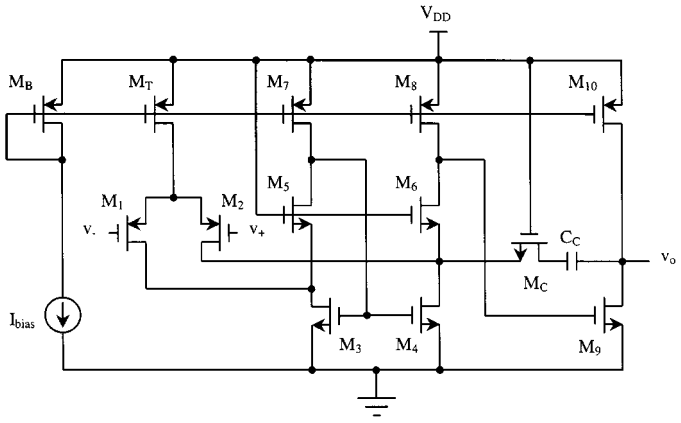

Fig. 7. Single-ended 1-V opamp design.

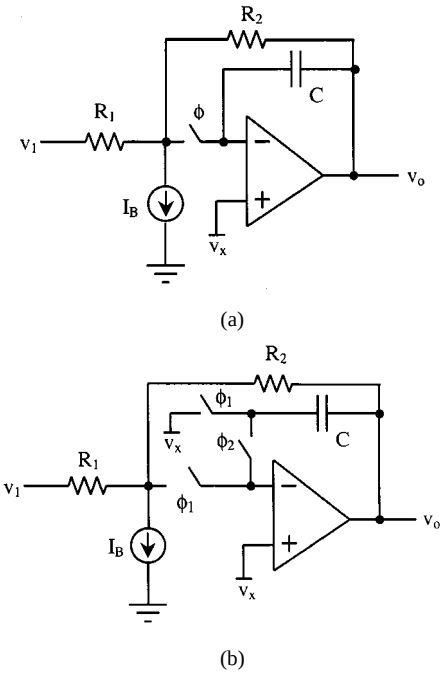

Fig. 8. Proposed 1-V single-ended THA architectures.

outlined in Section II. A biasing scheme that uses current source is adapted. The switch is again used only for passing current signal. Since the drain voltage and source voltage of the switch is always at about v_x, it has adequate overdrive voltage and the charge injection is not very signal dependent. During track mode, the THA behaves like a low-pass filter with the -3 dB frequency at about $1/[(R_2R_S/R_1 + R_S + R_2)C]$, where R_S is the resistance of the switch. This limited bandwidth will lead to tracking error for an input signal with frequencies close to the -3 dB frequency. Therefore, for fast tracking, small R_2, R_S and C are needed. However, using a small R_2 would be a problem since the opamp must be able to drive it. Using a very small capacitor would cause large charge injection and increase the kT/C noise. Furthermore, increasing the size of the switch will increase the charge injection. Hence, optimum values for these components must be chosen based upon the application requirement and the opamp driving capability. In the prototype design, the size of the switch and the values of the resistors and the capacitor were chosen to be 21.6/1.2, 20 kΩ and 1.5 pF, respectively.

Scheme 2, shown in Fig. 8(b), is proposed to reduce the tracking error. The THA tracks the input during ϕ_1. When ϕ_2 turns high, the THA is in the hold mode. During track mode, the THA operates as an inverting amplifier with unity gain, and the capacitor C is acting as a load to the opamp. In this case, the -3 dB frequency is approximately equal to $f_t/(1 + R_2/R_1)$ where f_t is the unity gain bandwidth of the opamp. Therefore, the bandwidth of scheme 2 will be higher than that of scheme 1 for large C and the tracking error will be minimized. Since the drain and source voltages of all the switches in scheme 2 are always at about v_x (similar to scheme 1), charge injection generated from these switches are almost signal independent and only offset voltage (including the offset of the opamp) is produced at the output. Converting the proposed THA's shown in Fig. 8 into fully differential implementations, as shown in Fig. 9, can minimize the offset error due to charge injection. However, a fully differential opamp is required.

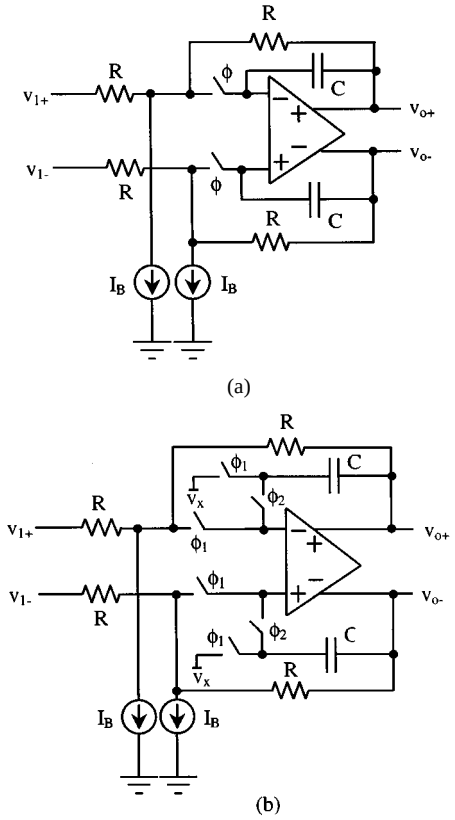

Fig. 9. Proposed 1-V fully differential THA architectures.

VI. Fully Differential Opamp Design

Fig. 10(a) and (b) show the architecture of the 1-V fully differential opamp [15] and its corresponding common mode feedback (CMFB) circuit. The opamp is again a two-stage design that consists of a folded cascode input stage, a common source output stage and a continuous time CMFB. Although dynamic CMFB circuits have been proposed for implementing switched-opamp circuits [13], a continuous time CMFB circuit has to be used for the proposed THA schemes since the opamps used in the THA's are not switched-opamps, and the outputs of the opamps have to be valid for the entire clock cycle.

The proposed CMFB circuit is similar to a transimpedence amplifier. It does not need a differential pair, which is a common choice [13], [15] for comparing the common-mode voltage with the desired value. As shown in Fig. 10(b), two resistors with values equal to $2R$ are used to sense the output common mode voltage and produce a current i_1. This current is compared with i_2, which is set by the desired common-mode voltage $(V_{\rm DD}/2)$ and the resistor R. The difference between i_1 and i_2 is then converted into a control voltage labeled as CMFB by transistors M_{11}, M_{12} and M_{13}. The control voltage will then be used to adjust the $V_{\rm GS}$'s of M_3 and M_4, such that the output common-mode voltage is stabilized to about $V_{\rm DD}/2$. The proposed CMFB circuit has advantages of allowing rail-to-rail output swing. Furthermore, it does not need any level shift or attenuation on the common mode signal, unlike other continuous time CMFB circuits that use differential pairs [15]. Simulation results of the fully differential opamp show a unity gain frequency of 9 MHz and a dc gain of over 60 dB for a capacitance load of 20 pF and a resistive load of 20 kΩ. The opamp consumes about 250 μW at 1 V.

VII. Implementation and Experimental Results

The proposed 10-bit DAC and the THA's were implemented in a conventional 1.2-μm CMOS process with $V_{tn} \approx 0.6$ V and $V_{\rm tp} \approx -0.8$ V. Two THA schemes for both single-ended and fully differential were implemented. The resistors were realized using polysilicon, which has a sheet resistance of $\approx$30 Ω/square. The die photos of the DAC and the THA's are shown in Figs. 11 and 12, respectively. The DAC has an active area of 0.6×1.1 mm^2 and the total active area for the four THAs is equal to 1.2×0.8 mm^2.

The DAC has a single-ended output swing approximately between 0.1 V and 0.9 V (close to rail-to-rail) after $V_{\rm ref}, v_x$ and I_B are set approximately to 1 V, 50 mV, and 70 μA, respectively. The total power dissipation, including all the biasing currents and all the digital circuits, was measured to be less than 0.45 mW at 1 V for a throughput of 1 MS/s. When the digital input was switched from its minimum value to its maximum value and vice versa, the worst-case settling time with a loading capacitance of approximately 20 pF was measured (single-ended output) and found to be less than 1 μ,s as shown in Fig. 13. The settling time for the DAC is limited by the opamp finite gain bandwidth product and slew rate limit. The DNL and INL were measured as shown in Fig. 14. The maximum DNL and INL are 1.7 LSB's and 3.0 LSB's, respectively. Fig. 15 shows the output spectrum of the DAC sampling a 1 kHz digital sinusoidal input signal at a rate of 500 kS/s. The SNDR was measured to be 48.3 dB. The nonlinearity is mainly caused by resistor mismatch. When the supply voltage is set to 0.9 V, the DAC still operates properly with a lower output swing after proper adjustments made on $V_{\rm ref}$ and I_B.

All the four THA's were measured with a 1-V supply and a loading capacitance of 20 pF. Figs. 16 and 17 show the measured output waveforms for the single-ended and the fully differential implementation of scheme 2, respectively. For the first figure, the input frequency $f_{\rm in}$ is 50 kHz and the sampling frequency f_S is 500 kHz. For the second figure, $f_{\rm in}$ and f_S are 100 kHz and 1 MHz, respectively. The THD's during track mode for all different THA's are measured to be less than -67 dB for input less than 50 kHz with peak-to-peak value $V_{\rm p\text{-}p}$ of 600 mV (single-ended). High linearity is achieved due to the use of the poly resistors. When $V_{\rm p\text{-}p}$ is increased to 700 mV (single-ended), the track mode THD's for all the THA's are less than -60 dB. During hold mode, the two single-ended implementations gave an offset of about 10 mV due mainly to charge injection generated from the switches. This offset is minimized in the fully differential implementations. After comparing the performance of all four THA's, the fully differential THA using scheme 2 gave the best results in terms of track-and-hold mode THD and tracking error. Fig. 18 shows the THD versus peak-to-peak output swing for the fully differential THA using scheme 2. Its performance is also summarized in Table I. Since the opamps were designed for driving external capacitive load, the unity-gain frequencies of the opamps were limited. If the THA's were to be used on chip along with an analog-to-digital

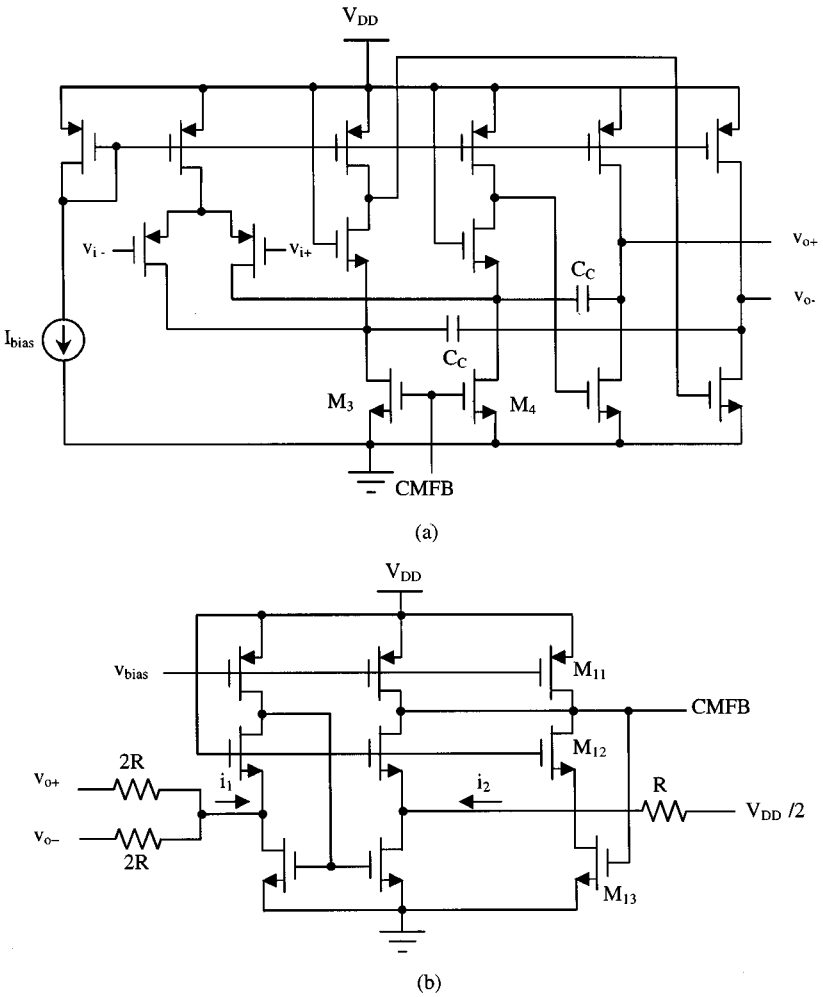

Fig. 10. (a) Fully differential 1-V opamp design. (b) Proposed continuous CMFB circuit.

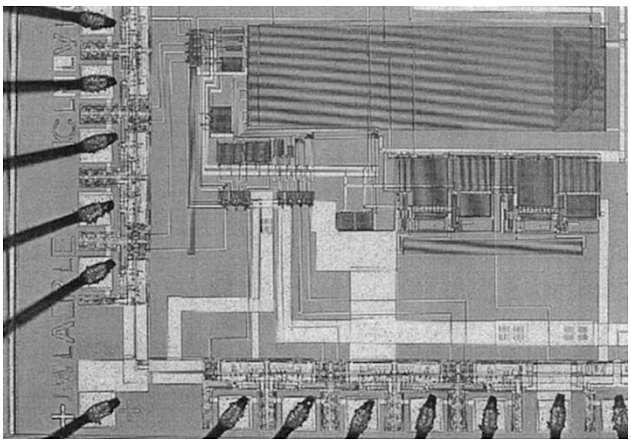

Fig. 11. Die photo for the 1-V DAC.

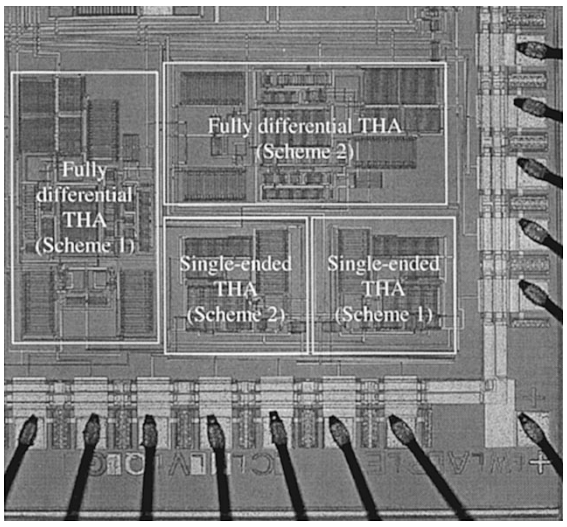

Fig. 12. Die photo for the four 1-V THA's.

converter (ADC) so that the capacitive load is less, then a higher sampling rate can be expected.

VIII. Conclusion

In this paper, a technique for converting analog circuits that utilizes inverting opamp configurations into low-voltage designs is proposed. To minimize the supply voltage, a current source or a resistor is introduced between the opamp negative input terminal and one of the supply rails so that the opamp input common-mode voltage can be set close to one of the supply rails, independent of the quiescent input and output voltages. Based on this technique, an opamp with limited

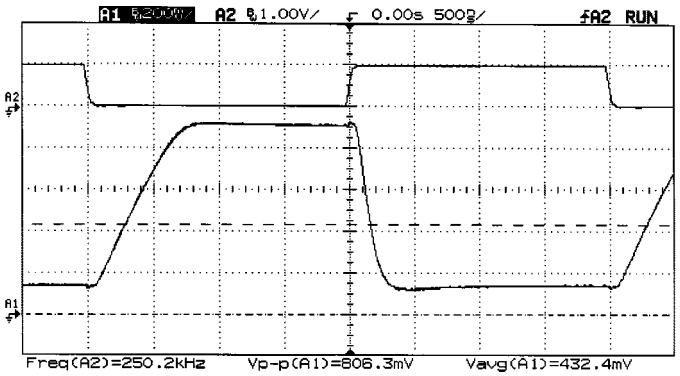

Fig. 13. DAC transient response for (upper) digital input values and (lower) DAC output.

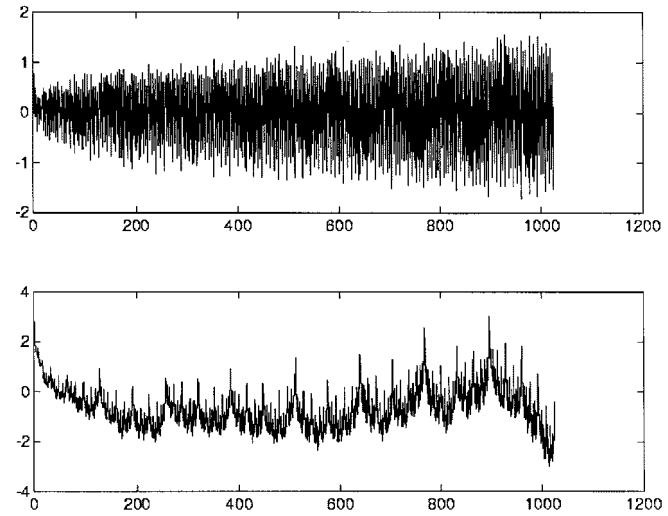

Fig. 14. Measured (upper) DNL and (lower) INL for the 1-V DAC.

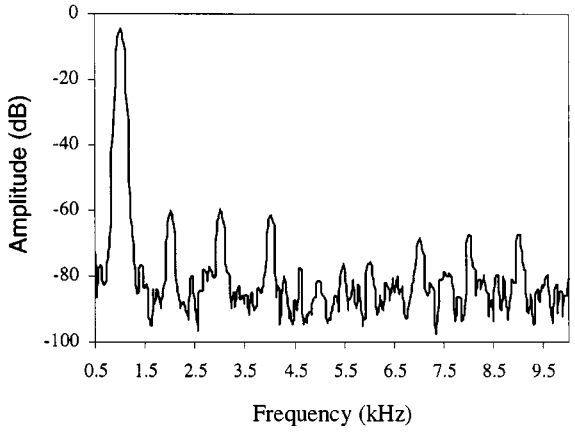

Fig. 15. Output spectrum of the DAC for a 1-kHz digital sinusoidal input signal.

input common-mode range can be used for low-voltage design. Furthermore, low-voltage analog circuits such as low-voltage continuous time active *RC* filters can be realized without the need for a specialized process or using bulk driven MOSFET's. The minimum supply voltage for the proposed technique is approximately equal to $3V_{\mathrm{DSsat}} + V_t$. For analog circuits that require switches, switches for passing current signals can be incorporated into the proposed technique by placing the

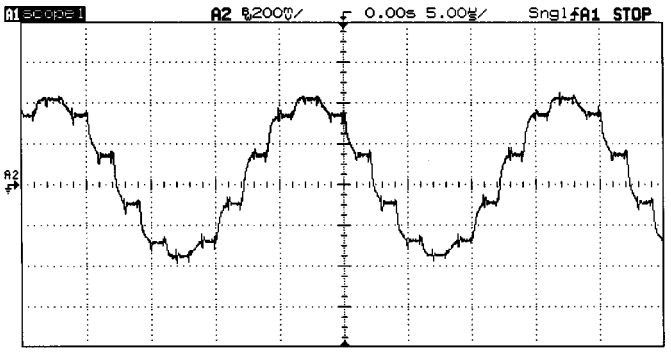

Fig. 16. Output waveform of the single-ended THA (scheme 2) at $f_s = 500$ kHz and $f_{\mathrm{in}} = 50$ kHz.

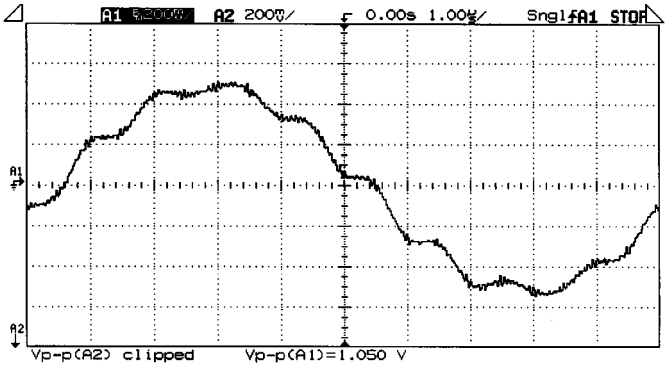

Fig. 17. Differential output waveform of the differential THA (scheme 2) at $f_s = 1$ MHz and $f_{\mathrm{in}} = 100$ kHz.

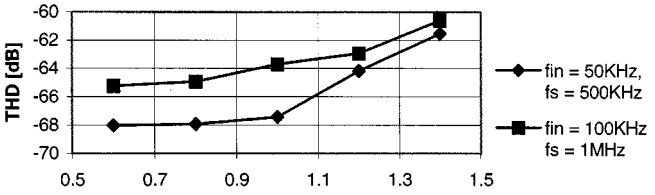

Fig. 18. Track-and-hold mode THD versus differential output swing.

TABLE I
PERFORMANCE SUMMARY FOR THE 1-V DIFFERENTIAL THA USING SCHEME 2 TECHNOLOGY

Technology	1.2 µm CMOS process ($V_{tn} \approx 0.6$ V and $V_{tp} \approx -0.8$ V)
THD (Track mode)	< -70 dB @ f_{in} = 100 kHz, V_{out} = 1.2 Vp-p
THD (Track-and-hold mode)	-61 dB @ f_{in} = 100 kHz, V_{out} = 1.4 Vp-p, f_S = 1 MHz
Droop Rate	2 mV/µs
Maximum Tracking Error	< 5 mV
Slew Rate	0.3 V/µs
Supply Voltage	1 V
Power Dissipation	< 350 µW
Active Area	430×220 µm^2

switches at the opamp negative input terminal. At this location, the switches will have sufficient overdrive voltages. Therefore, critical voltage switches can be avoided. It should be mentioned that although the proposed technique can be applied to design many useful low-voltage analog circuits, it cannot be used directly to replace switched-opamp or switched-capacitor class of circuits since some circuits may be more effective to be realized using these techniques.

To demonstrate the proposed technique, a 10-bit DAC and four THA's were implemented in a conventional 1.2-μm CMOS

process with $V_{tn} \approx 0.6$ V and $V_{\rm tp} \approx -0.8$ V. The designs are capable of operating at a very low voltage (1 V) with low power consumption (<0.45 mW for the DAC and <0.35 mW for each THA). The designs also have a wide input and output signal swings close to rail-to-rail. From the experimental results, the DAC has a maximum DNL of 1.7 LSB's, a maximum INL of 3.0 LSB's, a SNDR of 48.3 dB, and a maximum throughput of 1 MS/s for an output swing between 0.1 V and 0.9 V. The fully differential THA using scheme 2 shows to have a track-and-hold mode THD of less than -61 dB at a sampling frequency of 1 MHz for an input signal frequency of less than 100 kHz with a differential output signal swing of 1.4 $V_{\rm p\text{-}p}$.

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REFERENCES

[1] A. Chandrakasan, S. Sheng, and R. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 27, pp. 473–484, Apr. 1992.

[2] B. Davari, R. Dennard, and G. Shahidi, "CMOS scaling for high performance and low power—The next ten years," *Proc. IEEE*, vol. 83, pp. 595–606, Apr. 1995.

[3] Y. Matsuya and J. Yamada, "1 V power supply, 384 kS/s 10 b A/D and D/A converters with swing-suppression noise shaping," in *1994 IEEE ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 192–193.

[4] S. Bazarjani, M. Snelgrove, and T. MacElwee, "A 1 V switched-capacitor $\Sigma\Delta$ modultor," in *1995 IEEE Symp. Low Power Electronics, Dig. Tech. Papers*, Apr. 1995, pp. 70–71.

[5] E. Peeters, M. Steyaert, and W. Sansen, "Afully differential 1.5 V low-power CMOS operational amplifier with a rail-to-rail current regulated constant-g_m input stage," *Proc. IEEE CICC*, pp. 75–78, 1996.

[6] J. Duque-Carillo, R. Perez-Aloe, and J. Valverde, "Biasing circuit for high input swing operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 30, pp. 156–159, Feb. 1995.

[7] G. Ferri and W. Sansen, "A rail-to-rail constant-g_m low-voltage CMOS operational transconductance amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1563–1567, Oct. 1997.

[8] B. Blalock, P. Allen, and G. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst.s II* , vol. 45, pp. 769–780, July 1998.

[9] R. Griffith, R. Vyne, R. Dotson, and T. Petty, "A 1-V BiCMOS rail-to-rail amplifier with n-channel depletion mode input stage," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2012–2022, Dec. 1997.

[10] A. Baschirotto and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1979–1986, Dec. 1997.

[11] J. Crols and M. Steyaert, "Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, pp. 936–942, Aug. 1994.

[12] A. Baschirotto, "A 40 MHz CMOS sample & hold operating at 1.2 V," in *Proc. 24th ESSCIRC*, Sept. 1998, pp. 248–251.

[13] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900 mV 40 μW switched-opamp $\Sigma\Delta$ modulator with 77 dB dynamic range," in *1998 IEEE ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 68–69.

[14] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley , 1997.

[15] R. Castello, F. Montecchi, and A. Baschirotto, "Low-voltage analog filters," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 827–840, 1995.

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