2016 Analog IC Design Homework 3 ***due date: 05/05/2016***

1. Design a differential amplifier as shown in Fig. 1. (50%)
   (a) With V_{DD} = 1.8V and I_d (M_3) = 20uA, design the W/L sizes of M_1 ~ M_3 and R_D and the dc bias V_b to get the voltage gain $|A_v| = V_{out}/(V_{in}+ - V_{in}-) > 20dB$ with $V_{in}+(DC) = V_{in}-(DC) = 0.9V$. (10%)
   (b) Use the design in (a) and make width of M_2 10% larger than M_1. Plot the frequency response of common-mode voltage gain $A_{cm} = V_{out}/(V_{in}+=V_{in}-)$ and find CMRR(A_v/A_{cm}), with and without adding C_P = 100fF from P to ground. Comments the correlation between CMRR bandwidth and C_P. (10%)
   (c) Use the design in (a), simulate and find the input common-mode range(ICMR) with $|A_v|$>20dB, (all MOS devices operate in saturation region). (10%)
   (d) Use the design in (a), simulate and find the input differential range with $|A_v|$>20dB, (all MOS devices operate in saturation region). (10%)
   (e) Use the design in (a), and stimulate the circuit to get the voltage gain under TT, FF, SS corner. Then use current mirror to generate the V_b voltage, then run the corner stimulation under TT, FF, SS. Comment the difference between using ideal voltage source and current mirror. (10%)

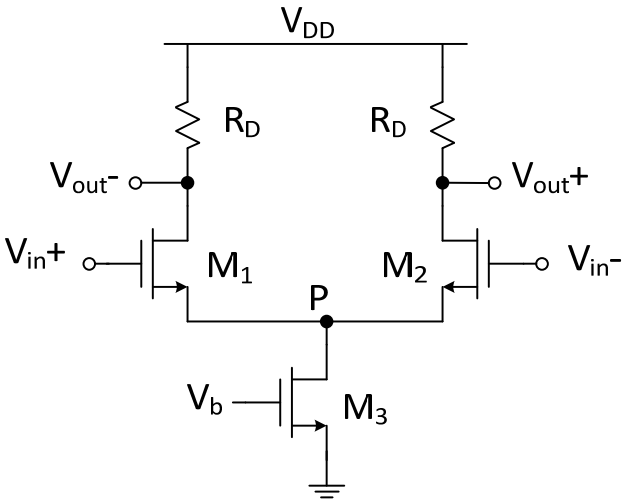

Fig. 1

2. Design a 1:4 wide-swing cascade current source as shown in Fig. 2(a). (50%)
   (a) With I_{ref} = 4uA (I_{out} = 16uA), design the W/L sizes of M_1 ~ M_4, and the dc bias V_b to get a minimum operational voltage at V_{out} < 300mV and R_{out} > 600kΩ. (10%)
   (b) Use the circuit structure as shown in Fig. 2(b) as a reference to design a bias generation circuit of V_b. Please calculate the size of M_5 and write down your calculation in the report. (10%)
   (c) Stimulate the circuit with the size of M_5 in (b) and check if the V_b is close to the value you want. Run the corner simulations with SS, TT, and FF to make sure $V_{out.min}$ < 300mV and comment the difference with using ideal voltage source as the bias. (10%)
   (d) State the M_5's and M_6's operation region and show in hand calculation. (10%)
   (e) Show the DC voltage of V_{IN1} in terms of V_{ov} and V_t. (10%)

by CCHsieh

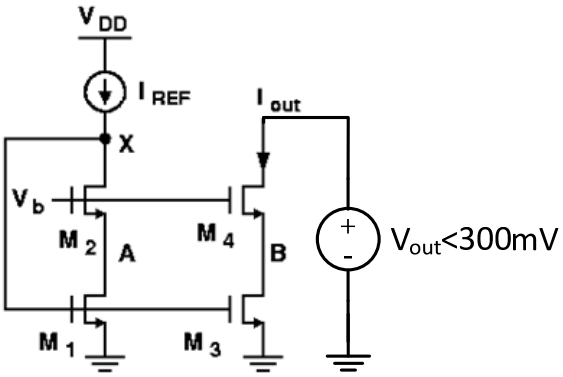

Fig. 2(a)

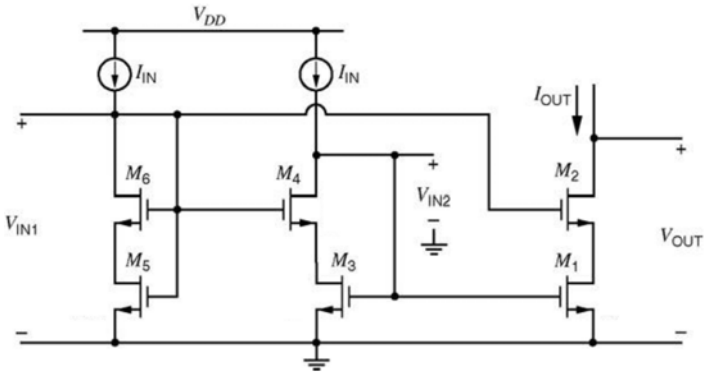

Fig. 2(b)

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***