2016 Analog IC Design Homework 1 ***due date: 03/24/2016***

1. Use composer and hsipce to simulate the capacitance characteristic of nMOS as shown in Fig. 1 with body connected to gnd=0V. (30%)
   (a) Assume the W/L = 5*10um/0.5um, V_G = ~~0V ~ 3.6V~~ -3.6V～3.6V (use CIC 0.18um hspice model). (10%)
   (b) Modify the W/L =50um/0.5um, redo the simulation and plot, comments the capacitance difference compared to (a). (10%)
   (c) Modify the W/L =5um/5um, redo the simulation and plot, comments the capacitance difference compared to (a) and (b). (10%)

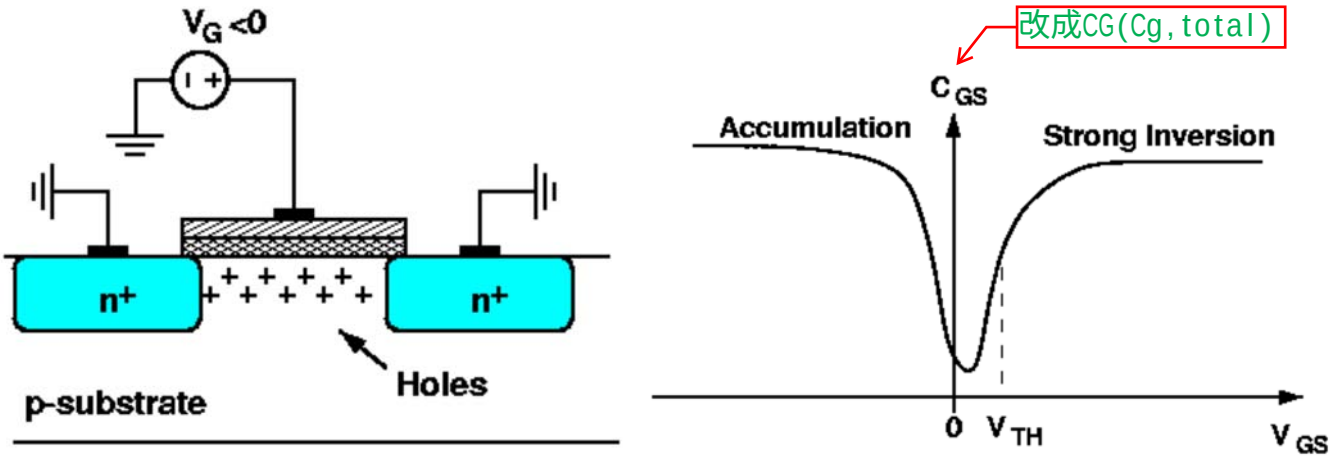

Fig. 1.

2. A source follower as shown in Fig. 2 has V_{DD} = 1.8V, V_{in} = 0 ~ 1.8V, W/L (M_1) = 5um / 0.5um, and I_1 = 5uA. (40%) 1/2Vout的slope
   (a) Use composer and hspice to simulate and plot the voltage transfer curve V_{in} vs. V_{out}. Find the linear range, the slope, and DC offset of this source follower. (10%)
   (b) Change the body of M_1 connected to source node and redo the simulation and plot, Find the linear range, the slope, DC offset and comments the difference compared to (a). (10%)
   (c) Use the circuit in (a) and modify the current I_1 to 500uA, Find the linear range, the slope, DC offset and comments the difference compared to (a). (10%)
   (d) Use the circuit in (a) and modify the W/L (M1) = 50um / 0.5um, Find the linear range, the slope, DC offset and comments the difference compared to (a). (10%)

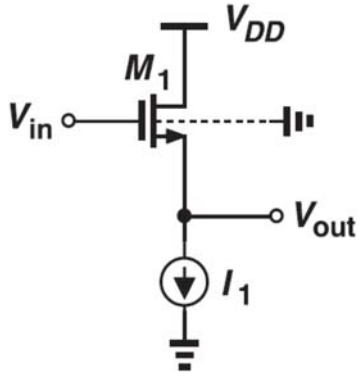

Fig. 2.

※To define the linear range, please find Vout at Vin=1.8V. Set the slope of 1/2 Vout as the reference point to find the range of Vin within 0.5% slope variation of Vout.

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3. Choose two nMOSs (1.8V devices) with W/L = 2um/0.2um and W/L = 2um/2um. Use HSPICE DC sweep analysis to show the I_D-V_{DS} characteristic waveforms with V_{GS} = 0, 0.3, 0.6, 0.9, 1.2, 1.5 and 1.8V as shown in Fig. 3. Comment the characteristics difference between long-channel and short-channel devices. (10%)

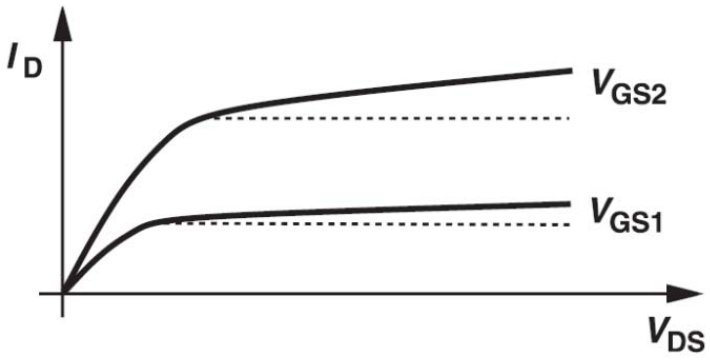

Fig. 3.

4. Choose an nMOSs (1.8V devices) with W/L = 3um/0.5um. Assume V_S = 0V, V_D = 0.3V, V_G = 0V ~ 3.6V. Use HSPICE DC sweep analysis to show the V_{GS}-C_{GS} and V_{GS}-C_{GD} characteristic waveforms as shown in Fig. 4. Comment the characteristics of the waveform. (10%)

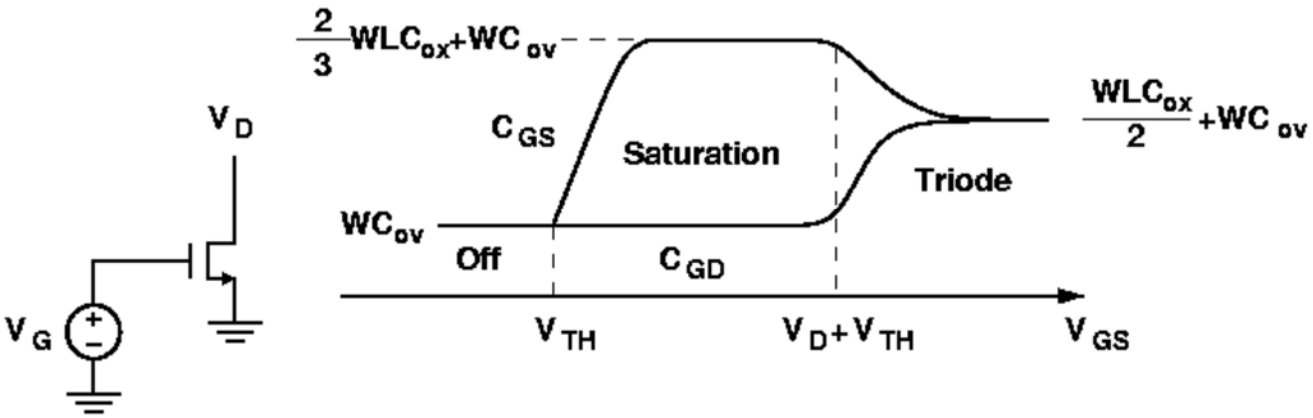

Fig. 4.

5. Choose a nMOSs (1.8V devices) with W/L = 0.5um/0.2um. Assume V_S = 1V, and V_G = 0V ~ 1.8V. Use HSPICE DC sweep analysis to show the V_G-R_{on} characteristic waveforms as shown in Fig. 5. Comment the characteristics of the waveform. (10%)

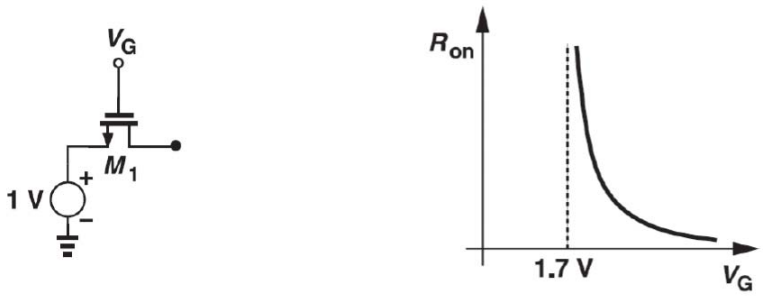

Fig. 5.

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***

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