

Composer Tutorial

Outline

•Full custom IC Design Flow

 Composer Tutorial Making library and cells Drawing schematics –an inverter example Opening existing cells Creating symbol

Full Custom IC Design Flow

Circuit Netlist/ Schematic

Pre-layout simulation

Layout

DRC, LVS

Parasitic Extraction

Post-layout simulation

Composer, Text Editor

Hspice, Spectre, Eldo...

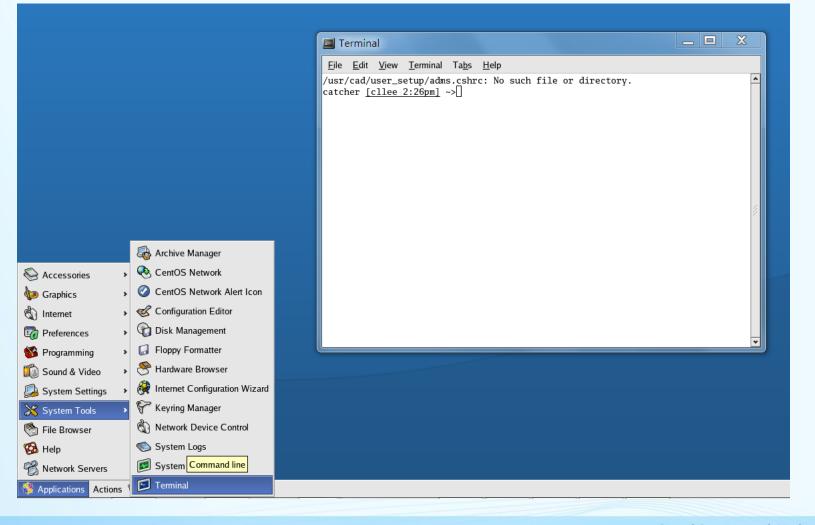
Virtuoso, Laker

Calibre

Calibre

Hspice, Spectre, Eldo...

Open the Terminal Environment



Start Cadence Environment

Invoking *icfb* & in terminal

bigbird:~(m9761571)% bigbird:~(m9761571)%telnet ws2 Trying 140.114.24.112...

[m9761571@ws2 ~]\$ mkdir vlsi_composer [m9761571@ws2 ~]\$ cd vlsi_composer/ [m9761571@ws2 ~/vlsi_composer]\$ icfb &



Main Window

After successfully checking license, the main window shows

	Í		icfb + Log: /home/users3/ydwu/CDS3og	*	7	
	File	Tools	Options		Help	1
1111	/ / / /		WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.			 7
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>						

Making library

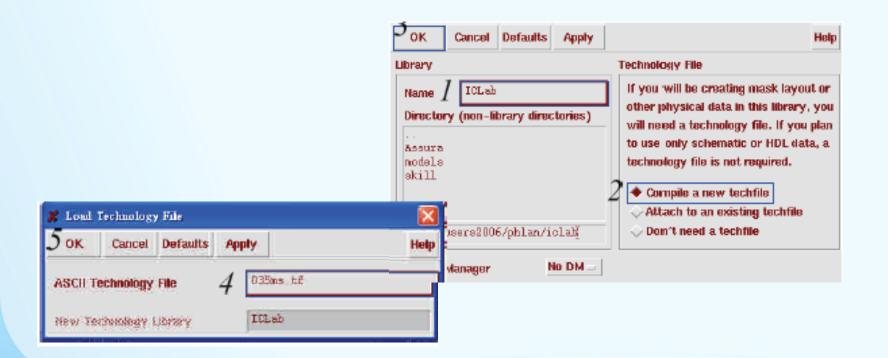
From main window, $File \rightarrow New \rightarrow Library...$ A new window called *New Library* pops up

File Tools Option:		Help 1
New 1	Library le - "/usc/mentor/modelsim_ss/cuc/shared/pkgs/icv/tools/queryskl/	4
Open 📕	Cellviewding file - 'calibre.skl"	nge_ear
Import		IV
Export	×	E2
Refresh		
¹ Make Read Only	M: R:	
Close Data		

# New Sibrary			
OK Cancel Defaults Apply	Help		
Library	Technology File		
Name Directory (nen-library directories) Assura nodels skill	 If you will be creating mask layout or other physical data in this library, you will need a technology file. If you plan to use only schematic or HDL data, a technology file is not required. Compile a new techfile Attack to an existing techfile 		
/boas/users2006/phlan/iclab	Don't need a techfile		

Making Libraries

Enter the library name in the *Name* field If you have techfile (018ms.tf), you can choose the option of *Compile a new techfile* option, and press *OK.* or , you choose the option "*Don't need a techfile*".



Making Cells

From main window, *File* \rightarrow *New* \rightarrow *Cellview...* Choose the Library at which the cell is created Enter the desired name in the *Cell Name* field (nand2) Choose *Composer-Schematic* in the Tool field Press *OK*

				5 ок	Cancel D	efaults	Help
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File Tools Options			Help 1	Cell Name			
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VerilogA-Editor VerilogAMS-Editor

Virtuoso

Create New File

Schematic Editing Window

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Inserting Symbols

Press key "i" or the instance button from ↓ the toolbar
Press "*Browse*" from the popped window
Pick the desired cell from library manager
Choose *symbol* view for schematic editing, and press *close*analogLib → nmos4 → symbol

Hide Cancel Defaults Help Library	X Add I	nstance			Chevrol Reporter - and Common		
renoy nows a country a starting to the startin	Hide Library Cell	Cancel	Defaults	1	WARDEN.	Jacob.	eyetal.
Rotate Sideways Upside Down			Rows ¹	4 Upside Down		Ann Ann Ann Ann	-

Editing Properties of Symbol

After closing the library manager, the corresponding library and cell name appears in the popped window Fill some properties for the symbol

Name: Mn Model Name: nch Multiplier: 1 Width: 0.5u Length:0.18u

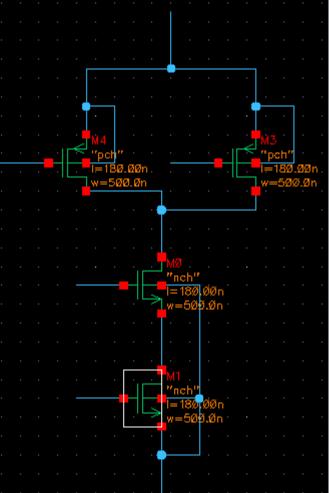
Press Hide Button

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Adding and Connecting

Insert nmos4, pmos4, symbols from the analogLib library

nmos4: 0.5u/0/18u/1 pmos4: 0.5u/0.18u/1 vdc: DC voltage=3.3V gnd Press key "**w**"to place wire

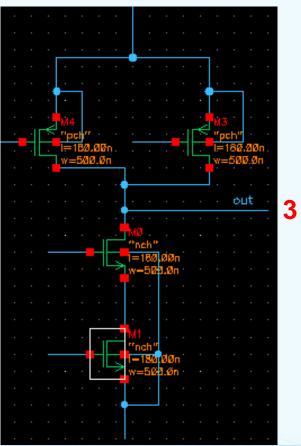


Adding Net Names

Press key "I"(Label) and keyin the corresponding node name in the popped window

Press Hide and drag the "net name" to some wire/node

Hide Ca	uncel Defaults		Hel
Wire Name	Net Express	ion	
Names	1 out		
Font Height	0.0625	Bus Expans	sion 🔶 off 😓 on
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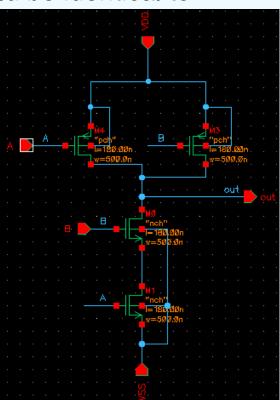
Indicating I/O Ports

Press key "**p**"or the pin button from the toolbar Specify the **Pin Name** and choose the **Direction** (input/output/bidirection)

If pin connect to some net, the pin name should be identical to net name to avoid confusion.

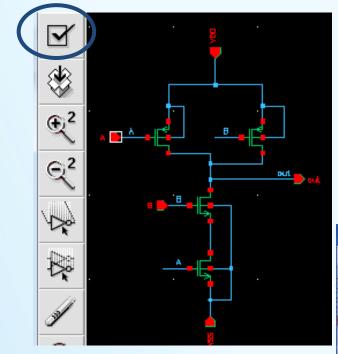
Press Hide and drag the pin to the right place

# Add Pa	ie.			8
4 Hilde	Cancel	Defaults		Help
Pin Names Direction Usage	3	and state and state	Contraction of the	n 🔶 ett 😞 on 🍝 single 🥪 multiple
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Saving the Schematic

Press key "**X**" or check and save button **I** from the toolbar To save the schematic and make sure schematic is error free The main window reports the status of schematic



🗶 icfa - Log: /home/user/2006/phin	a/CDS log			×
File Tools Options			Help	1
WARNING, dleExtractLayers was Loading off ext Loading layers ext Stracting 'inv schematic' Champtic check completed with 10Lah inv schematic' saved	?			
Schematic check completed wit	h no errors.			
acuse L: nouseAddPt()	M: schHiMpussPopUp()	R. Toggle Bray Mode		
Point at starting point for the route	r or snap to diamond using the 's' key.			

Open Existing Cell

From main window, choose *File* \rightarrow *Open* In the popped window, choose the *Library* and *Cell Name* you want Choose the desired *View Name*, and Press *OK*

File Tools Options		Hidip 1	
New Open Import Export	Layers was renamed to InEntractLayers et "Matio" Slated with no errors.		
Refresh Make Read Only Gose Data	p" saved. splated with no errors.]	Open File	x
Defragment Data Exits	N:	5 OK Cancel Defaults	Help
		Library Name hw1 2 Cell Names Cell Name nand④ PRBS Name schematic 4 Wiew Name schematic 4 Browse w1_1_FR4 hw1_2_PRBS hw1_3 hw1_3_P nand2 Mode edit ◇ read Library path file 3	

Creating Symbol

Open *nand2* schematic first From schematic editing window, $Design \rightarrow Create Cellview$

→ From Cellview...

Make sure that *Library* and *Cell Name* are correct. Choose *Composer-Symbol* and Press *OK*

Tools	Design Window Edit	Add			
	Check and Save	X			
2	Save (not needed)	S			
ab	Save As	^s		S Cellview From Cellview	
۱	Hierarchy		1	4 OK Cancel Defaults Apply Hel	p
€²	Create Cellview		From Cellview		
×.	New		From Pin List	Library Name hw1 Browse	
⊖²	Open		From Instance	Cell Name nandž 2	
\triangleleft	Discard Edits		1 400m	From View Name schematic - To View Name symbol	
IIIX	Make Read Only			Tool / Data Type3 Composer-Symbol 😑	
	Probe	- D		Display Cellview	
-1>->	Plot	Þ		Edit Options	
	Renumber Instances				

Defining I/O Ports

Another window pops up

The *I/O Pins* listed in the window accord with *Pins* that was inserted in Schematic Editing Window

You can decide the position of *Pins* on your own

Press OK if the I/O pins list is correct

Library Name	Cell Name View Name	
hwl	nand2į̇̃ symbolį̇̃	
Pin Specificatio	ns /	Attribute
Left Pins	A B <u>i</u>	List
Right Pins	outi	List
Top Pins	ADI	List
Bottom Pins	vsa	List
Exclude Inherita	ed Connection Pins:	_

Symbol Editing Window

Then, **Symbol Editing Window** pops up Input (output) ports lie at left (right) as previous page's setup

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Export Netlists (1/3)

$\textit{File} \rightarrow \textit{Export} \rightarrow \textit{CDL}...$

	🕱 icfb - Log: /home/m	197/m9761614	/CDS.log		
	File Tools Options			Help 1	
Ľ	New >	ined in lib	File '/home/m97/m9761614/cds.lib' for Lib 'lab3'.		$ \Delta $
	Open				
	Import >				
	Export D	EDIF 200			
μ	Refresh	EDIF 300			
	Make Read Only	PRFlatten	M: schHiMousePopUp() R: schHiReturn()		
L	Close Data	CDL			
1	Defragment Data 👂	DEF			
	Exit	LEF			
		Stream			
		CIF			
		Router			

Export Netlists (2/3)

Choose "Library Brower"

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					1					basic	hw1_2_	
Netlisting	Mode			Analog						cdsDefTechLiJ functional	hw1_2_PRBS hw1_3	
				Library	Browser					hw1	hw1_3_P	
								_		rfExamples rfLib	nand2 nand2_test	
Top Cell I	Name			nand2						wilchw3	_	
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								-14		Close	Filters	Help
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Export Netlists (3/3)

Specify output netlist name (.sp) View the generated netlist

Virtuoso?CDL Out	
OK Cancel Defaults App	ly Help
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	Library Browser
Top Cell Name	nand2
View Name	symboli
Library Name	hwlž
Output File	nand2. sp
Run Directory	

Hotkeys

Instance	i	Сору	с
Narrow Wire	w	Move	М
Wide Wire	W	Delete	del
Pin	р	Rotate	r
Undo	u	Property	q
Redo	U	Zoom	z
Stretch	m	Check & Save	Х
Descend Edit/Read	E/e	Ascend one level	Ctrl+e

Thank you!