2014 Analog IC: Midterm Examination (100%)

1. Answer definitions of the following effects and explain the physical mechanisms. (**10%**)
   (a) Junction breakdown. (2%)
   (b) Channel length modulation effect. (2%)
   (c) Mobility degradation. (2%)
   (d) Hot carrier effect. (2%)
   (e) Velocity saturation. (2%)

2. A source follower as shown in Fig. 2 with g_m = 1mA/V, $g_{mb} = 0.2g_m$, R_S = 500kΩ, and r_o = 100kΩ. (**5%**)
   (a) Sketch the small signal equivalent circuit. (2.5%)
   (b) Find the voltage gain V_{out}/V_{in}. (2.5%)

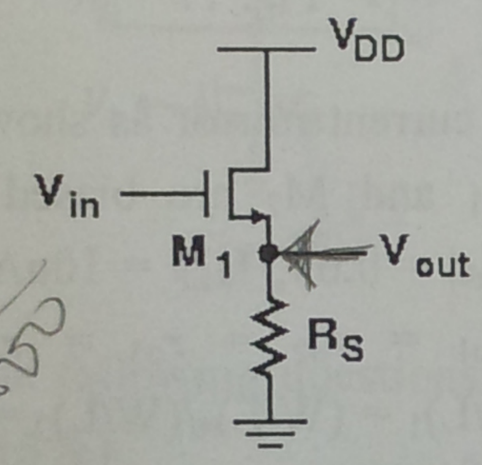

Fig. 2

3. Sweep V_{GS} of nMOS with a constant V_D, the C_{GS} and C_{GD} curves are shown in Fig. 3. (**10%**)
   (a) Find values of C1, C2, and C3 in W, L, C_{ox}, and C_{ov}. (6%)
   (b) Define the operation regions I, II, and III. (4%)

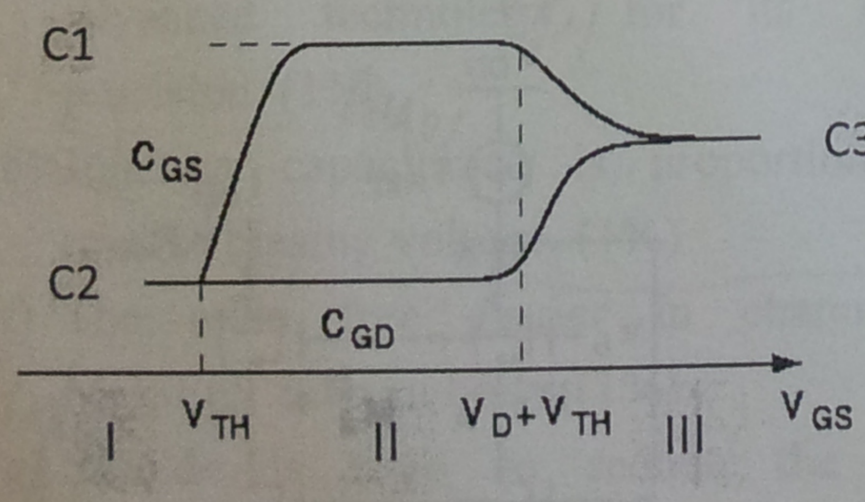

Fig. 3

4. Write down the drain current equations of MOSFET in triode and saturation region with channel length modulation effect. (**5%**)

5. The r_o vs. V_{DS} characteristic of MOSFET is shown in Fig. 5. Please identify and explain the effects at the three regions. (**5%**)

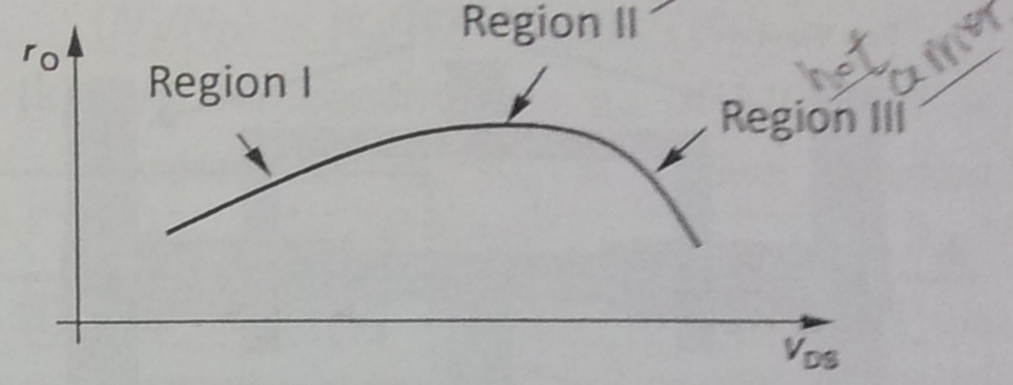

Fig. 5

6. Derive the equation of voltage gain V_{out}/V_{in} of amplifier as shown in Fig. 6 in terms of $g_{m<n>}$, $g_{mb<n>}$, $g_{m<p>}$, $g_{mb<p>}$, $r_{o<n>}$ and $r_{o<p>}$. (**5%**)

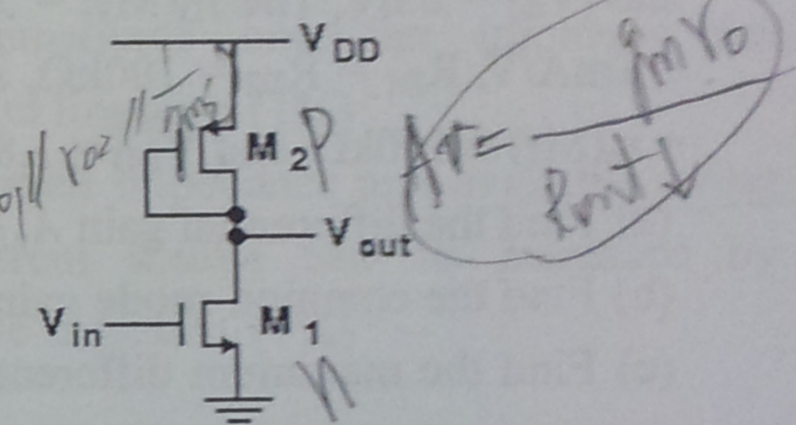

Fig. 6

7. Assume $g_{mb} = 0$, $r_o = \infty$, g_m = 1mA/V, R_S = 20kΩ, and R_D = 100kΩ in the circuit of Fig. 7. (**5%**)
   (a) Find the short circuit transconductance G_m of this amplifier. (2.5%)
   (b) Find the voltage gain V_{out}/V_{in}. (2.5%)

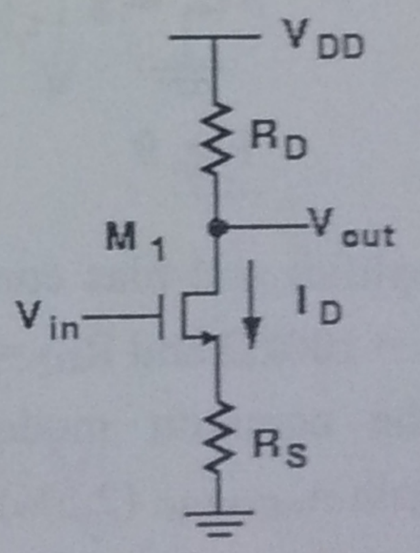

Fig. 7

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8. Fig. 8 is a layout of CMOS inverter. (**5%**)
   (a) Draw the cross section from A-A'. (2.5%)
   (b) Identify and index all the name of layers. (2.5%)

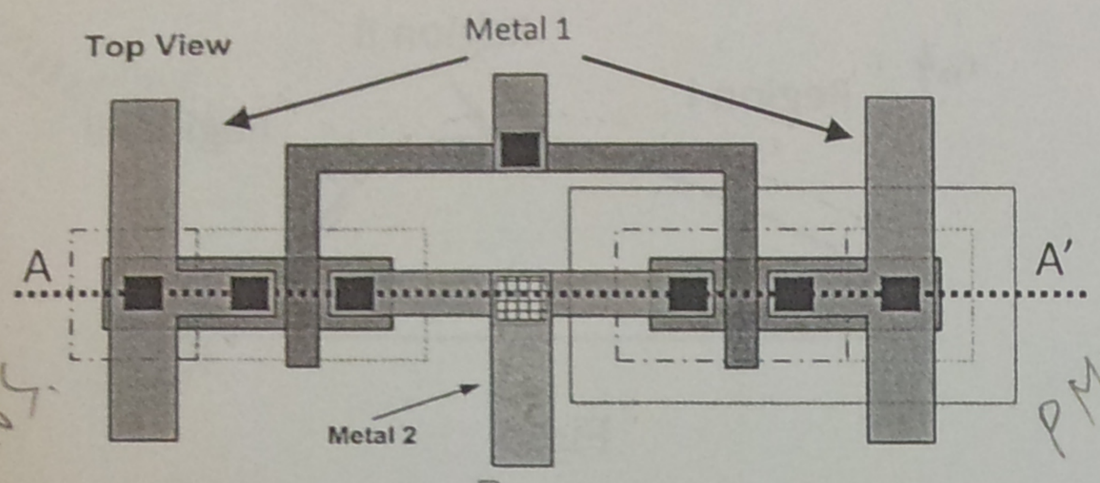

Fig. 8

9. A differential pair is shown in Fig. 9. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV and $|V_{th}|$ = 0.6V. The $I_D(M_3)$ = 50uA, $g_{m1} = g_{m2}$ = 1mA/V, $R_{D1} = R_{D2}$ = 100kΩ, $r_o(M_1) = r_o(M_2) = r_o(M_3)$ = 100kΩ, and V_{DD} = 1.8V. (**10%**)
   (a) Find the differential gain $A_{v.DM}$. (2.5%)
   (b) Find the common-mode gain $A_{v.CM}$. (2.5%)
   (c) Find the maximum differential input signal range. (2.5%)
   (d) Find the input common mode range. (2.5%)

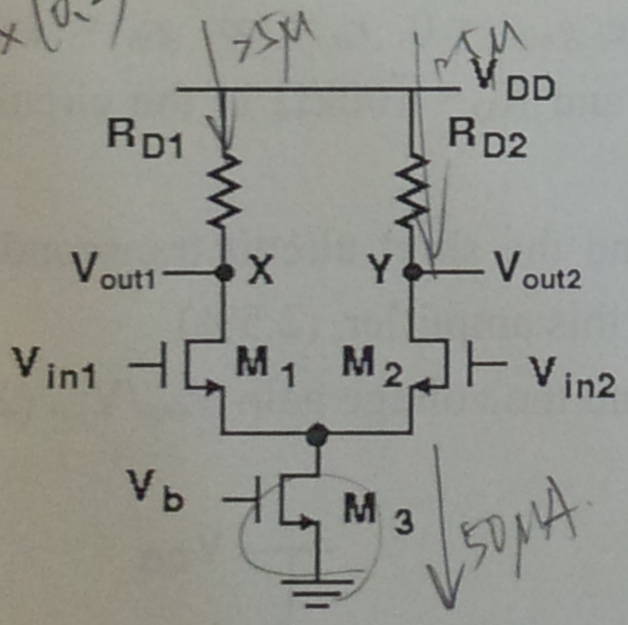

Fig. 9

10. Use the amplifier and bias condition in Fig. 9, assume R_{D1} = 100kΩ and R_{D2} = 110kΩ. (**5%**)
   (a) Find the common mode to differential mode gain $A_{v.CM\text{-}DM}$. (2.5%)
   (b) Assume $A_{v.DM}$ = the value in 9(a), find the *CMRR*. (2.5%)

11. Assume g_m = 1mA/V, $g_{mb} = 0.2\ g_m$, R_S = 10kΩ, and R_D = 100kΩ in the circuit of Fig. 11. (**5%**)
   (a) With $r_o = \infty$, find input impedance. (2.5%)
   (b) With r_o = 100kΩ, find the output impedance. (2.5%)

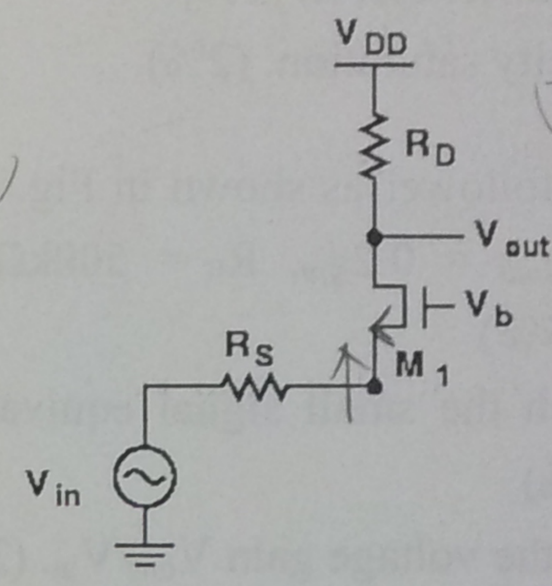

Fig. 11

12. A cascode current mirror as shown in Fig. 12, assume M_1 and M_2 are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.6V, I_{REF} = 10uA, $g_{m1} = g_{m2}$ = 1mA/V, $r_{o1} = r_{o2} = r_{o3} = r_{o4}$ = 100kΩ, $(W/L)_3/(W/L)_1 = (W/L)_4/(W/L)_2$ = 4, and V_{DD} = 1.8V. (**10%**)
   (a) Find the g_{m3} and g_{m4}. (2.5%)
   (b) Find the minimum V_b and related output voltage V_{out} for proper current mirror operation. (2.5%)
   (c) Find the output resistance R_{out}. (2.5%)
   (d) Sketch a circuit to generate the required optimal bias V_b in (b). (2.5%)

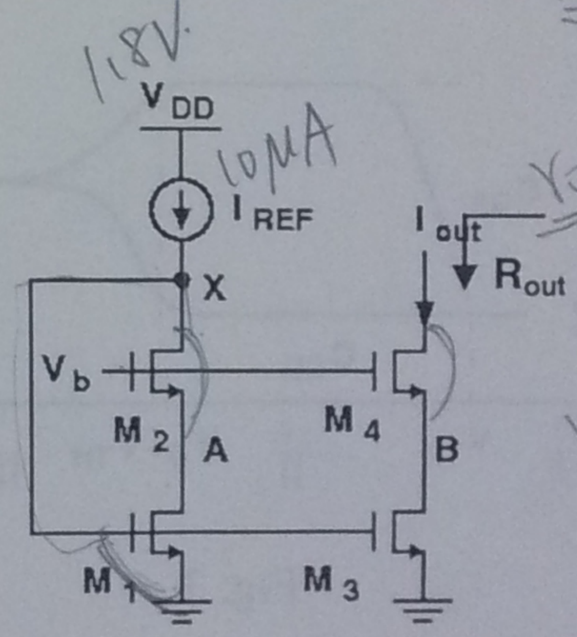

Fig. 12

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13. A differential to single-ended amplifier is shown in Fig. 13. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.6V, r_o = 100kΩ, and u_nC_{ox} = 0.001F/V*S. The $I_D(M_5)$ = 80uA and V_{DD} = 1.8V. **(5%)**

(a) Find the minimum input DC bias voltage. (2.5%)

(b) Find the voltage gain $V_{out}/(V_{in1}-V_{in2})$. (2.5%)

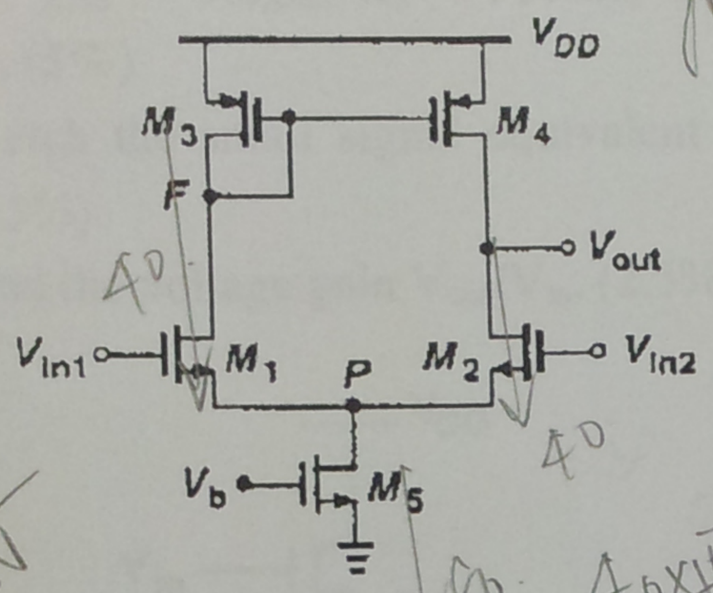

Fig. 13

14. Answer the following questions with TRUE or FALSE: **(15%)**

F (a) The angle of ion implant is "zero" degree for better depth control. (1%)

F (b) Chemical vapor deposition is a common process for metal formation in IC manufacturing. (1%)

F (c) Annealing is for crystal lattice reforming after oxidation. (1%)

F (d) Shallow trench isolation is used in advanced technology for its higher precision. (1%)

F (e) Junction capacitance is proportional to reverse biasing voltage. (1%)

F (f) The main free carrier in channel of MOSFET is from body. (1%)

F (g) Silicide is used to reduce the sheet resistance of diffusion. (1%)

T (h) The voltage gain of source follower is smaller than unity and decreased by body effect. (1%)

F (i) The threshold voltage of nMOS is increased by n+ channel implantation. (1%)

F (j) The depletion width of p/n ratio (W_p/W_n) in diode is correlated to doping concentration (N_A/N_D) as $W_p/W_n = N_A/N_D$. (1%)

F (k) The transconductance g_m of MOSFET is proportional to V_{ov} at known constant biasing current. (1%)

T (l) The channel charge of MOSFET is proportional to W*L and overdrive voltage V_{ov} as well. (1%)

F (m) The output resistance of MOSFET at saturation region is inversely proportional to bias current. (1%)

F (n) The addition of source resistor on common-source amplifier improves the gain and linearity. (1%)

F (o) The output impedance and available swing of current source can be increased by cascode structure. (1%)

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