1. A common gate amplifier is shown in Fig. 1 with C_D = 10fF, C_S = 10fF, C_L = 50fF, g_{mb} = 0, r_o = ∞, g_m = 1mA/V, R_S = 20kΩ, and R_D = 100kΩ. **(5%)**
   (a) Find the input and output impedances. (2.5%)
   (b) Find the correlated input pole ω_{in} and output pole ω_{out}. (2.5%)

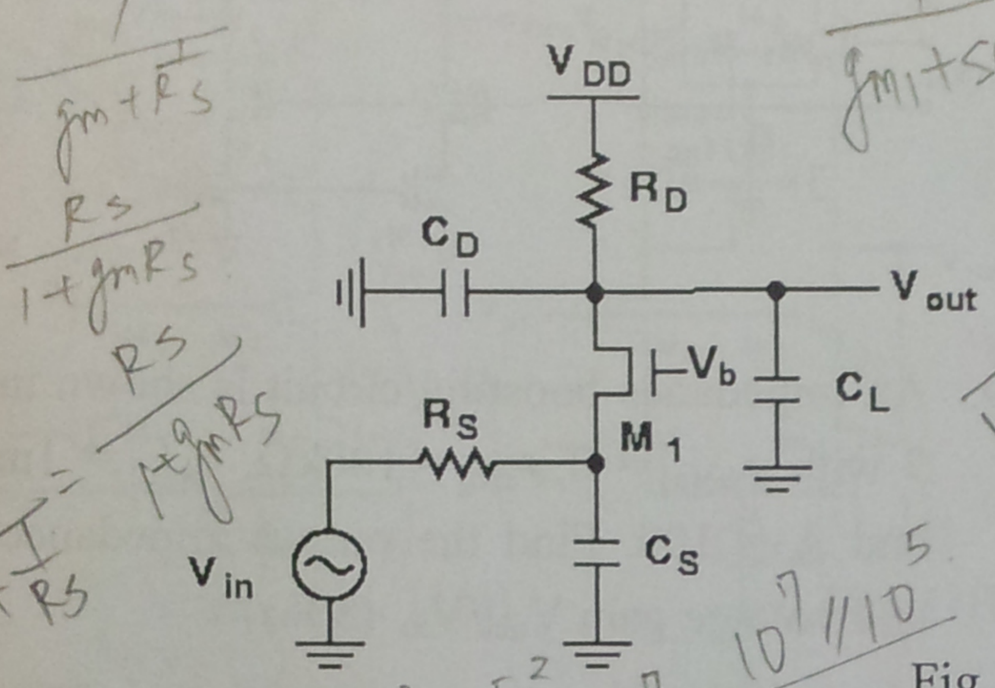

Fig. 1

2. A cascode amplifier is shown in Fig. 2 with $C_{GD[n]} = C_{GS[n]}$ = 20fF, $C_{SB[n]} = C_{DB[n]}$ = 10fF, C_L = 50fF, $g_{mb[n]}$ = 0, $r_{o[n]}$ = 100kΩ, $g_{m[n]}$ = 1mA/V, R_S = 20kΩ, and R_D = 100kΩ. **(5%)**
   (a) Find the equivalent C_{in} at node A and C_{out} at node V_{out} . (2.5%)
   (b) Find the correlated input pole ω_{in} and output pole ω_{out}. (2.5%)

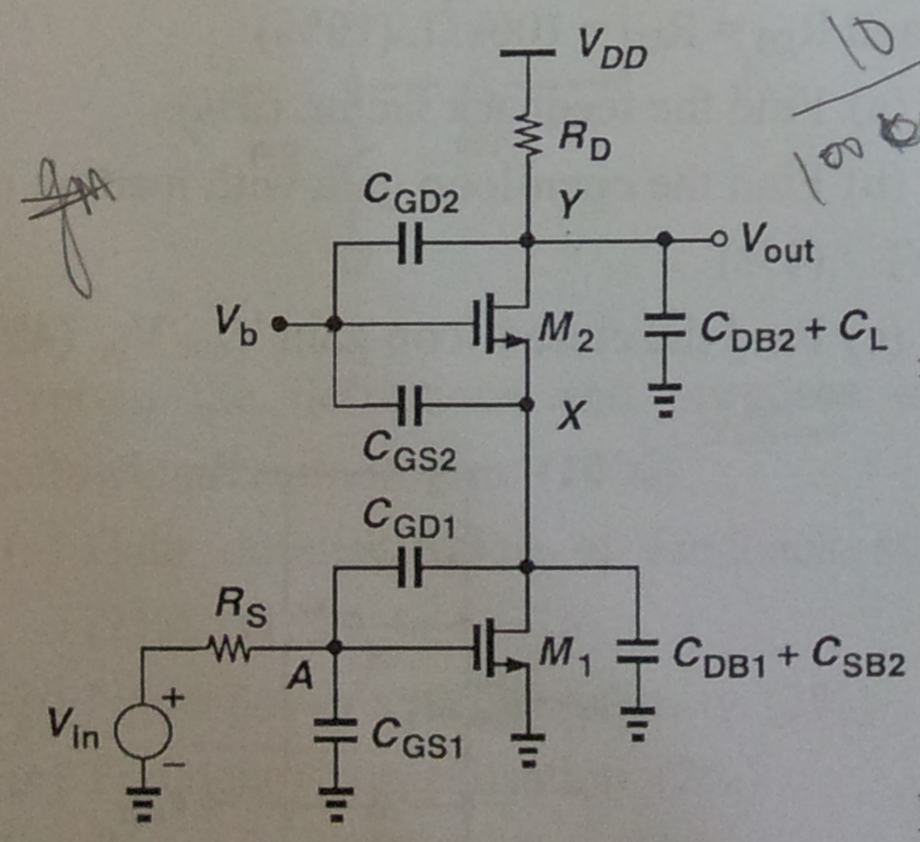

Fig. 2

3. A two-stage Op Amp in Fig. 3 has A_{v1} = 10, A_{v2} = 100. The output referred noise of A1 = 5×10^{-12} V^2/Hz and A2 = 10×10^{-12} V^2/Hz. **(5%)**
   (a) Find the total output referred noise of amplifier A. (2.5%)
   (b) Find the "**best**" total input referred noise by rearrangement of A1 and A2 to get the same total gain A = 1000. (2.5%)

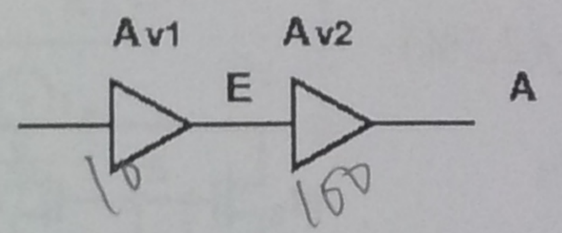

Fig. 3

4. A R-C low-pass filter is shown in Fig. 4. The resistor's thermal noise = 4kTR. Derive the total noise power at output node. **(5%)**

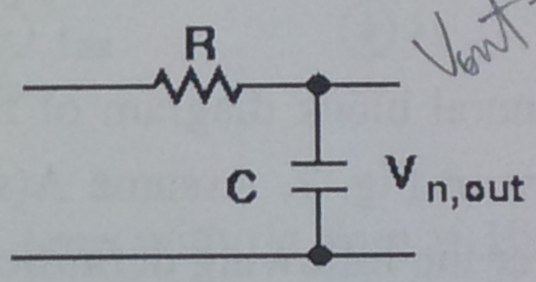

Fig. 4

5. A common source amplifier is shown in Fig. 5. The thermal noise and flicker noise of M_1 are $\overline{I_n^2} = 4kTg_m(\frac{2}{3})$ and $\overline{V_n^2} = \frac{K}{C_{ox}WL}\cdot\frac{1}{f}$. **(5%)**
   (a) Derive the input referred noise $\overline{V_{n,in}^2}$ due to thermal noise. (2.5%)
   (b) Derive the input referred noise $\overline{V_{n,in}^2}$ due to flicker noise. (2.5%)

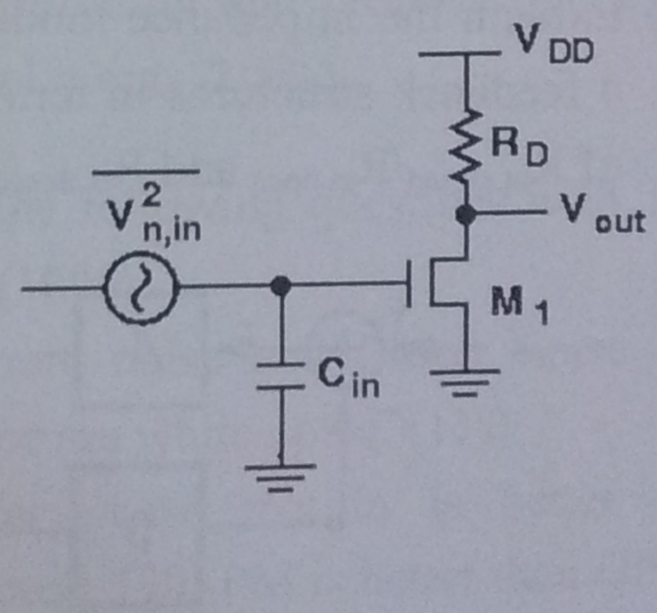

Fig. 5

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6. A differential pair is shown in Fig. 6 with C_E = 50fF, C_L = 50fF, $g_{mb[n]} = 0$, $r_{o[n]}$ = 100kΩ, $g_{m[n]}$ = 1mA/V, $|V_{gs[n]}| = 0.8V$, $|V_{th[n]}| = 0.5V$. **(10%)**
   (a) Find the minimum input DC bias voltage with $V(I_{SS}) = 0.2V$. (2.5%)
   (b) Find the voltage gain V_{out}/V_{in}. (2.5%)
   (c) Find the frequency of the dominant pole. (2.5%)
   (d) Find the frequency of the second pole. (2.5%)

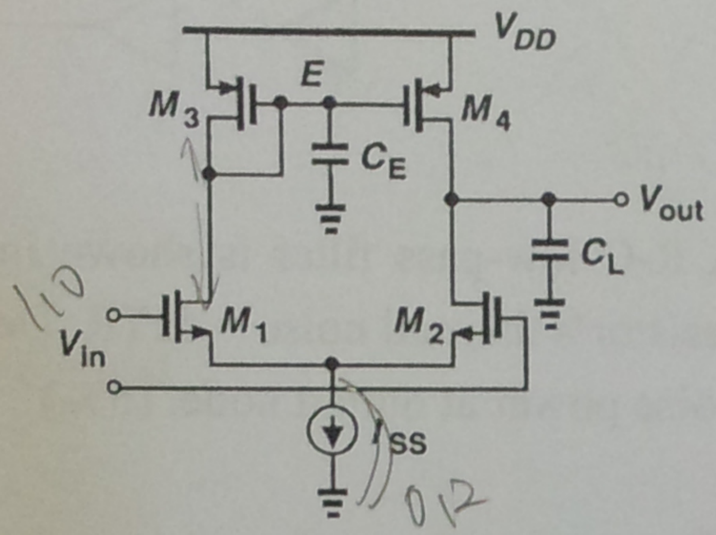

Fig. 6

7. A general block diagram of feedback system is shown in Fig. 7. Assume $A(s) = A_0/[1+(s/\omega_0)]$, answer the following definitions of terminology. **(10%)**
   (a) State the oscillation condition. (2%) (Barkhausen's Criteria)
   (b) Derive the equation of closed loop gain. (2%)
   (c) Explain the ***bandwidth modification*** of closed- loop system compared to open-loop. (2%)
   (d) List down 4 types of feedback structures. (2%)
   (e) Explain the impedance modification of the 4 feedback structures in terms of equations of $R_{in.closed}/R_{in.open}$ and $R_{o.closed}/R_{o.open}$.

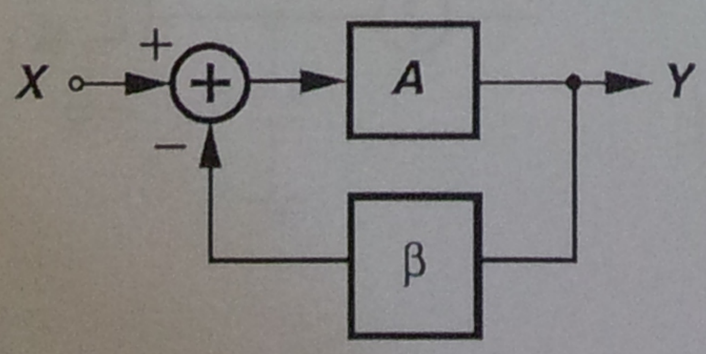

Fig. 7

8. A fully-differential amplifier is shown in Fig. 8. Add the necessary biases and common-mode feedback circuit on it, sketch the complete circuit. **(5%)**

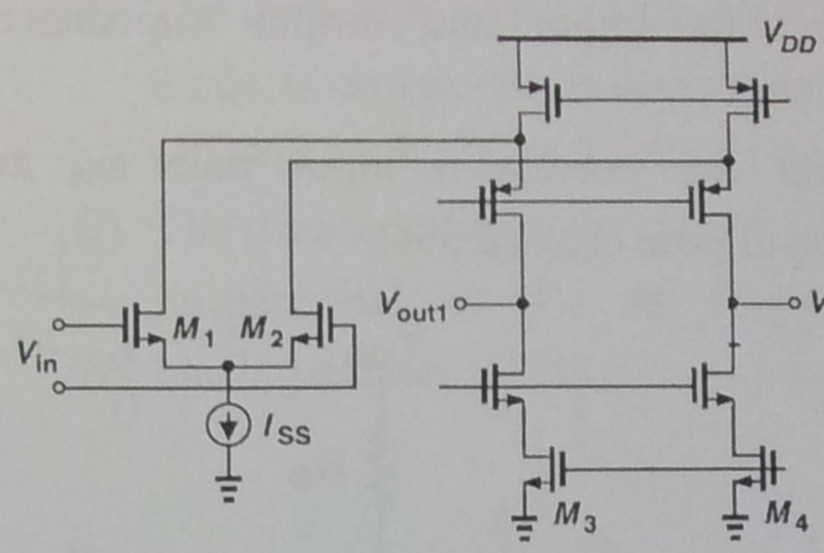

Fig. 8

9. An impedance boosting circuit is shown in Fig. 9 with $g_{mb[n]} = 0$, $r_{o[n]}$ = 100kΩ, $g_{m[n]}$ = 1mA/V, and A = 100. Find the output impedance R_{out} and voltage gain V_{out}/V_{in}. **(5%)**

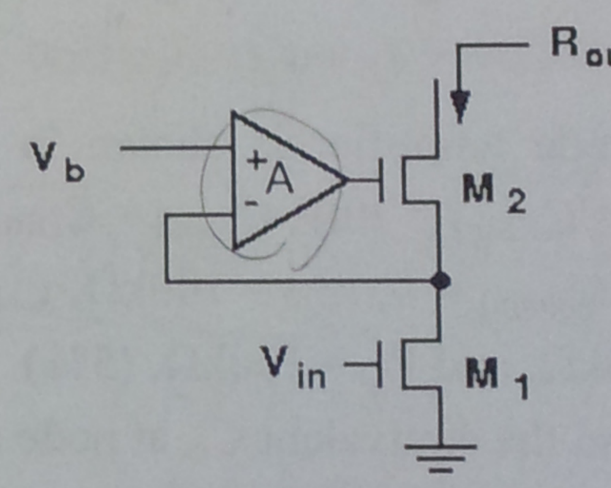

Fig. 9

10. A common-source amplifier with resistive feedback as shown in Fig. 10 with $g_{mb[n]} = 0$, $r_{o[n]}$ = 100kΩ, $g_{m[n]}$ = 1mA/V, R_S = 20kΩ, R_F = 30kΩ, and $R_{D1} = R_{D2}$ = 100kΩ. **(10%)**
    (a) Find the feedback factor. (2%)
    (b) Find the open-loop gain with loading effect. (4%)
    (c) Find the closed-loop gain V_{out}/V_{in}. (4%)

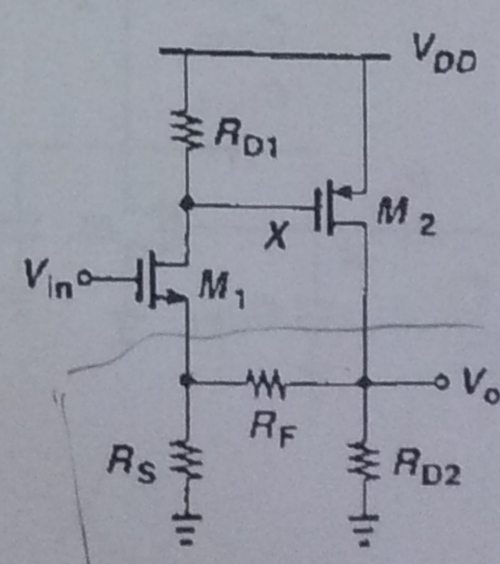

Fig. 10

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11. A differential-to-single-ended Op Amp is shown in Fig. 11 with $|V_{gs[n]}| = 0.8V$, $|V_{th[n]}| = 0.5V$, and $V_{DD} = 3.3V$. **(5%)**
    (a) Find the Vb1 and the corresponding maximum output swing in 11(a). (2.5%)
    (b) As a unity-gain buffer in 11(b), find the available maximum output range. (2.5%)

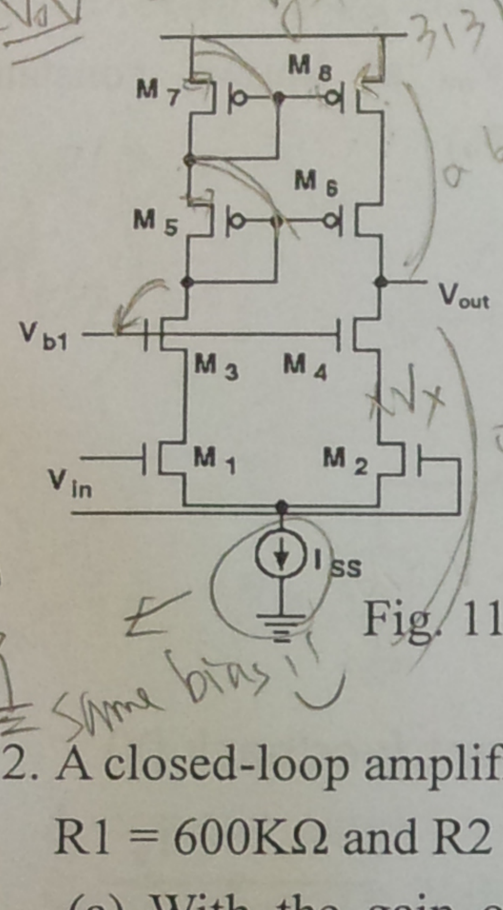

Fig. 11(a)

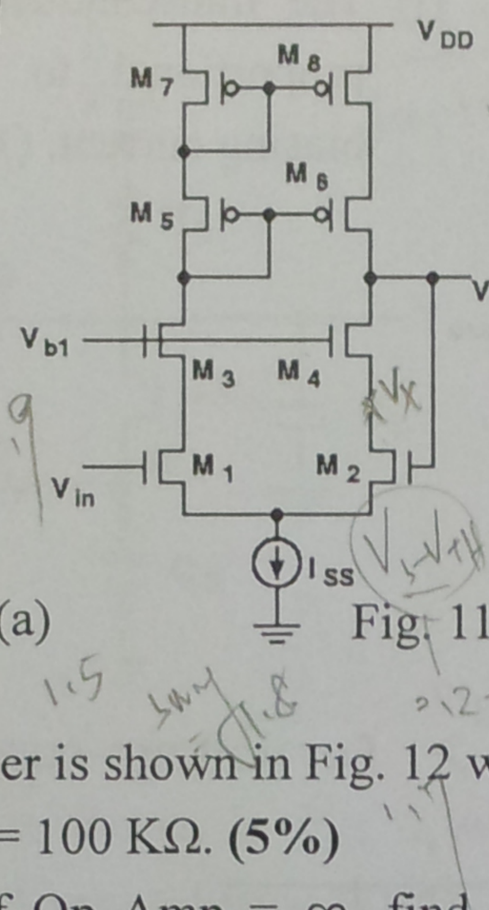

Fig. 11(b)

12. A closed-loop amplifier is shown in Fig. 12 with R1 = 600KΩ and R2 = 100 KΩ. **(5%)**
    (a) With the gain of Op Amp = ∞, find the ideal closed-loop gain. (2.5%)
    (b) What is the open-loop gain requirement of Op Amp to get an error of closed-loop gain smaller than 1%. (2.5%)

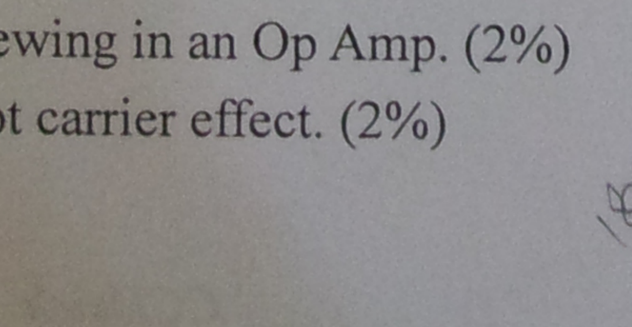

Fig. 12

13. Explain the definitions and purposes of the following terminologies. **(10%)**
    (a) Gain desensitization of feedback system. (2%)
    (b) Noise power spectrum density. (2%)
    (c) Frequency compensation. (2%)
    (d) Slewing in an Op Amp. (2%)
    (e) Hot carrier effect. (2%)

14. Find slew rate of the following Op Amps. **(5%)**
    (a) Differential pair with capacitive feedback. (2.5%)
    (b) 2-stage OP Amp with capacitor C_C. (2.5%)

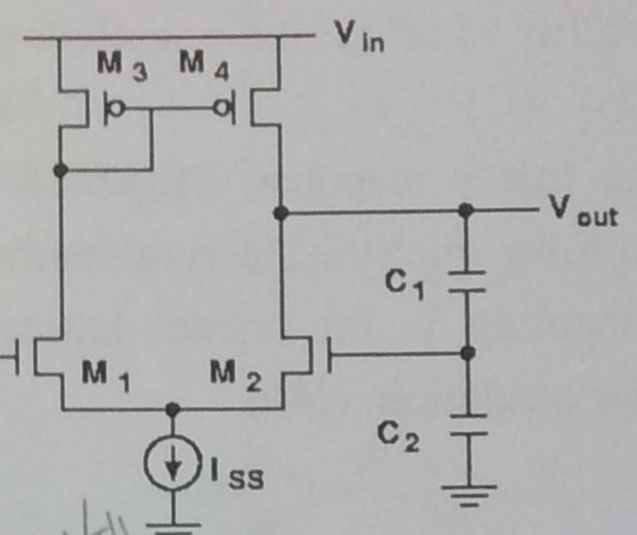

Fig. 14(a)

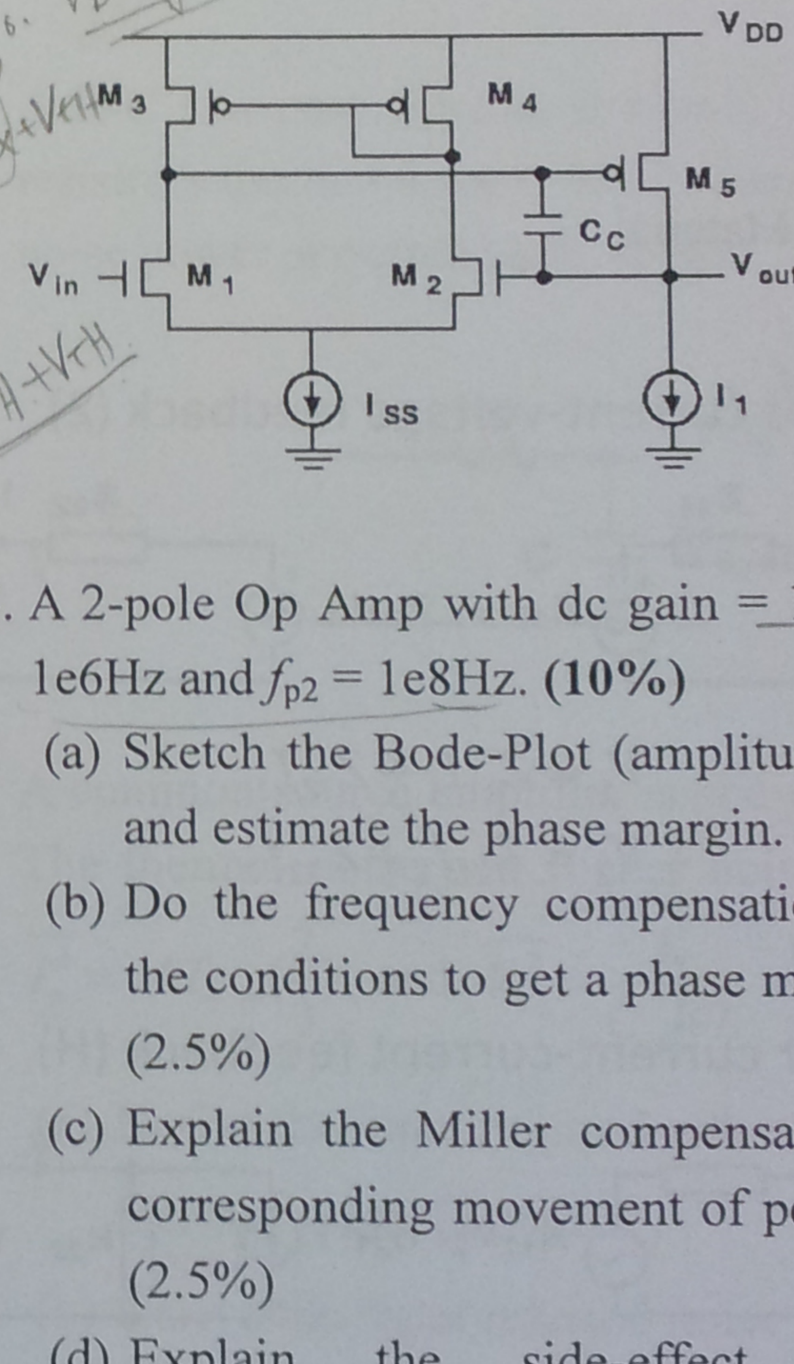

Fig. 14(b)

15. A 2-pole Op Amp with dc gain = 100dB, f_{p1} = 1e6Hz and f_{p2} = 1e8Hz. **(10%)**
    (a) Sketch the Bode-Plot (amplitude & phase) and estimate the phase margin. (2.5%)
    (b) Do the frequency compensation and state the conditions to get a phase margin as 45°. (2.5%)
    (c) Explain the Miller compensation and the corresponding movement of pole positions. (2.5%)
    (d) Explain the side-effect of Miller compensation and propose one solution to cancel it out. (2.5%)

16. Answer the following questions with TRUE or FALSE: **(10%)**
    (a) Thermal noise and flicker noise of MOS device are white noise. (1%)
    (b) Larger phase margin is better for step response. (90° PM is better than 60°). (1%)

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(c) CMRR is defined by the ratio between A_{DM}/A_{CM} and it will degrade at high frequency. (1%)

(d) Right half plane zero will degrade the stability due to its negative phase shift. (1%)

(e) The linear response happened only when Op Amp enter the slewing condition. (1%)

(f) Annealing is for crystal lattice reforming after oxidation. (1%)

(g) The main free carrier in channel of MOSFET is from body. (1%)

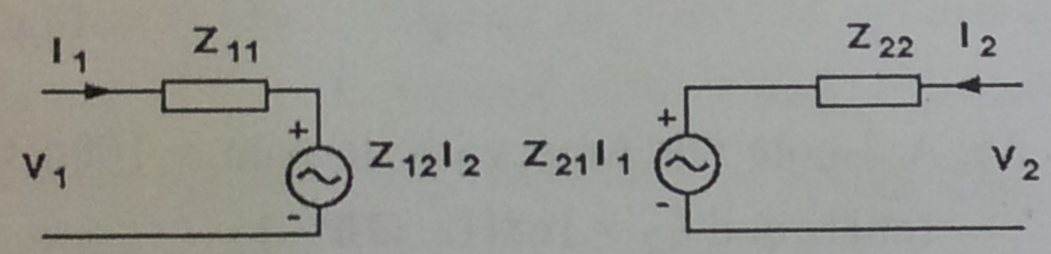
(h) The threshold voltage of nMOS is increased by n+ channel implantation. (1%)

(i) The depletion width of p/n ratio (W_p/W_n) in diode is correlated to doping concentration (N_A/N_D) as $W_p/W_n = N_A/N_D$. (1%)

(j) The transconductance g_m of MOSFET is proportional to V_{ov} at known constant biasing current. (1%)

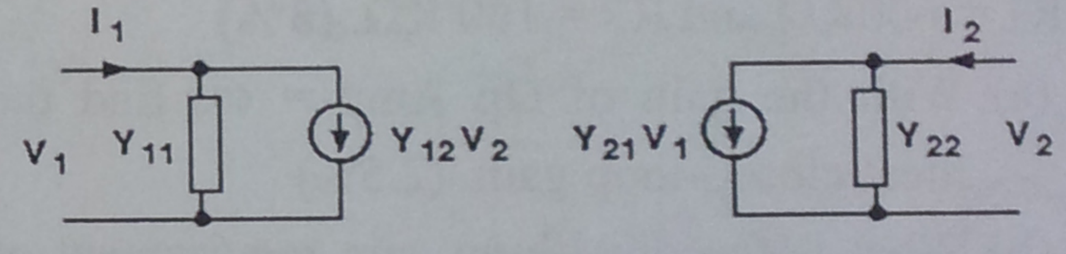
Reference Material

- For current-voltage feedback (Z)



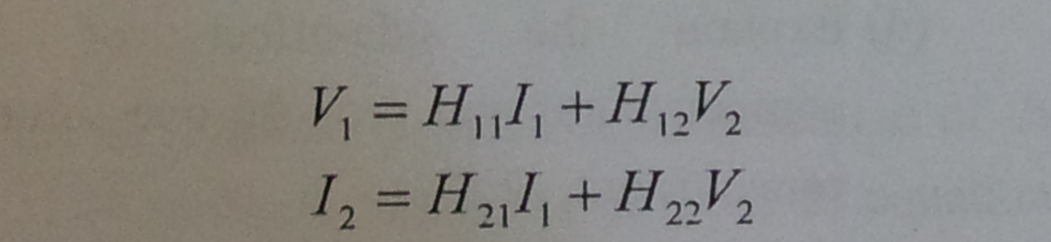
$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

- For voltage-current feedback (Y)



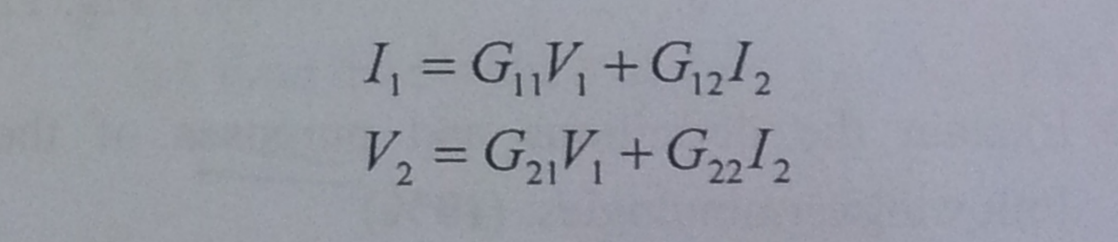
$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

- For current-current feedback (H)



$$V_1 = H_{11}I_1 + H_{12}V_2$$
$$I_2 = H_{21}I_1 + H_{22}V_2$$

- For voltage-voltage feedback (G)



$$I_1 = G_{11}V_1 + G_{12}I_2$$
$$V_2 = G_{21}V_1 + G_{22}I_2$$