2012 Analog IC: Midterm Examination (110%)

1. Answer definitions of the following effects and explain the physical mechanisms. **(10%)**
   (a) Hot carrier effect. (2%)
   (b) Mobility Degradation. (2%)
   (c) Punch Through. (2%)
   (d) Body effect. (2%)
   (e) Velocity Saturation. (2%)

2. A NMOS is biased with a gate voltage V_G and a drain voltage V_D as shown in Fig. 2. **(10%)**
   (a) Sketch the I_D-V_D transfer curves with different V_G. (2.5%)
   (b) Illustrate the boundary line of linear / saturation regions on the curves. (2.5%)
   (c) Illustrate the early voltage and ro. (2.5%)
   (d) Illustrate the threshold voltage V_{TH}. (2.5%)

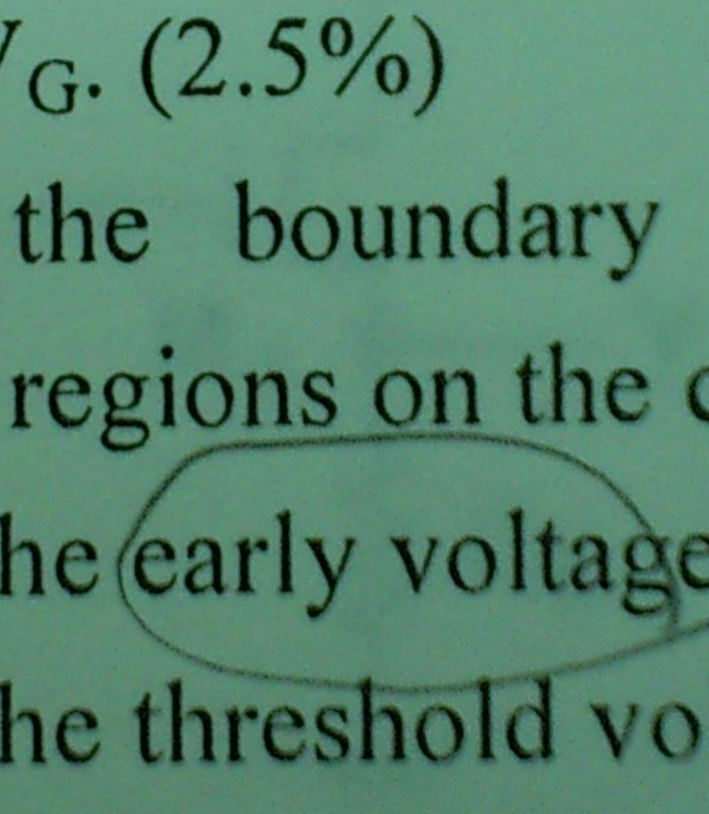

Fig. 2

3. Figure 3 shows a NMOS with parameters of

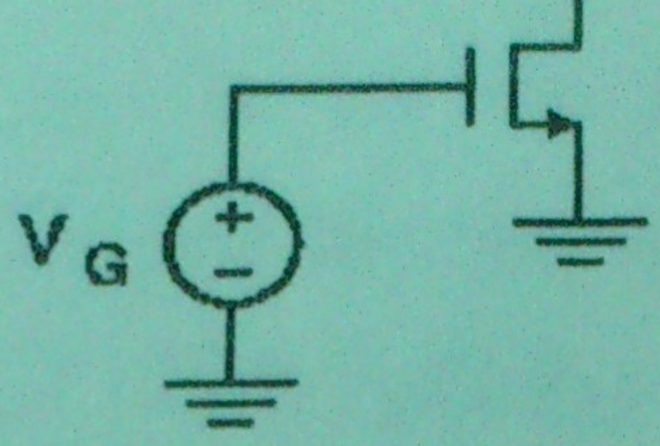

Fig. 2

3. Figure 3 shows a NMOS with parameters of $V_{TH} = 0.7V$, $W = 10um$, $L = 1um$, $C_{ox} = 1fF/um^2$ and $C_{ov} = 0.1fF/um$. **(10%)**

(a) Find and sketch the capacitances of C_{EN} and C_{EF} as V_X varies from 0 to 3V, identify V_X value of the transition point also. (5%)

(b) Sketch the capacitances of C_{FB} and C_{NB} as V_X varies from 0 to 3V, identify V_X value of the cross point also. (5%)

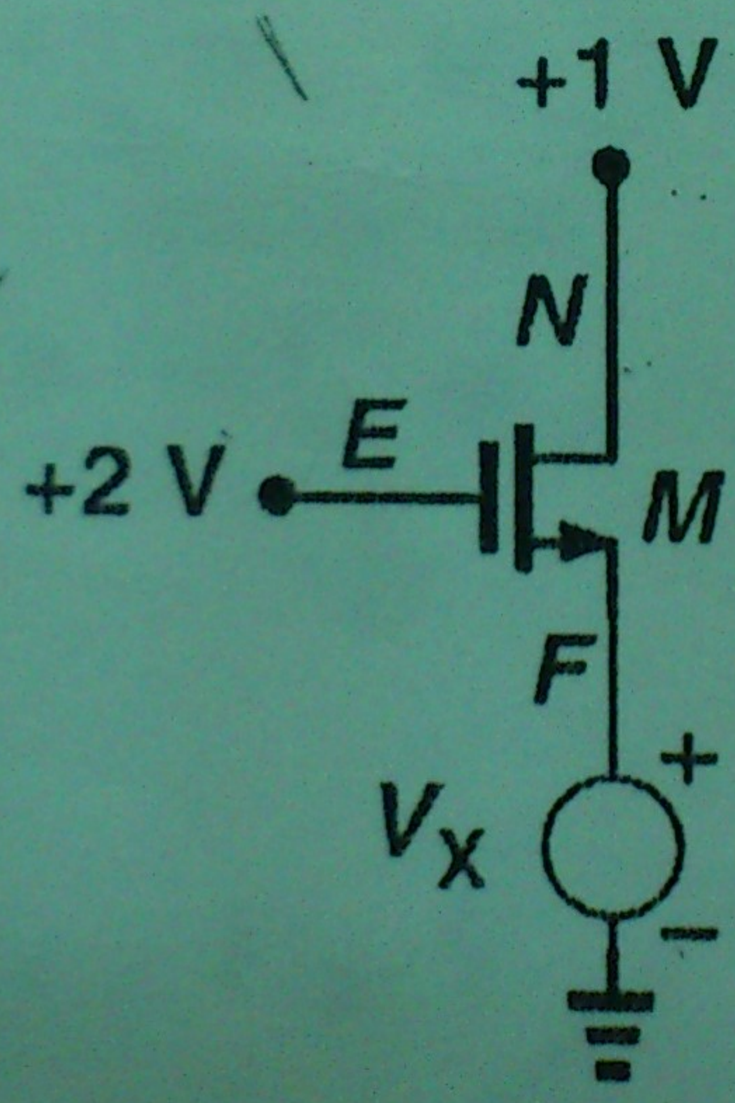

Fig. 3

4. Fig. 4 is a layout of CMOS inverter. **(5%)**
   (a) Draw the cross section from A-A'. (2.5%)
   (b) Identify and make the orders of masks in semiconductor process flow. (2.5%)

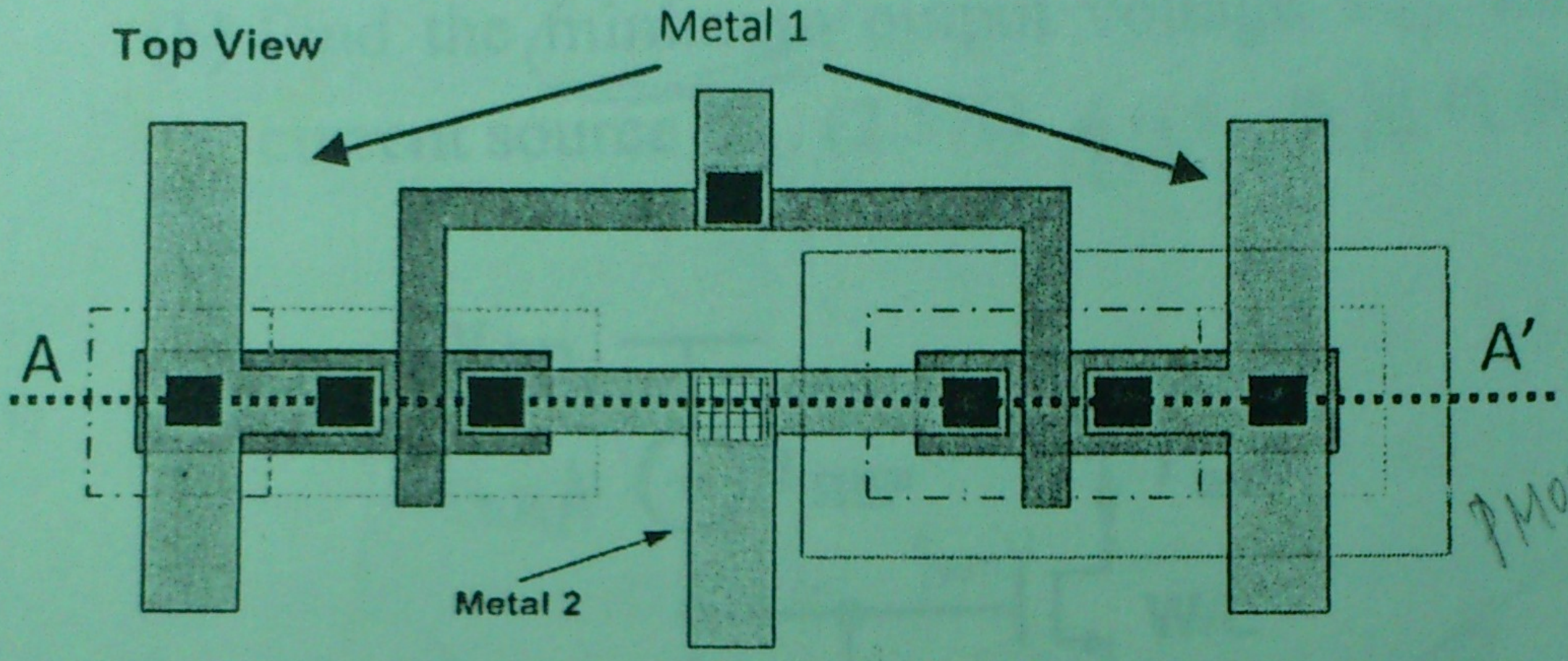

Fig. 4

5. Fig. 5 is a common-source amplifier. **(5%)**
   (a) Sketch the small signal equivalent circuit. (2.5%)
   (b) Derive the equation of voltage gain V_{out}/V_{in} in terms of $g_{m<n>}$, $g_{mb<n>}$ and $r_{o<n>}$. (2.5%)

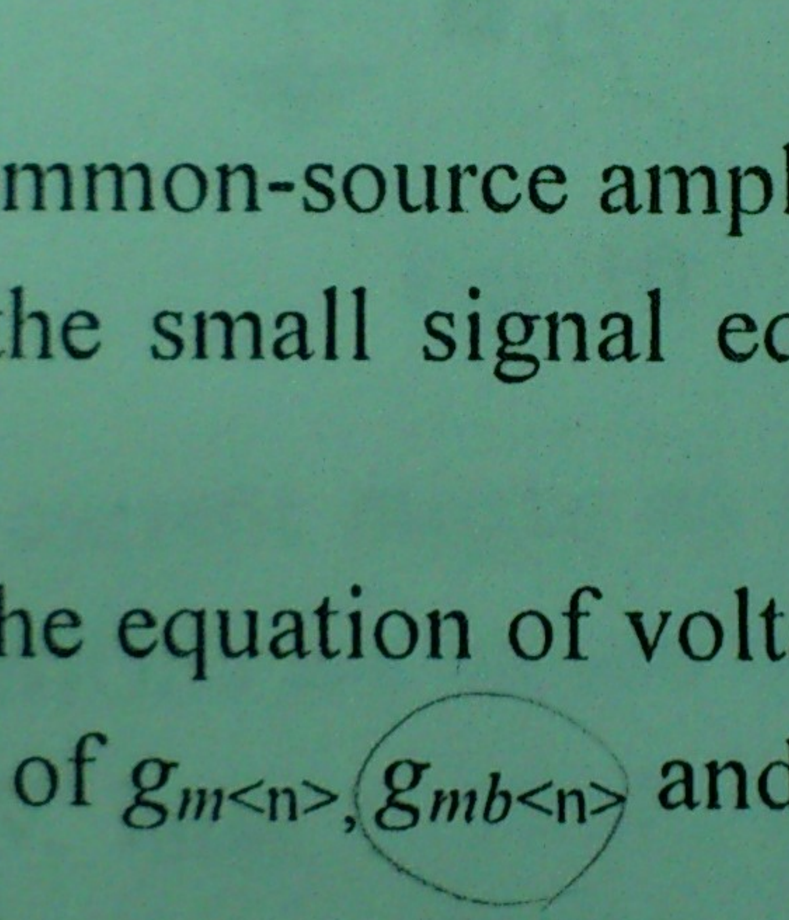

Fig. 5

6. Assume r_o = 100k, I_D=10uA, $|V_{ov}|$ = 200mV, g_{mb} = 0, and R_S=100KΩ in Fig. 6. **(5%)**
   (a) Sketch the small signal equivalent circuit.

in terms of $g_{m<n>}$, $g_{mb<n>}$ and $r_{o<n>}$. (2.5%)

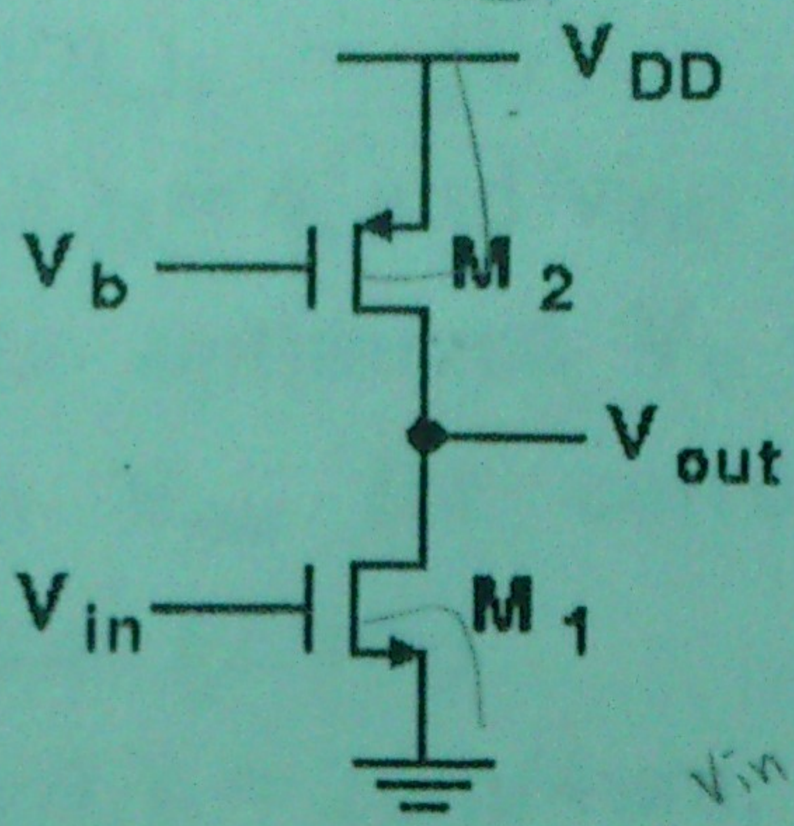

Fig. 5

6. Assume r_o = 100k, I_D=10uA, $|V_{ov}|$ = 200mV, g_{mb} = 0, and R_S=100KΩ in Fig. 6. **(5%)**

(a) Sketch the small signal equivalent circuit. (2.5%)

(b) Find the output resistance R_{out}. (2.5%)

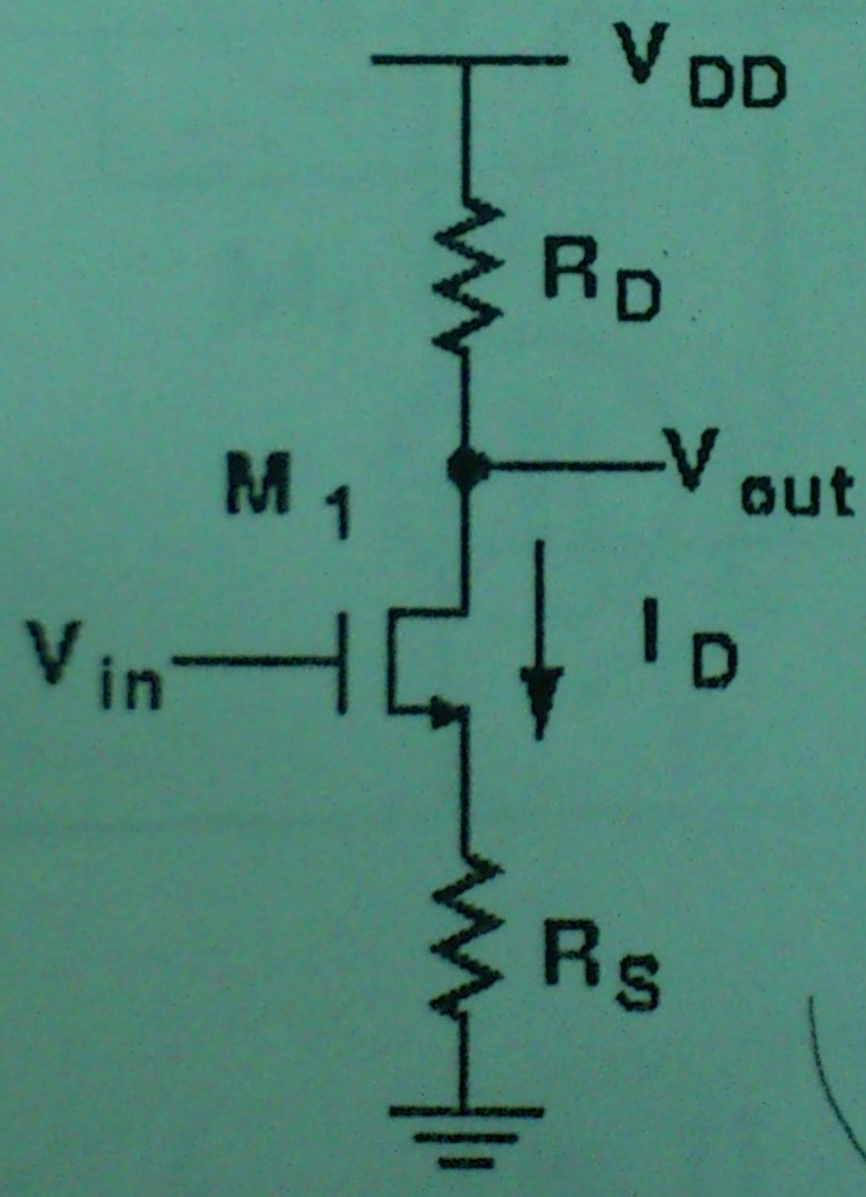

Fig. 6

$$I_D = \mu C_{ox} \frac{W}{L}\left((V_{GS}-V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

$$I_D = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

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7. Write down the drain current equations of MOSFET in triode and saturation region with channel length modulation effect. **(5%)**

8. A source follower as shown in Fig. 8 with g_m = 2mA/V, $g_{mb} = 0.2g_m$, R_S = 100KΩ, and $r_o = \infty$. **(5%)**

   (a) Sketch the small signal equivalent circuit. (2.5%)

   (b) Find the voltage gain V_{out}/V_{in}. (2.5%)

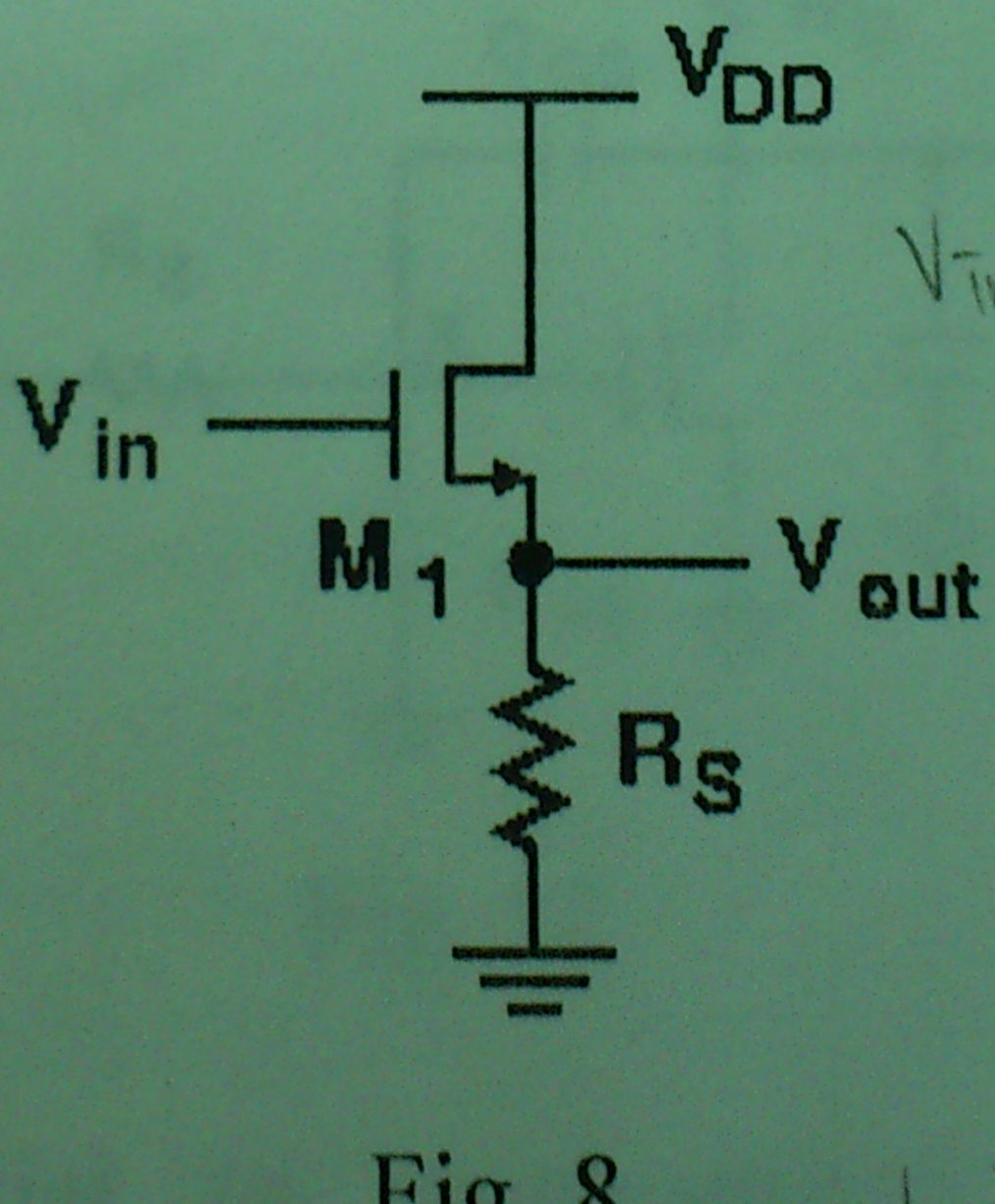

Fig. 8

9. A differential pair is shown in Fig. 9. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV and $|V_{TH}|$ = 0.6V. The $I_D(M_3)$ = 20uA, $g_{m1} = g_{m2}$ = 2mA/V, $R_{D1} = R_{D2}$ = 100kΩ, $r_o(M_1) = r_o(M_2)$

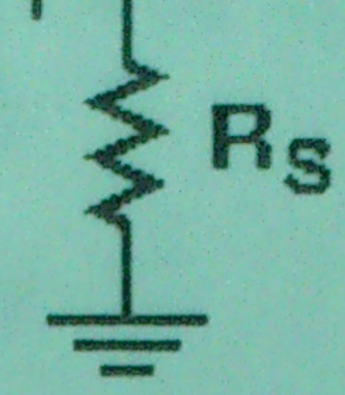

Fig. 8

9. A differential pair is shown in Fig. 9. Assume all the MOSFETs are biased with $|V_{ov}| = 200\text{mV}$ and $|V_{TH}| = 0.6\text{V}$. The $I_D(M_3) = 20\text{uA}$, $g_{m1} = g_{m2} = 2\text{mA/V}$, $R_{D1} = R_{D2} = 100\text{k}\Omega$, $r_o(M_1) = r_o(M_2) = r_o(M_3) = 200\text{k}\Omega$, and $V_{DD} = 1.8\text{V}$. **(10%)**

(a) Find the differential gain $A_{v.DM}$. (2.5%)

(b) Find the common-mode gain $A_{v.CM}$. (2.5%)

(c) Find the maximum differential input signal range. (2.5%)

(d) Find the input common mode range. (2.5%)

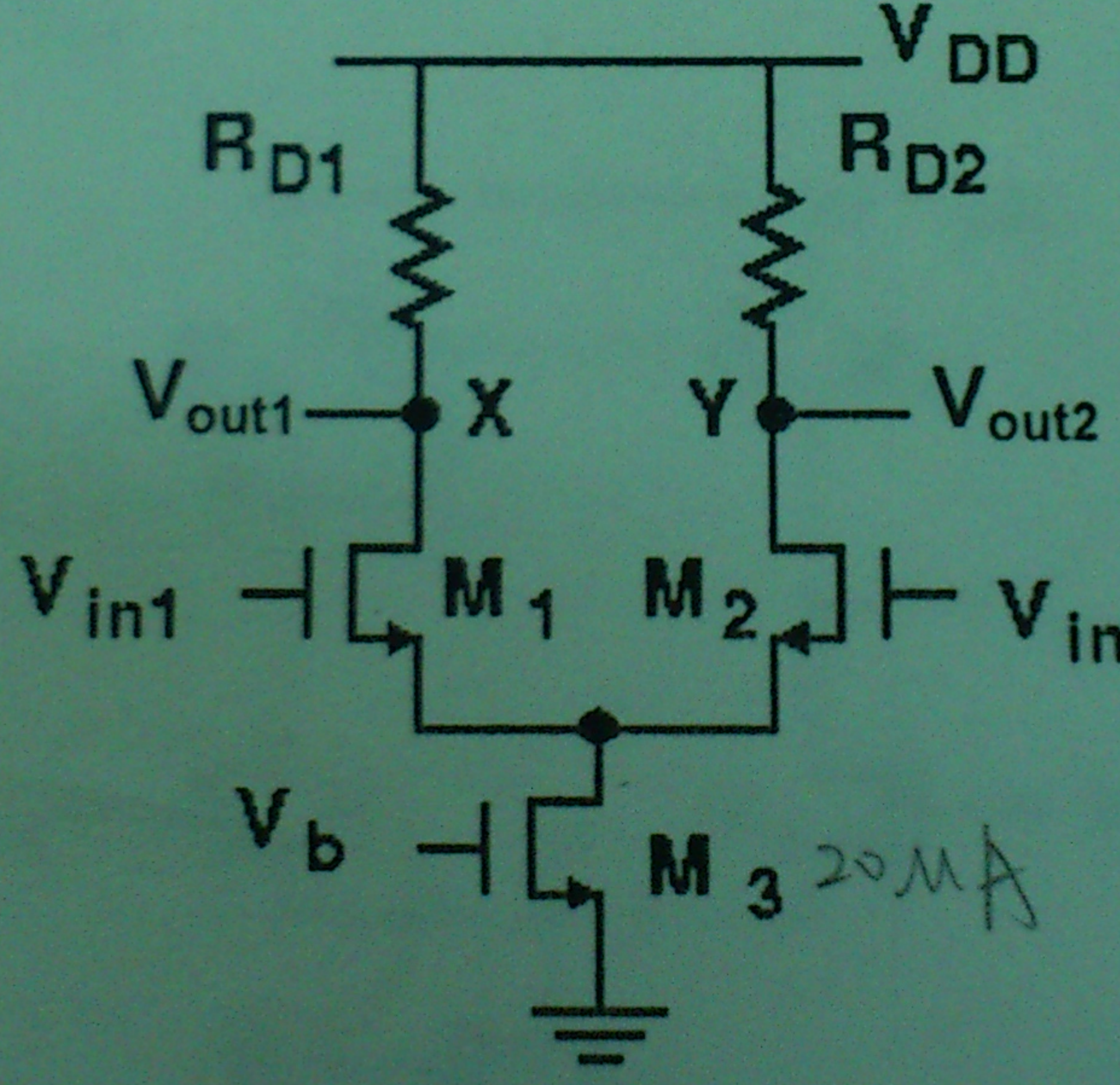

Fig. 9

$$\frac{I_{out}}{I_{REF}} = \frac{4\left(1+\frac{1}{50}\times 0.5\right)}{\left(1+\frac{1}{50}\times 0.7\right)} =$$

10. A current mirror as shown in Fig. 10, assume all MOSs are biased with $|V_{ov}|$ = 200mV, $|V_{TH}|$ = 0.5V, I_{REF} = 10uA, $(W/L)_2/(W/L)_1$ = 4, and V_{DD} = 1.8V. **(5%)**

(a) Assume early voltage V_A = 50V, find I_{out} at V_{out} = 0.5V. (2.5%)

(b) Find the minimum output voltage V_{out} for current source I_{out}. (2.5%)

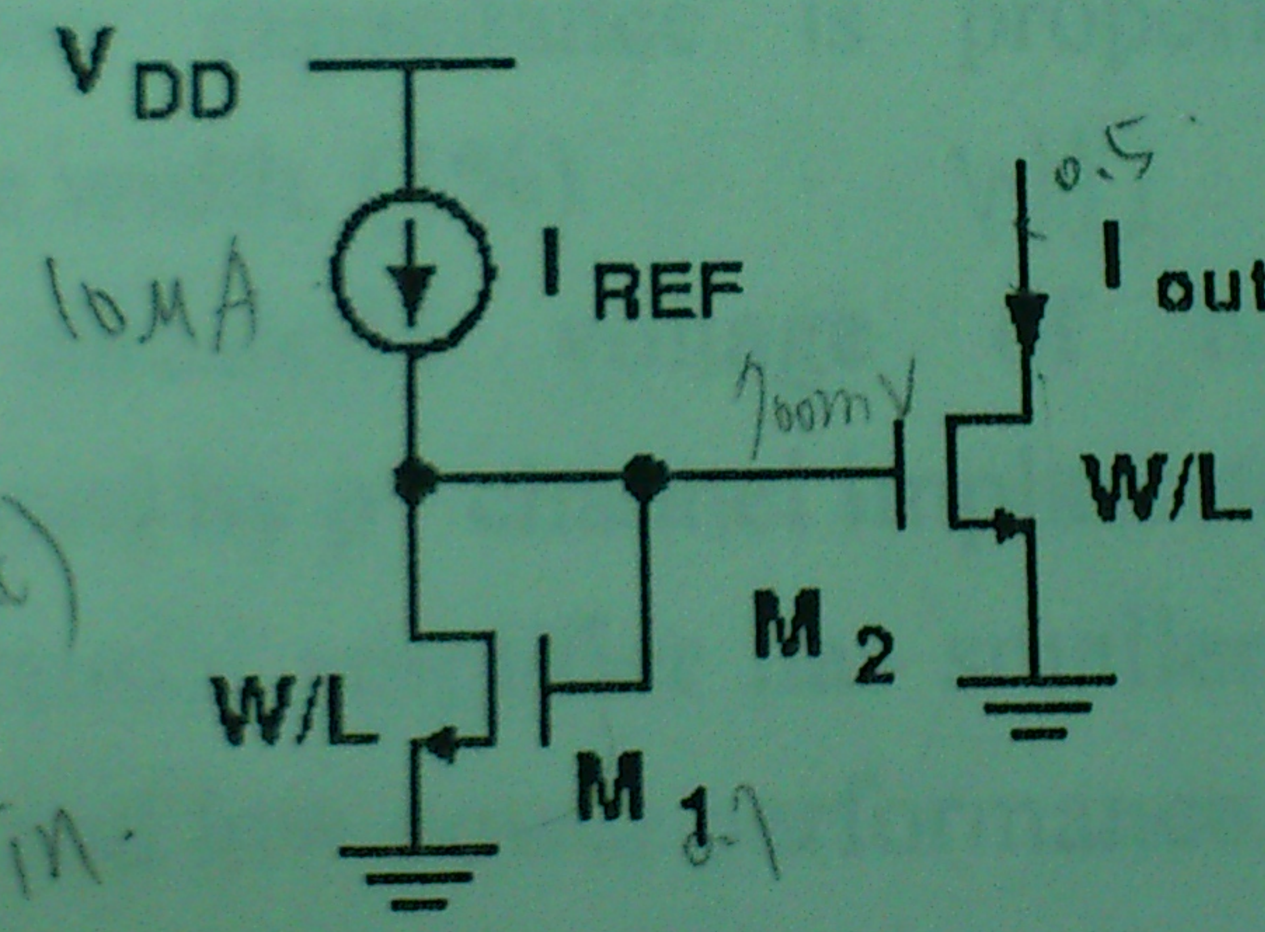

Fig. 10

11. A cascode current mirror as shown in Fig. 11, assume all MOSs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.5V, I_{BIAS} = 10uA, g_m = 2mA/V, r_o = 100kΩ, $(W/L)_1 = (W/L)_3$, $(W/L)_2/(W/L)_1$ = $(W/L)_4/(W/L)_3$ = 4, and V_{DD} = 1.8V. **(5%)**

(a) Find the optimized V_b and related output

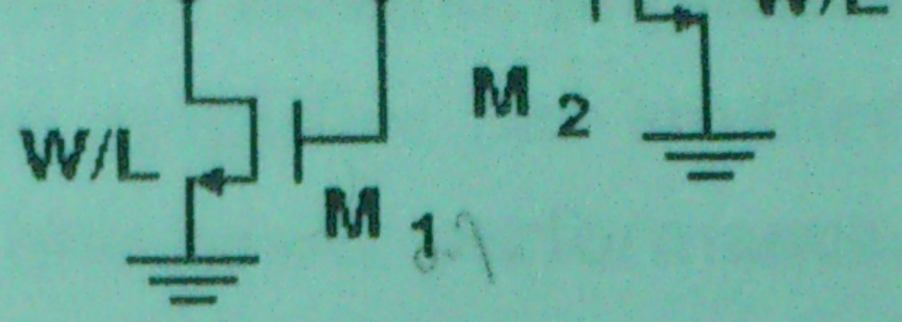

Fig. 10

11. A cascode current mirror as shown in Fig. 11, assume all MOSs are biased with $|V_{ov}| = 200\text{mV}$, $|V_{th}| = 0.5\text{V}$, $I_{BIAS} = 10\text{uA}$, $g_m = 2\text{mA/V}$, $r_o = 100\text{k}\Omega$, $(W/L)_1 = (W/L)_3$, $(W/L)_2/(W/L)_1 = (W/L)_4/(W/L)_3 = 4$, and $V_{DD} = 1.8\text{V}$. **(5%)**

(a) Find the optimized V_b and related output voltage V_{out} for correct current mirror operation. (2.5%)

(b) For $(W/L)_1 = 2\text{um}/4\text{um}$, find the size of ~~Q5~~ M5 to get the optimized V_b. (2.5%)

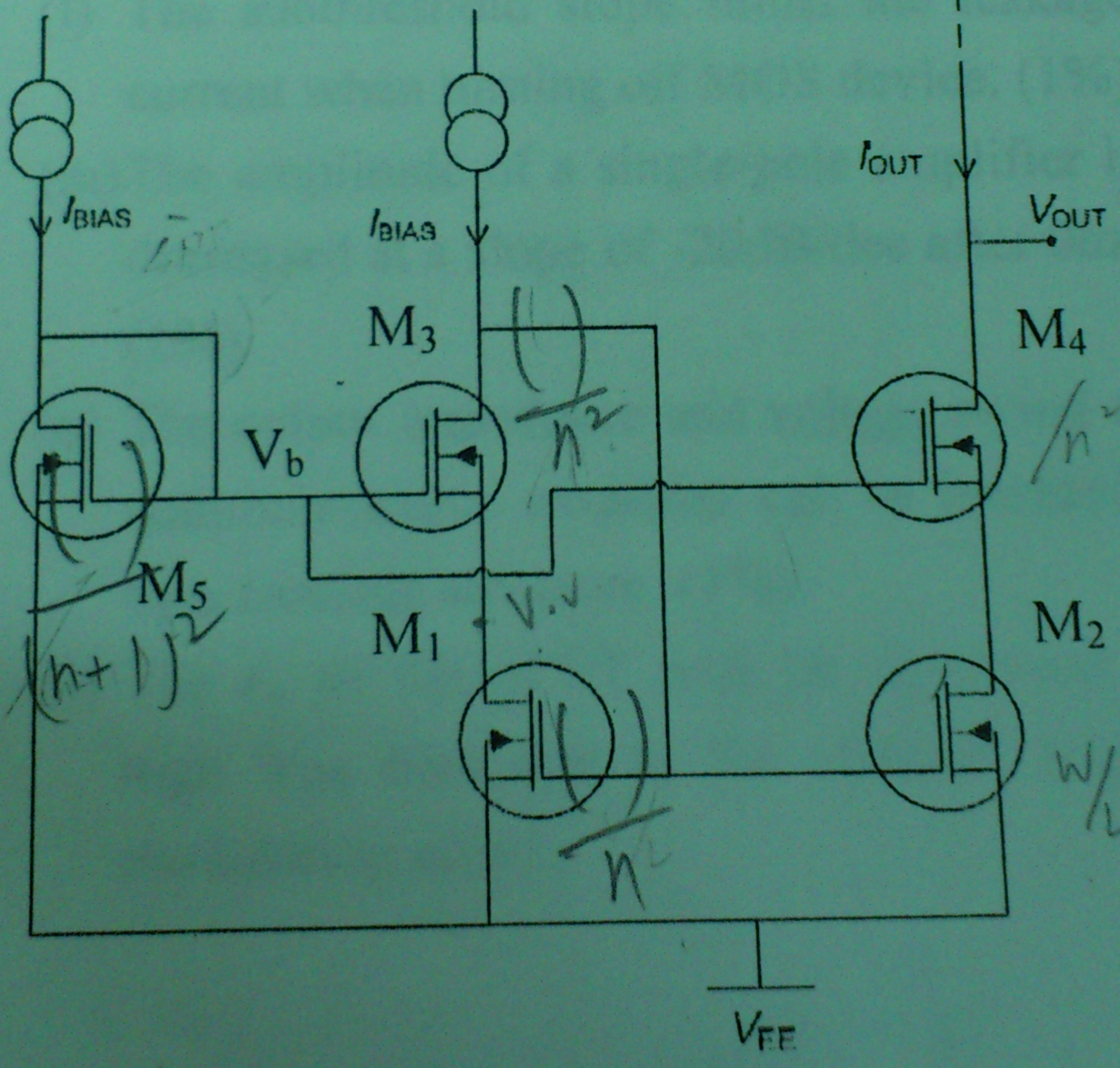

Fig. 11

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12. A common source amplifier is shown in Fig. 12 with the MOSFET bias of g_m = 2mA/V, r_o = 100KΩ, R_S = 10kΩ and R_D = 100kΩ. Assume $C_{GD} = C_{GS}$ = 5fF and $C_{DB} = C_{SB}$ = 2fF. **(10%)**

(a) Use Miller effect to find the equivalent C_{in} at node X and C_{out} at node V_{out} . (5%)

(b) Find the correlated input pole ω_{in} and output pole ω_{out}. (5%)

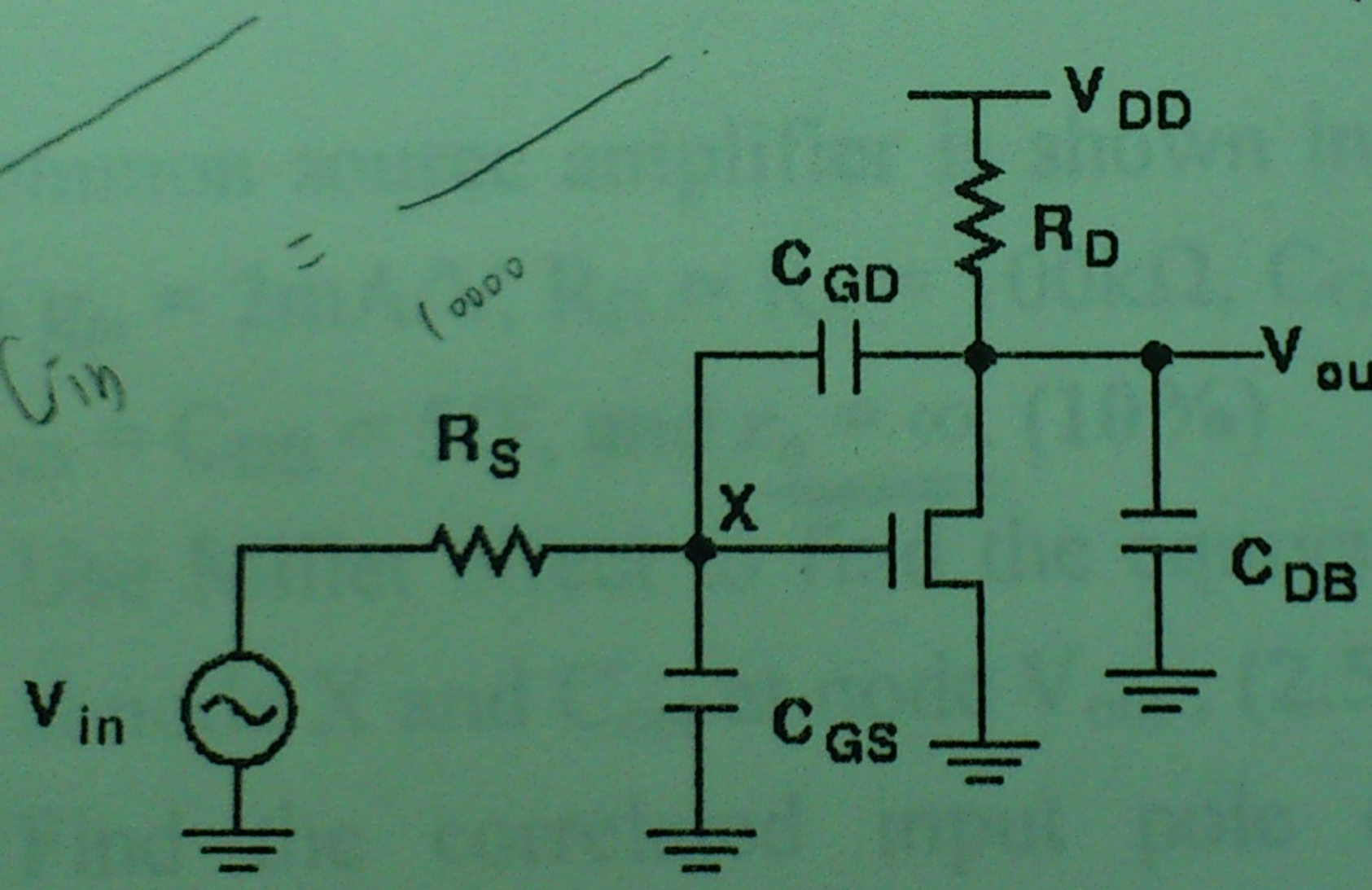

Fig. 12

13. A differential to single-ended amplifier is shown in Fig. 13. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.6V, r_o = 100kΩ, and g_m = 1mA/V. The $I_D(M_5)$ = 10uA and V_{DD} = 1.8V. **(10%)**

(a) Find the minimum input DC bias voltage,

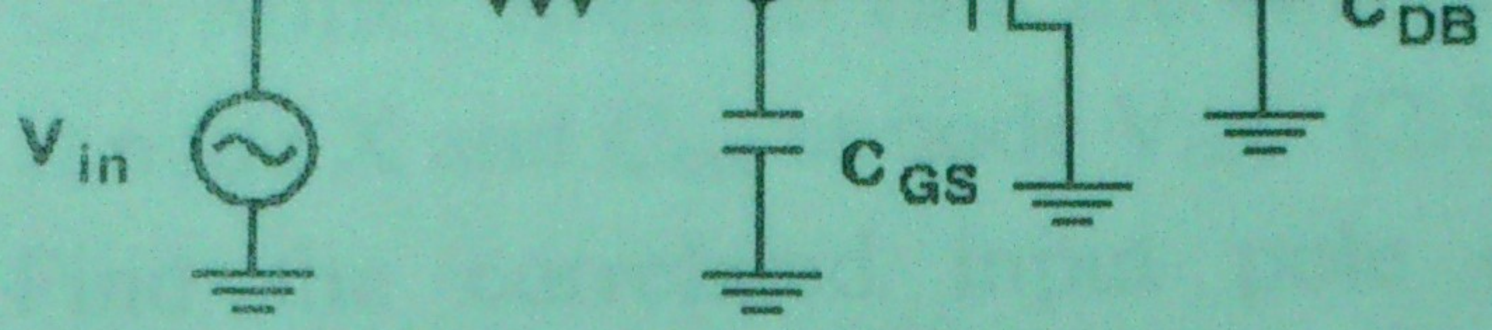

Fig. 12

13. A differential to single-ended amplifier is shown in Fig. 13. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.6V, r_o = 100kΩ, and g_m = 1mA/V. The $I_D(M_5)$ = 10uA and V_{DD} = 1.8V. **(10%)**

(a) Find the minimum input DC bias voltage. (2.5%)

(b) Find the maximum output swing V_{out}. (2.5%)

(c) Find the differential gain $V_{out}/(V_{in1}-V_{in2})$. (2.5%)

(d) Assume $A_{v.CM}$ = $1/(2g_mr_o)$, find the CMRR. (2.5%)

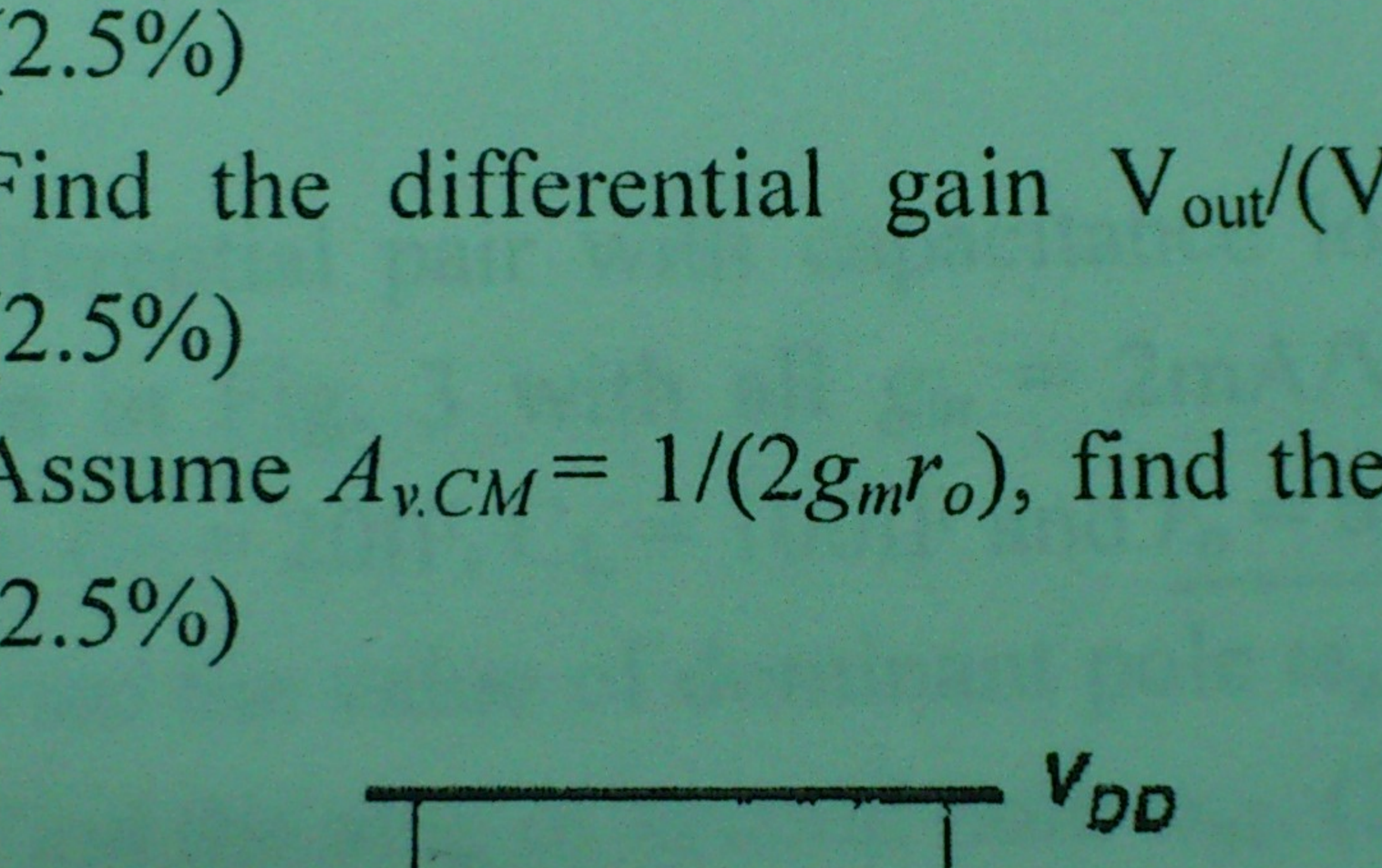

Fig. 13

14. Answer the following questions with TRUE or FALSE: **(15%)**

(a) Source/drain is implanted before gate formation. (1%) F

(b) Source follower is commonly used as a voltage buffer due to its low R_{out}. (1%) T

(c) Common gate amplifier is commonly used as current buffer due to its low R_{in}. (1%) T

(d) Junction capacitance is proportional to device width. (1%) T

(e) The threshold voltage of nMOS is increased by p+ channel implantation. (1%) T

(f) Differential amplifier has smaller common noise and low power performance. (1%) F

(g) Available voltage swing can be increased by using a larger bias current. (1%) F

(h) Chemical vapor deposition is used to form the source/drain region. (1%) F

(i) The transconductance g_m of MOSFET is proportional to *width* at a known constant biasing current. (1%) F

(j) The g_m of pMOS is larger than nMOS at same bias current and device size. (1%) F

(k) The gate-to-body capacitance of a MOS device is almost the same in strong inversion and accumulation region. (1%) T

(l) The subthreshold slope limits the leakage current when turning off MOS device. (1%) T

noise and low power performance. (1%)

(g) Available voltage swing can be increased by using a larger bias current. (1%)

(h) Chemical vapor deposition is used to form the source/drain region. (1%)

(i) The transconductance g_m of MOSFET is proportional to *width* at a known constant biasing current. (1%)

(j) The g_m of pMOS is larger than nMOS at same bias current and device size. (1%)

(k) The gate-to-body capacitance of a MOS device is almost the same in strong inversion and accumulation region. (1%)

(l) The subthreshold slope limits the leakage current when turning off MOS device. (1%)

(m) The amplitude of a single-pole amplifier is decreased at a slope of -20dB/dec after 0hz. (1%)

(n) The output impedance and voltage swing of common-source amplifier can be increased by a cascode structure. (1%)

(o) The r_o of MOSFET will be decreased at high V_{DS} bias due to the channel length modulation effect.

$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$

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