2013 Analog IC: Final Examination (130%)

1. Derive the equations of Miller effect to express Z_1 and Z_2 in terms of A and Z. **(5%)**

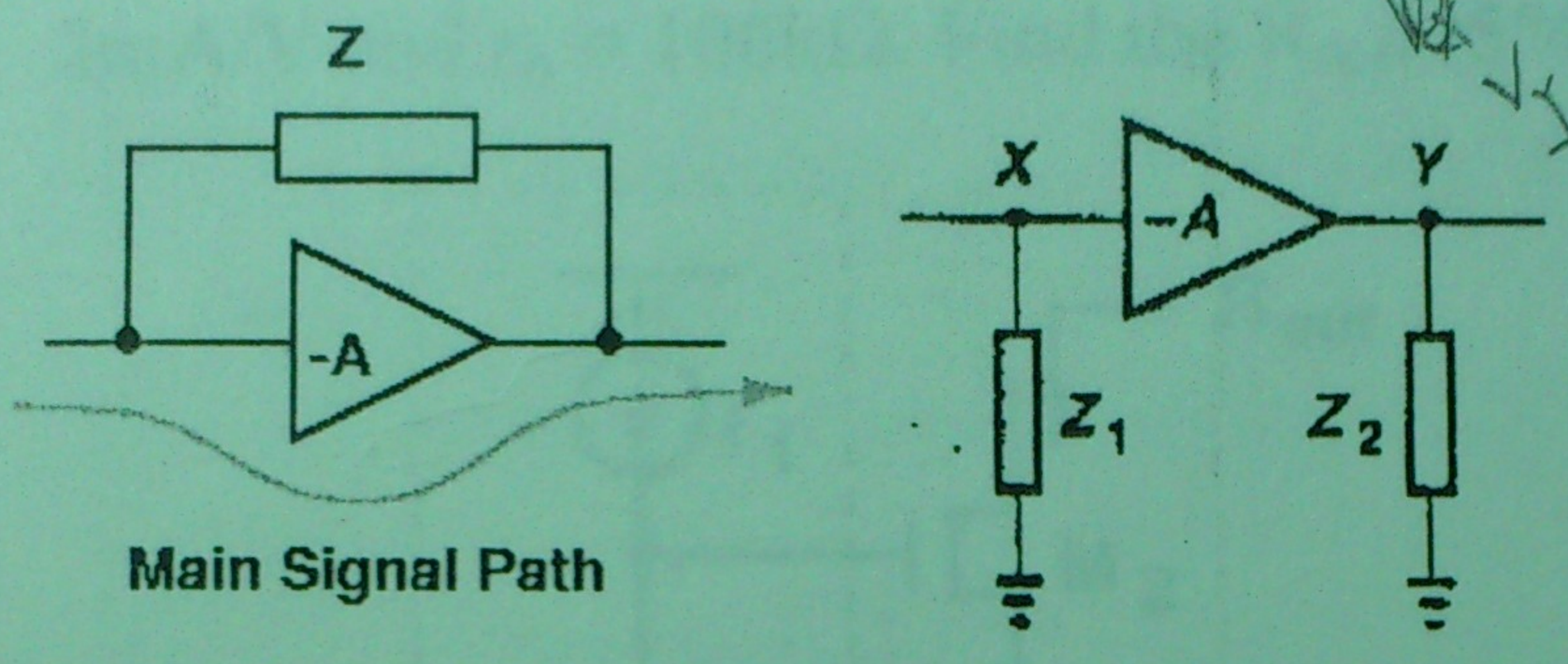

Fig. 1

2. A common source amplifier is shown in Fig. 2 with g_m = 2mA/V, $R_D = R_S$ = 100kΩ, C_{GS} = 5fF = $C_{GD} = C_{DB}$ = 5fF, and $r_o = \infty$. **(10%)**
   (a) Use Miller effect to find the equivalent C_{in} at node X and C_{out} at node V_{out} . (2.5%)
   (b) Find the correlated input pole ω_{in} and output pole ω_{out}. (2.5%)
   (c) Derive and find the zero ω_z. (2.5%)
   (d) Find Z_{in} at high frequency with $Z(C_{GD})$=0. (2.5%)

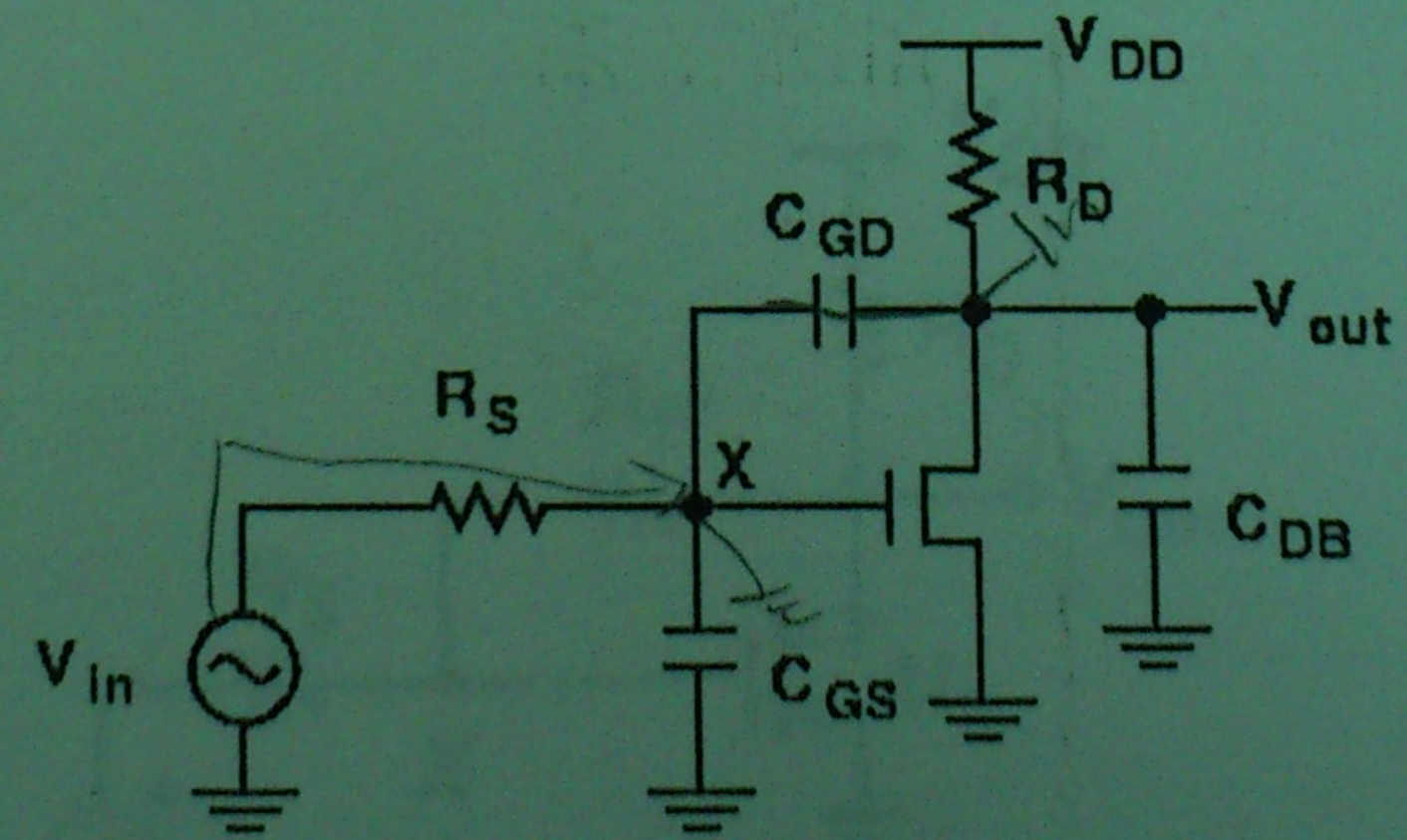

Fig. 2

3. A differential pair with capacitance loading is shown in Fig. 3 with all g_m = 2mA/V, R_{out} = 50kΩ, C_E = 20fF, C_L = 100fF and $r_o = \infty$. **(10%)**
   (a) Find the value of dominant pole ω_{p1}. (2.5%)

(d) Find Z_{in} at high frequency with $Z(C_{GD})=0$. (2.5%)

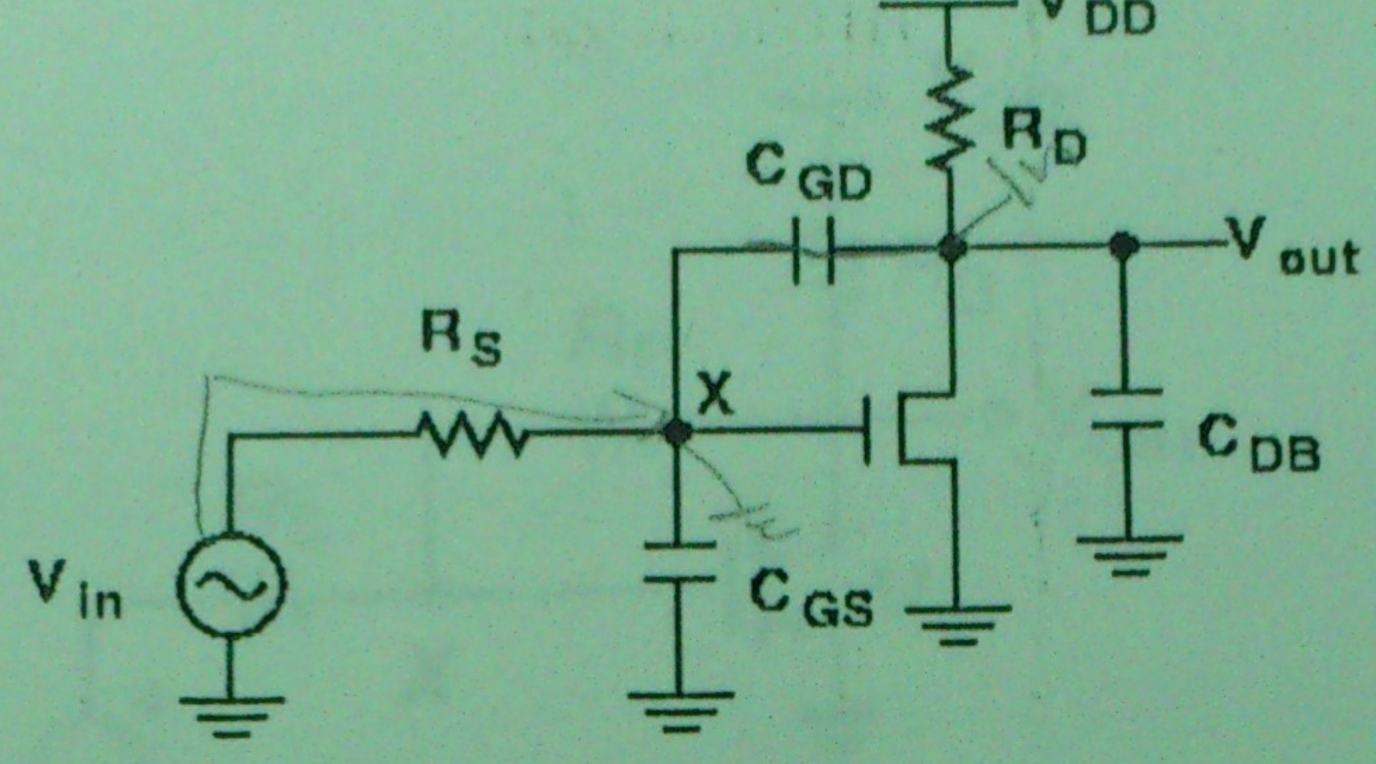

Fig. 2

3. A differential pair with capacitance loading is shown in Fig. 3 with all g_m = 2mA/V, R_{out} = 50kΩ, C_E = 20fF, C_L = 100fF and $r_o = \infty$. **(10%)**

(a) Find the value of dominant pole ω_{p1}. (2.5%)

(b) Find the alue of second pole ω_{p2}. (2.5%)

(c) Find the value of zero ω_z. (2.5%)

(d) Explain the relation of ω_z and ω_{p2}. (2.5%)

6.

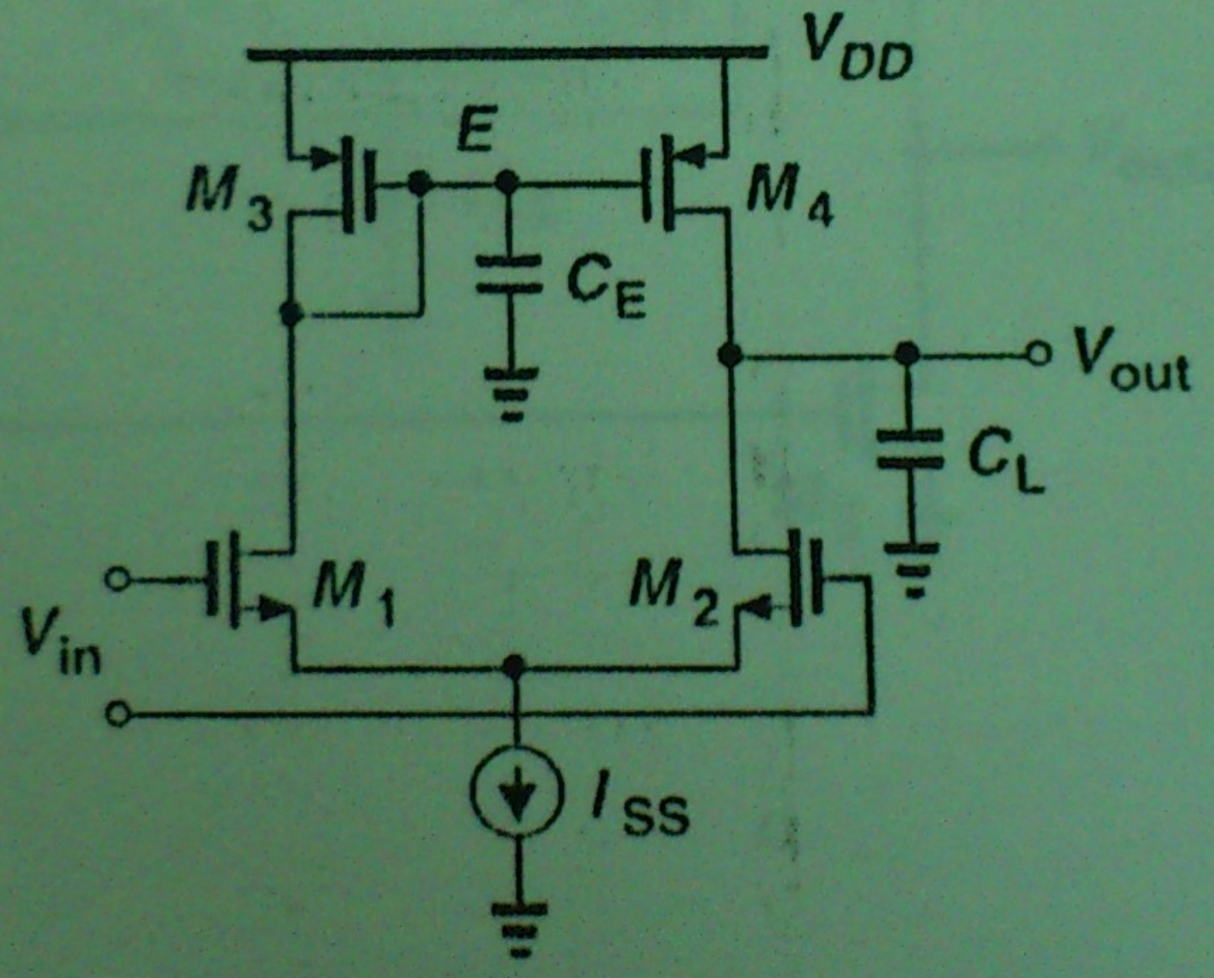

Fig. 3

$\frac{1}{sC(1+A)}$ $Z = \frac{1}{sC}$

$Z' = \frac{1}{sC(1+\frac{1}{A})}$

4. In Fig. 4, M_1 and M_2 are biased with g_m = 1mA/V and r_o = 100kΩ. The thermal noise of M_1 (M_2) is $\overline{i_n^2} = 4kTg_m(2/3)$, $4kT$ = 1.5x10^{-20} V^2/(Hz*Ω). **(10%)**

(a) Find the output referred noise $\overline{v_{n,out}^2}$. **(4%)**

(b) Find the input referred noise $v_{n,in}^2$. **(4%)**

(c) How to modify g_{m1} and g_{m2} to improve the noise performance? **(2%)**

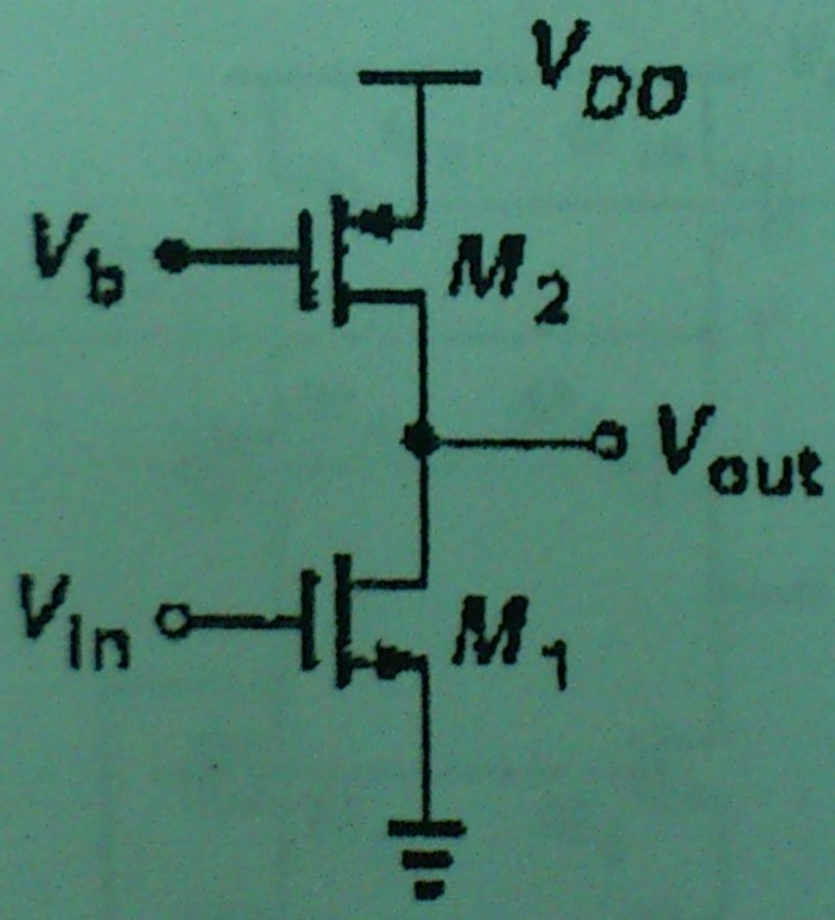

Fig. 4

5. In Fig. 5, the input and output impedance of feed-forward amplifier are R_{in} and R_{out}. **(10%)**

(a) Find the loop gain. (2%)

(b) Find the closed loop gain. (2%)

(c) Find the input impedance of closed-loop amplifier. (2%)

(d) Find the output impedance of closed-loop

Fig. 4

5. In Fig. 5, the input and output impedance of feed-forward amplifier are R_{in} and R_{out}. **(10%)**
   (a) Find the loop gain. (2%)
   (b) Find the closed loop gain. (2%)
   (c) Find the input impedance of closed-loop amplifier. (2%)
   (d) Find the output impedance of closed-loop amplifier. (2%)
   (e) Explain ***bandwidth modification*** of closed loop system compared to open loop. (2%)

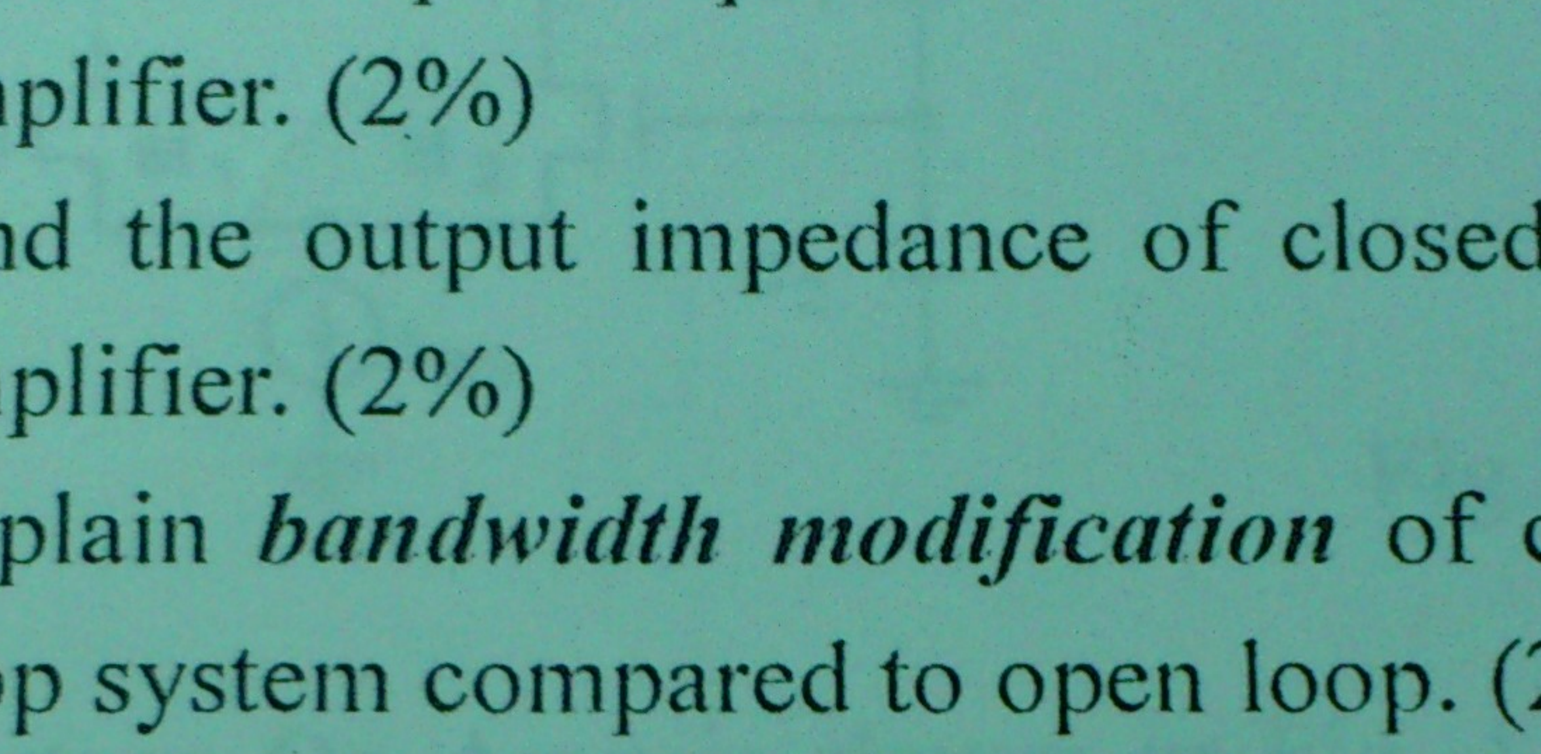

Fig. 5

6. Explain the following terminologies **(10%)**
   (a) Power Spectrum (Spectral) Density. (2%)
   (b) Flicker noise. (2%)
   (c) Corner Frequency. (2%)
   (d) Phase margin. (2%)
   (e) Noise bandwidth. (2%)

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7. Fig 7 shows an impedance boosting circuit with $R_S = 50k\Omega$. M_2 and M_3 are biased with $g_m = 2mA/V$ and $r_o = 100k\Omega$. Find the R_{out}. **(5%)**

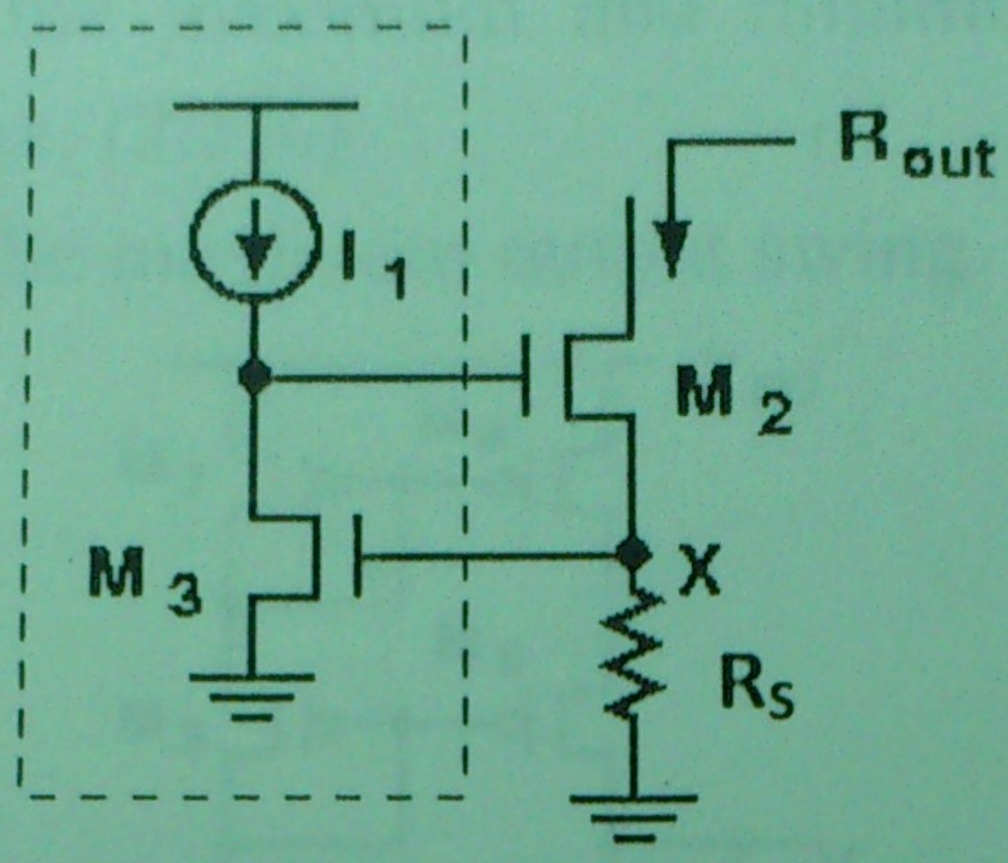
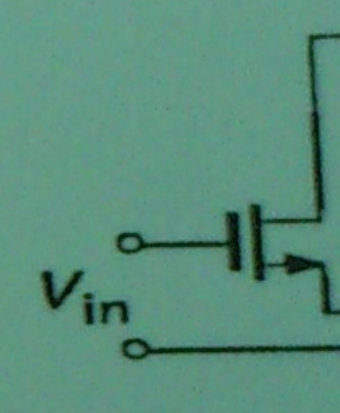


Fig. 7

8. A shunt-series feedback amplifier as shown in Fig. 8 is biased with $g_m = 2mA/V$, $R_D = R_S = 100k\Omega$, $R_F = 50k\Omega$ and $r_o = \infty$. **(10%)**



(a) Find the feedback factor. (2%)

(b) Find the open-loop gain with loading effect. (4%)

(c) Find the closed-loop gain V_{out}/V_{in}. (4%)

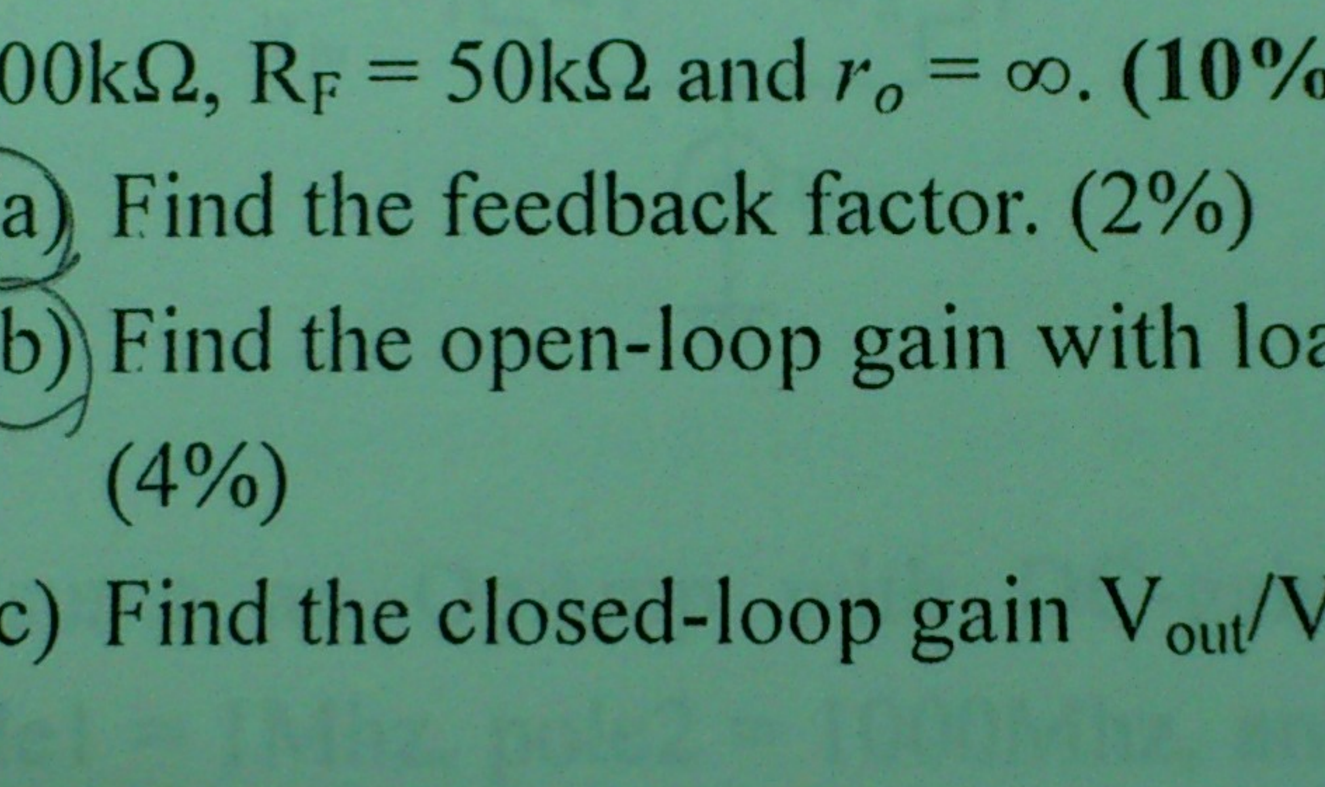


Fig. 10

9. Sketch a common-mode feedback circuit for the 2-stage Op Amp as shown in Fig. 9. **(5%)**

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(b) Find the open-loop gain with loading effect. (4%)

(c) Find the closed-loop gain V_{out}/V_{in}. (4%)

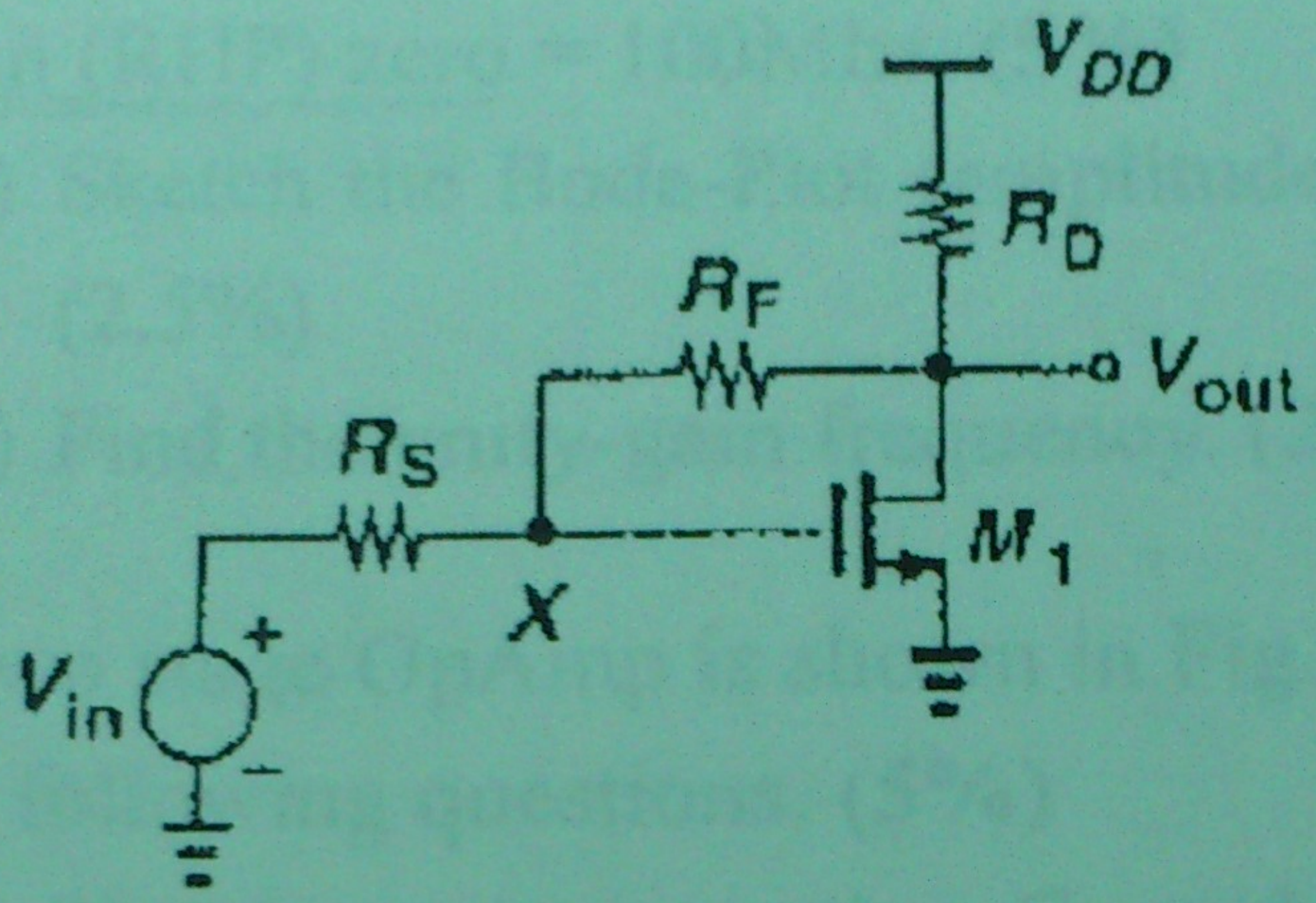

Fig. 10

11.

9. Sketch a common-mode feedback circuit for the 2-stage Op Amp as shown in Fig. 9. (5%)

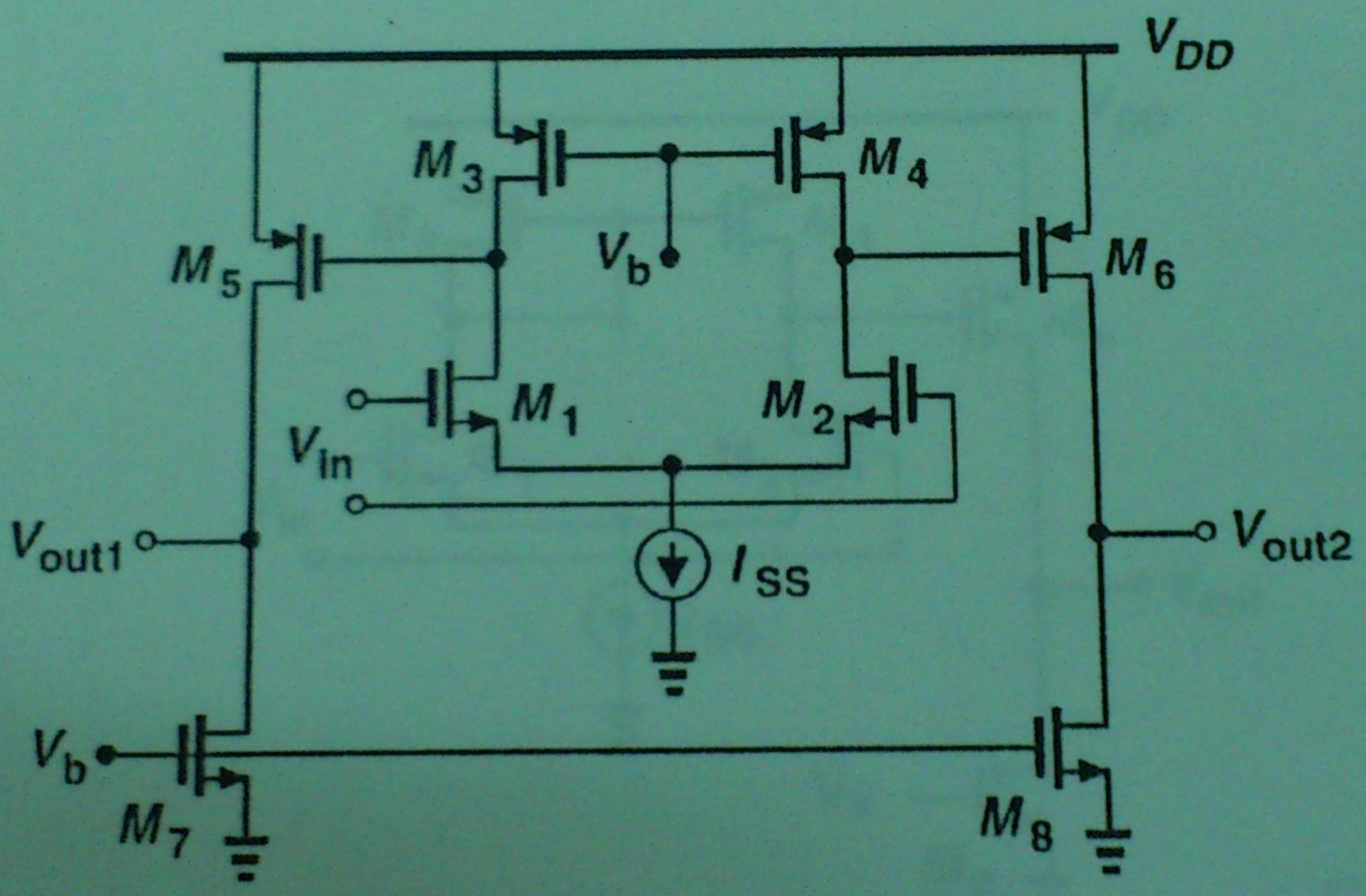

Fig. 9

10. Find slew rates of the following Op Amps in Fig. 10 with I_{SS} = 10uA. **(10%)**

(a) Folded cascade Amp with C_L = 2pF. (2.5%)

(b) 2-stage OP Amp with C_1 = 0.2pF and C_2 = 0.4pF. (2.5%)

(c) With $I_d(M_9)$ = 8uA, explain the behavior of node voltage X when slewing. (2.5%)

(d) Sketch a possible solution of condition (c). (2.5%)

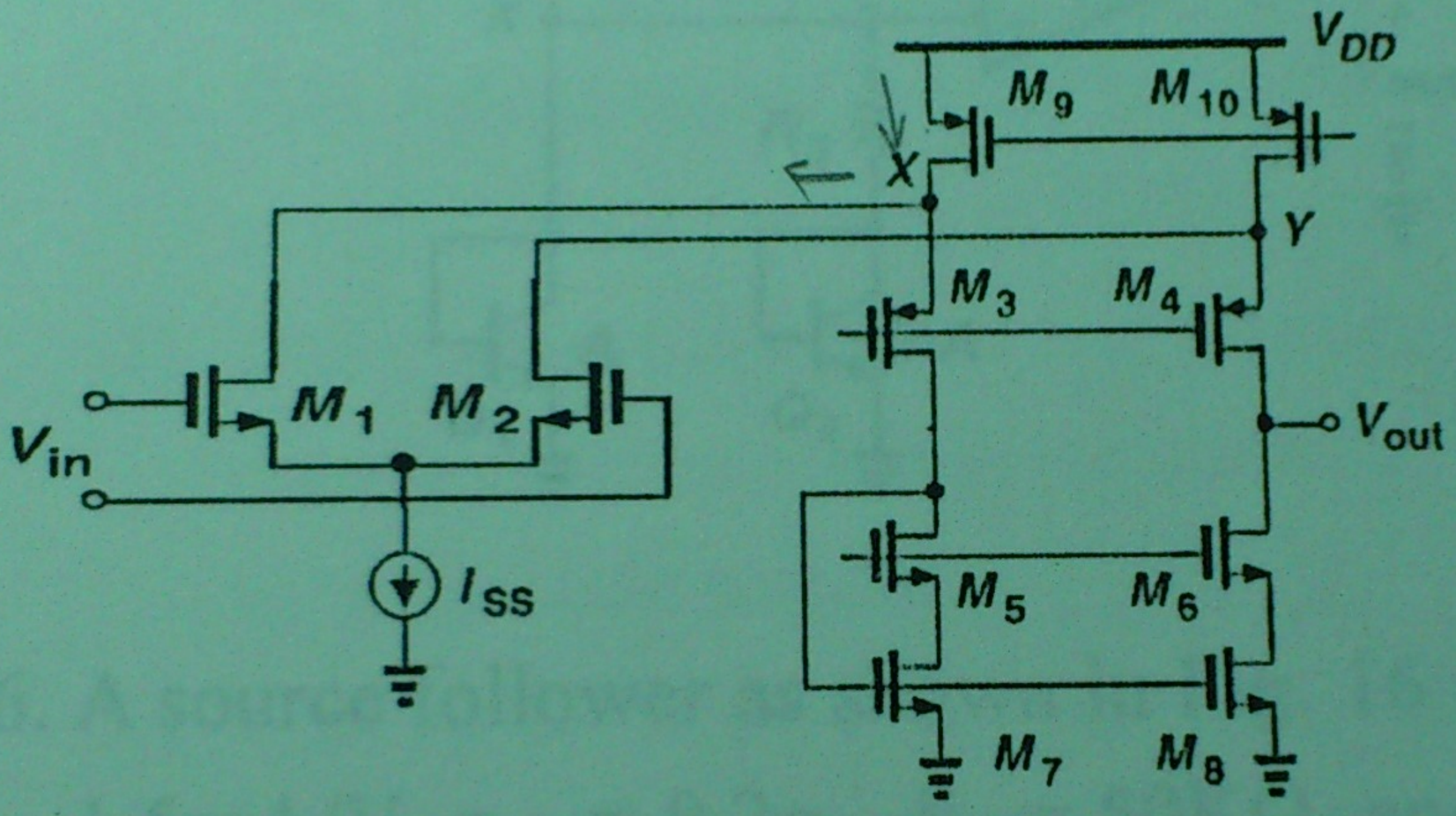

Fig. 10(a)

Fig. 10(b)

11. A two-stage Op Amp is shown in Fig. 11 with $R_{out1} = R_{out2}$ = 100kΩ, C_{out1} = 50fF, C_{out2} = 10fF, and A_{v1} = ~~10~~ −10, A_{v2} = ~~100~~ −100. **(5%)**

(a) Find frequencies of 1st and 2nd poles.

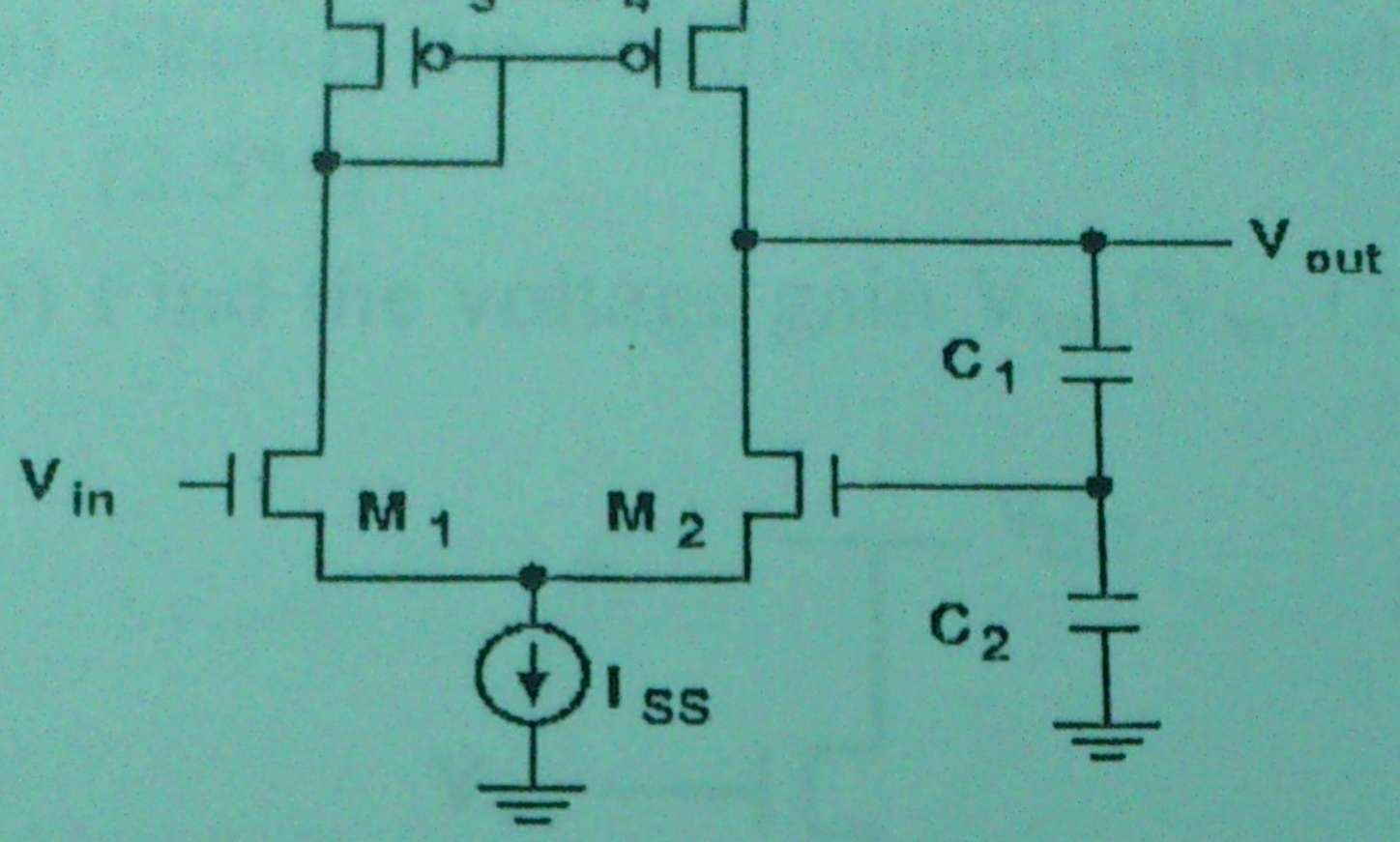

Fig. 10(b)

11. A two-stage Op Amp is shown in Fig. 11 with $R_{out1} = R_{out2} = 100k\Omega$, $C_{out1} = 50fF$, $C_{out2} = 10fF$, and $A_{v1} = -10$, $A_{v2} = -100$. **(5%)**

(a) Find frequencies of 1st and 2nd poles. (2.5%)

(b) Use Miller compensation to move the 1st pole to become 0.001x smaller. Sketch the compensated circuit and find the value of Cc. (2.5%)

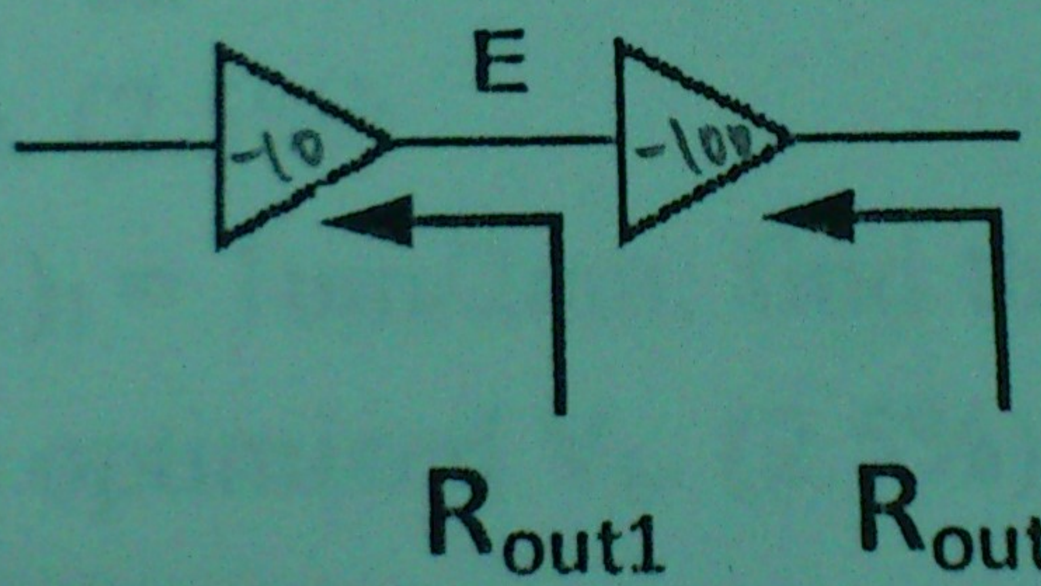

Fig. 11

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12. A telescopic amplifier is shown in Fig. 12 with V_{TH} = 0.6V and V_{ov} = 200mV for each MOS, and V_{b1} = 1.2V. **(5%)**

(a) Find the maximum and minimum output voltage. (2.5%)

(b) Find the maximum output swing. (2.5%)

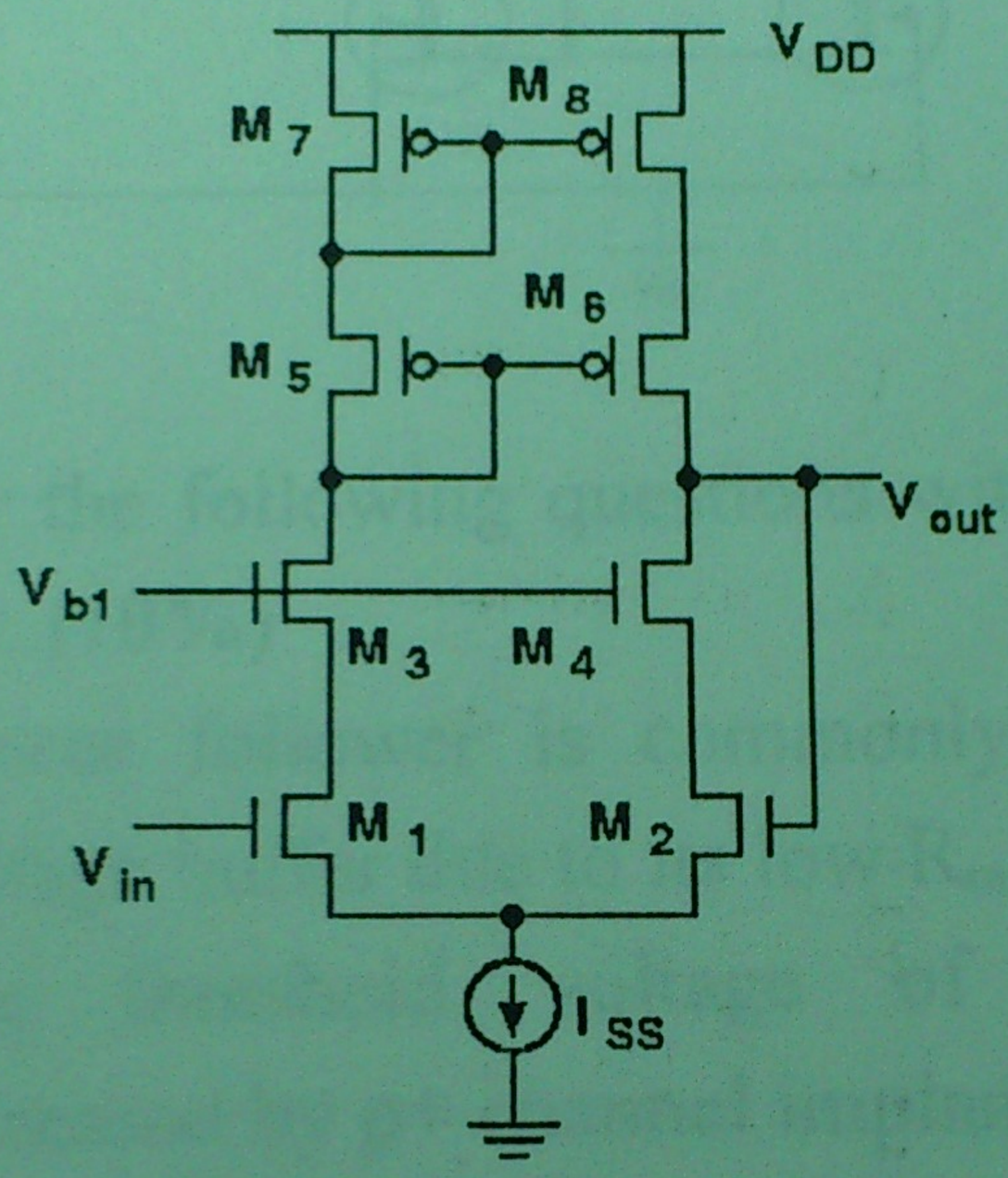


Fig. 12

13. Assume an OpAmp with DC-gain = 60dB, pole1 = 1Mhz, pole2 = 1000Mhz, and right half plan (RHP) zero = 100Mhz. **(5%)**

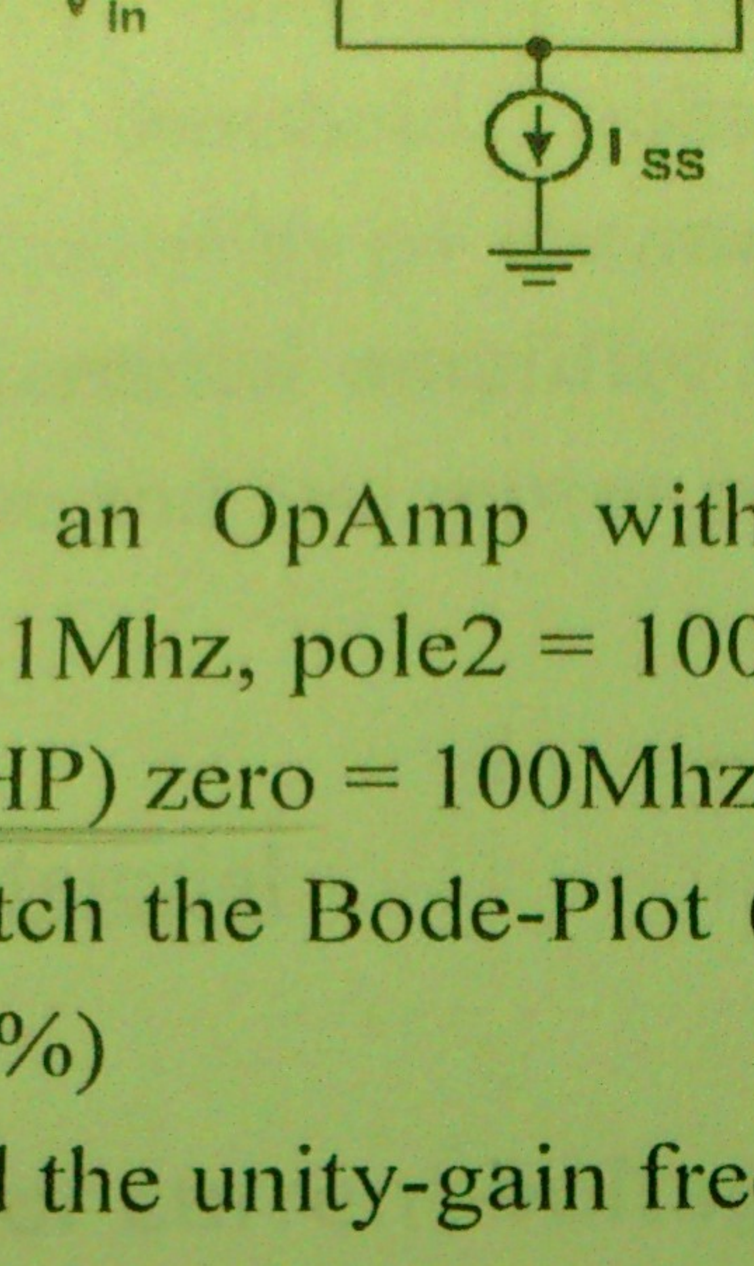
(a) Sketch the Bode-Plot (amplitude & phase). (2.5%)

(b) Find the unity-gain frequency. (2.5%)

14. A two stage OpAmp is shown in Fig. 14, answer the following questions. **(5%)**

(a) Sketch a compensation Cc and explain the pole-splitting effect. (2.5%)

(b) Explain the right half plane zero effect and provide one solution. (2.5%)



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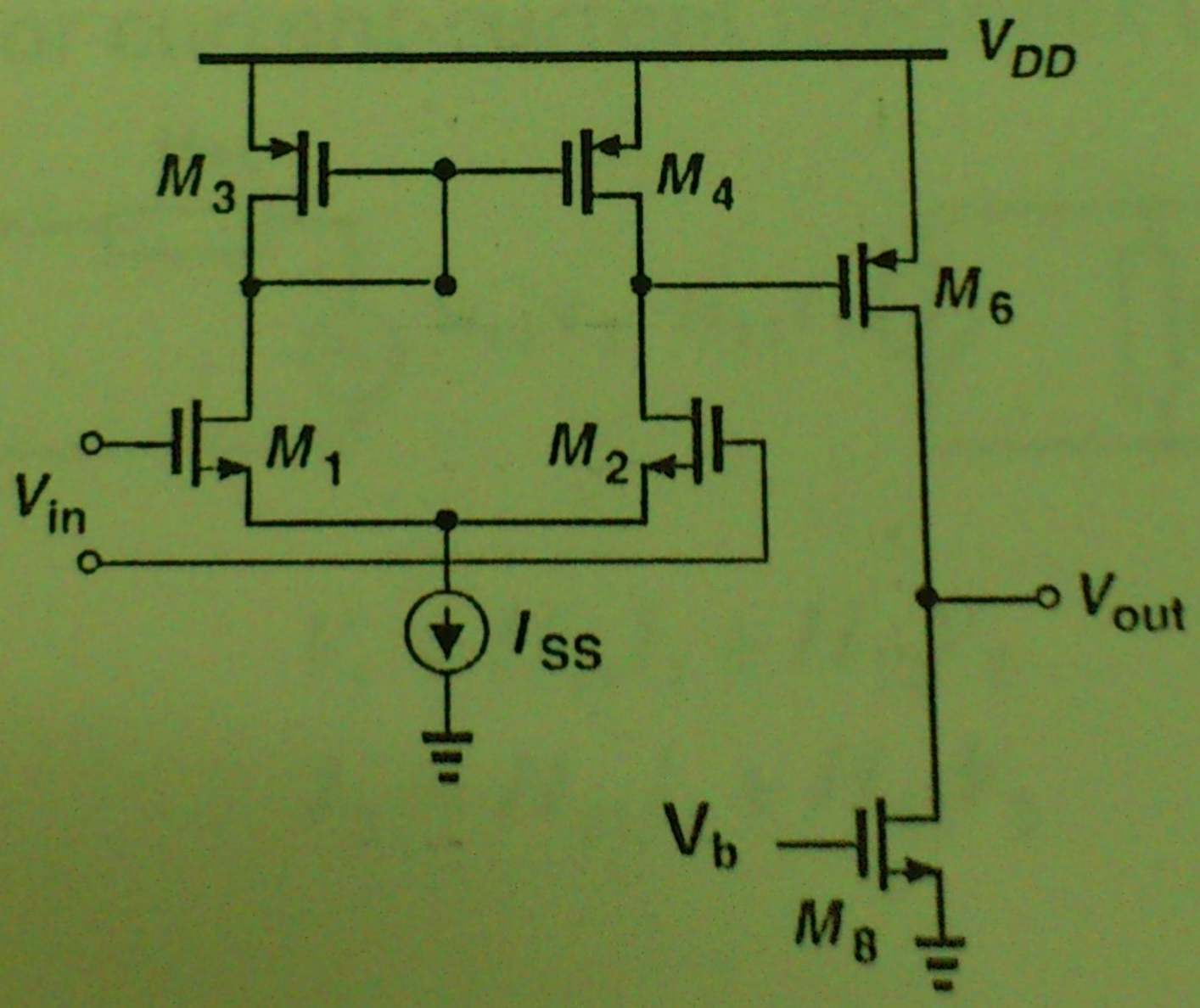

Fig. 14

15. A Bandgap voltage reference is shown in Fig. 15. Assume n = 8, $I_{C1} = I_{C2} = I_{D5}$, $V_{BE1} = 0.7V$, $\Delta V_{BE}(Q_1 - Q_2) = V_T \ln(n)$, $dV_T/dT = 0.08mV/K$, $dV_{BE3}/dT = -1.5mV/K$. **(5%)**

(a) Design R_2/R_3 to get $dV_{out}/dT = 0$. (2.5%)

(b) Find the V_{out} = ? volts in (a). (2.5%)

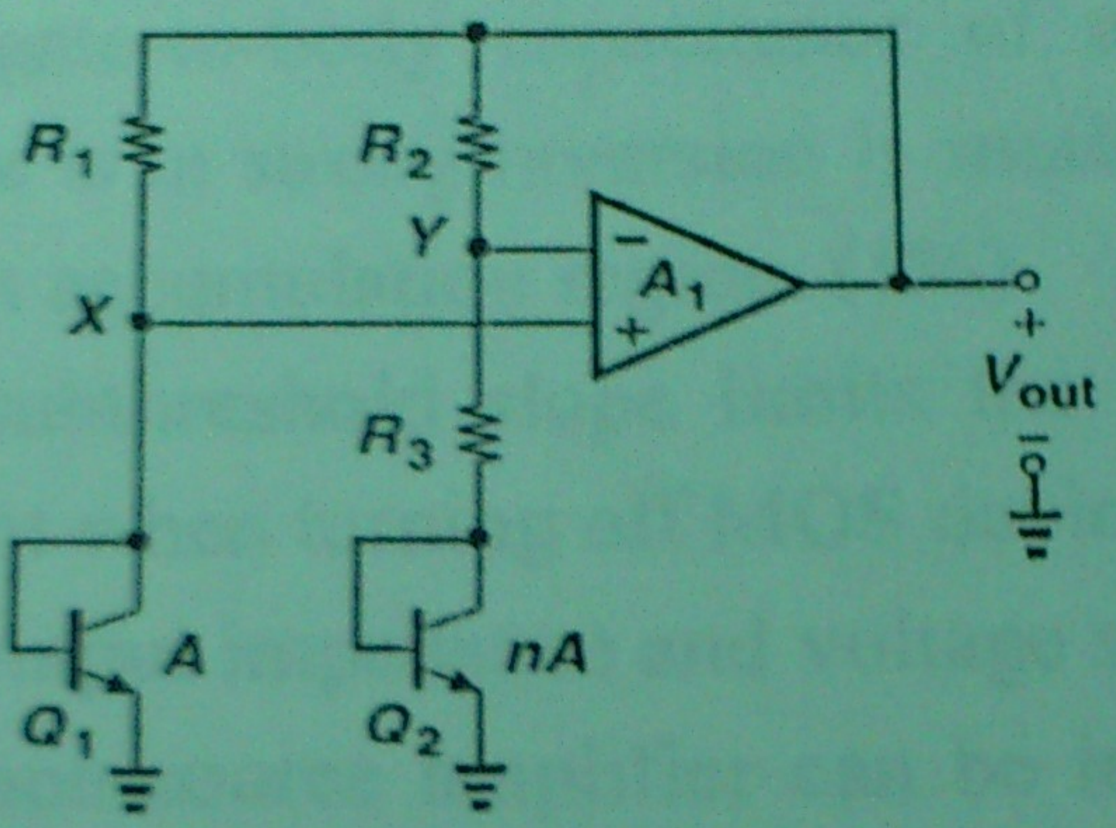

Fig. 15

16. A source follower as shown in Fig. 16 with g_m = 1.5mA/V, $g_{mb} = 0.2g_m$, $R_S = 50K\Omega$, and $r_o = \infty$. **(5%)**

(a) Sketch the small signal equivalent circuit. (2.5%)

(b) Find the voltage gain V_{out}/V_{in}. (2.5%)

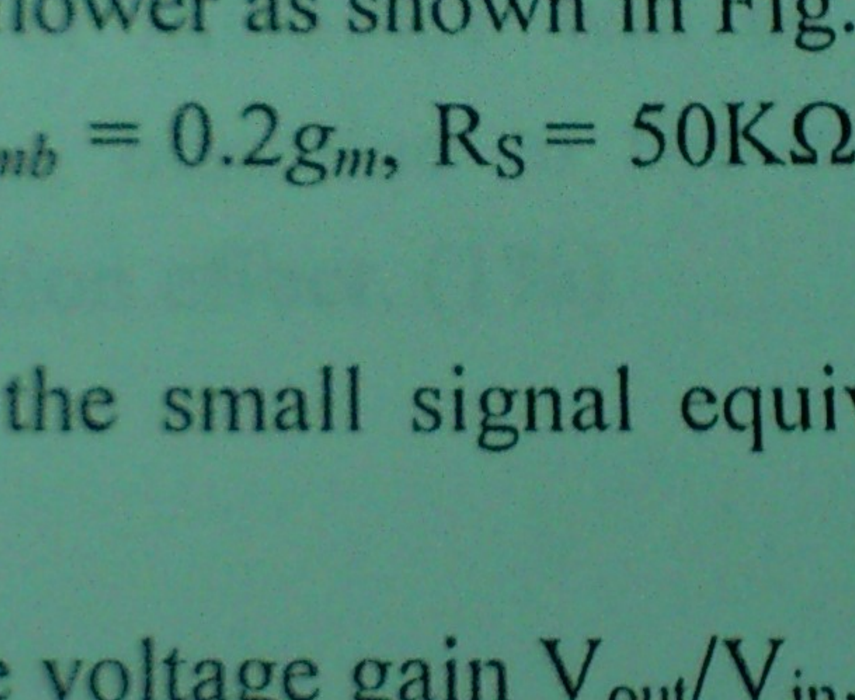

Fig. 16

17. A cascode current mirror as shown in Fig. 17, assume $Q_1 \sim Q_4$ are biased with $|V_{ov}| = 200mV$, $|V_{th}| = 0.6V$, $I_{BIAS} = 5uA$, $g_m = 2mA/V$, r_o =

Fig. 15

16. A source follower as shown in Fig. 16 with g_m = 1.5mA/V, $g_{mb} = 0.2g_m$, R_S = 50KΩ, and $r_o = \infty$. **(5%)**

(a) Sketch the small signal equivalent circuit. (2.5%)

(b) Find the voltage gain V_{out}/V_{in}. (2.5%)

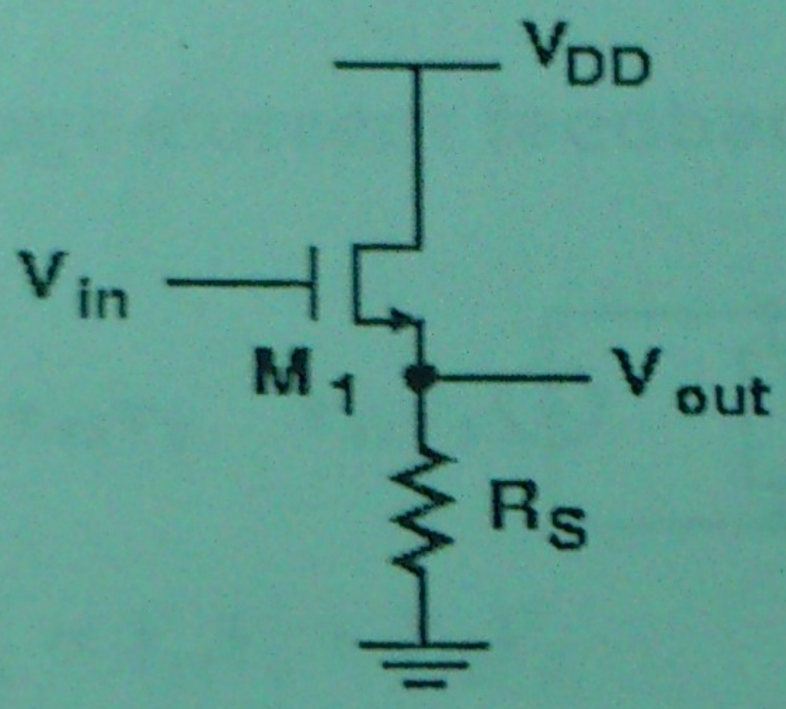

Fig. 16

17. A cascode current mirror as shown in Fig. 17, assume Q_1~Q_4 are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.6V, I_{BIAS} = 5uA, g_m = 2mA/V, r_o = 100kΩ, $(W/L)_1 = (W/L)_3$, $(W/L)_2/(W/L)_1 = (W/L)_4/(W/L)_3 = 4$, and V_{DD} = 1.8V. **(5%)**

(a) Find the optimized V_b and related output voltage V_{out} for correct current mirror operation. (2.5%)

(b) For $(W/L)_1$ = 1um/2um, find the size of Q5 to get the optimized V_b. (2.5%)

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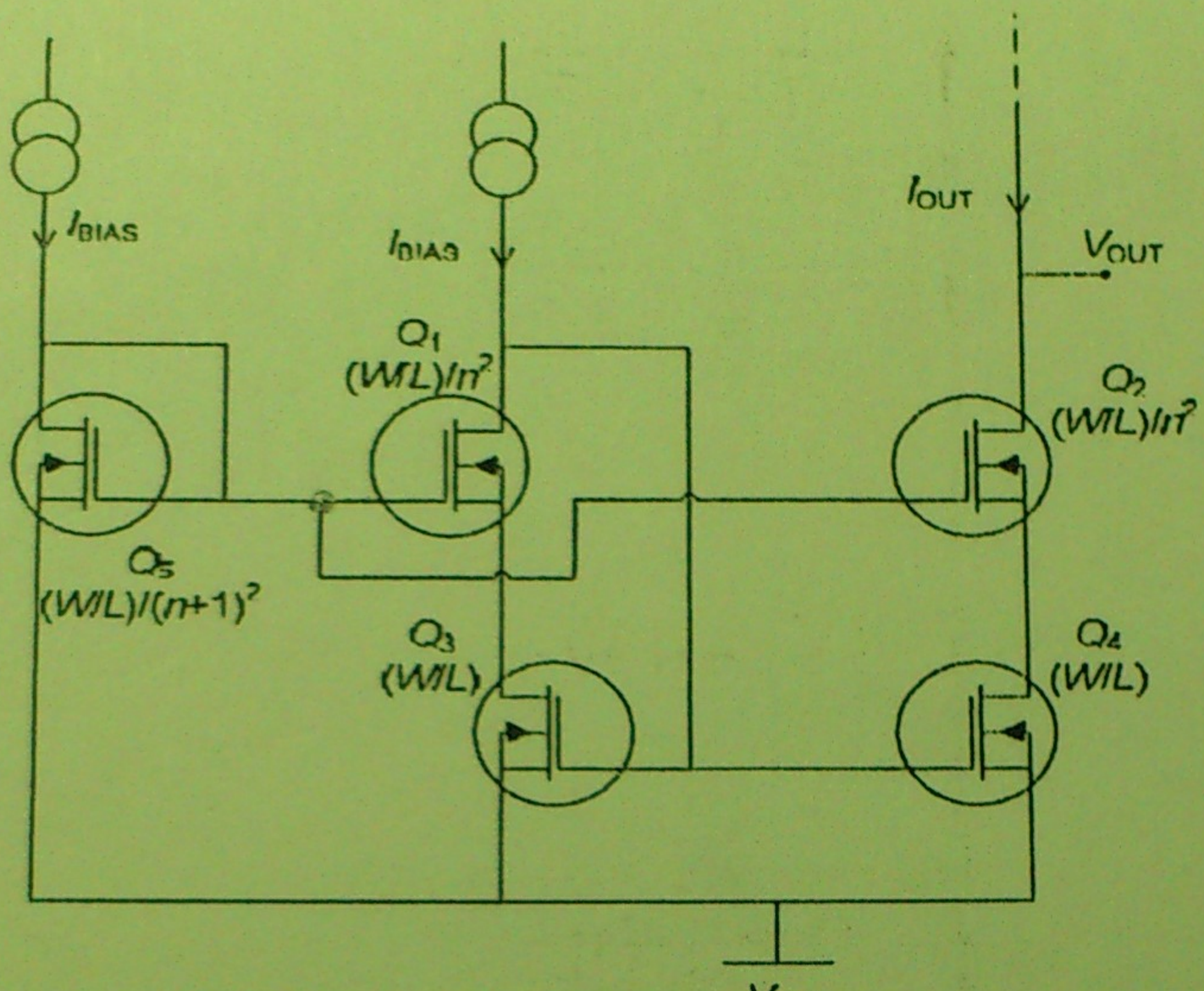


Fig. 17

18. Answer the following questions with TRUE or FALSE: **(10%)**

(a) Source follower is commonly used as a voltage buffer due to its low R_{out}. (1%)

(b) The threshold voltage of nMOS is increased by p+ channel implantation. (1%)

(c) Differential amplifier has smaller common noise and low power performance. (1%)

(d)

(e)

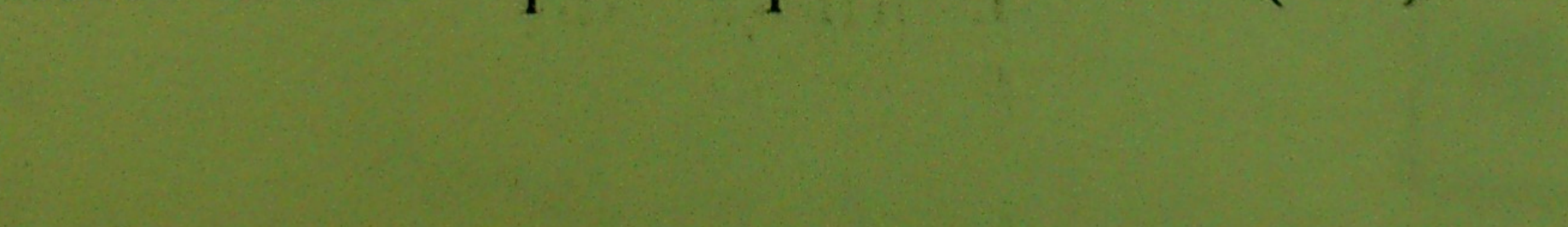
(f)

(g)

$g_m = \sqrt{\mu(\omega)}$

Reference Material

- For current-voltage feedback (Z)



(d) Junction capacitance is proportional to device length. (1%)

(e) The transconductance g_m of MOSFET is proportional to V_{ov} at a known constant biasing current. (1%)

(f) The g_m of pMOS is larger than nMOS at same bias current and device size. (1%)

(g) The gate-to-body capacitance of a MOS device is in strong inversion is smaller than that in accumulation region. (1%)

(h) The subthreshold slope limits the leakage current when turning off MOS device. (1%)

(i) The output impedance and voltage swing of common-source amplifier can be increased by a cascode structure. (1%)

(j) The r_o of MOSFET will be decreased at high V_{DS} bias due to the channel length modulation effect. (1%)

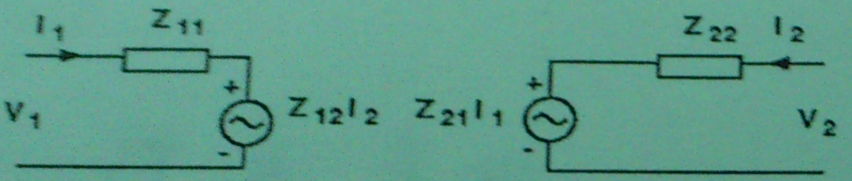
➢ For voltage-current feedback (Y)

noise and low power performance. (1%)

high V_{DS} bias due to the channel length modulation effect. (1%)

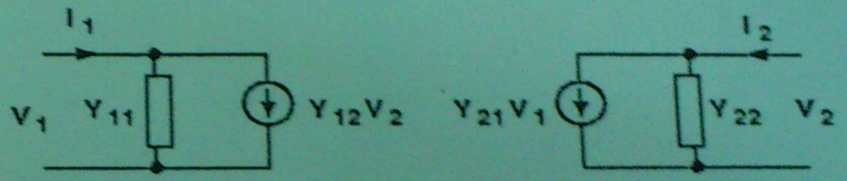
Reference Material

- For current-voltage feedback (Z)



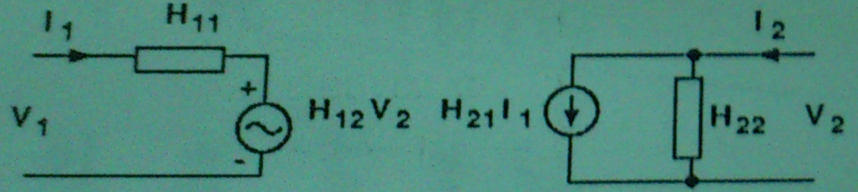
$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

- For voltage-current feedback (Y)



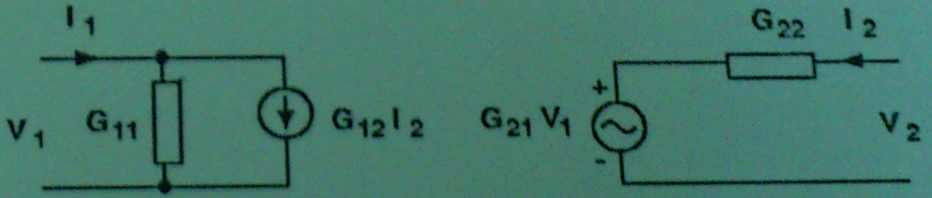
$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

- For current-current feedback (H)



$$V_1 = H_{11}I_1 + H_{12}V_2$$
$$I_2 = H_{21}I_1 + H_{22}V_2$$

- For voltage-voltage feedback (G)



$$I_1 = G_{11}V_1 + G_{12}I_2$$
$$V_2 = G_{21}V_1 + G_{22}I_2$$