1. Answer definitions of the following effects and explain the physical mechanisms. **(10%)**
   (a) Channel Length Modulation effect. (2%)
   (b) Mobility Degradation. (2%)
   (c) Drain Induced Barrier Lowering. (2%)
   (d) Body effect. (2%)
   (e) Velocity Saturation. (2%)

2. Sketch the small signal model of MOSFET in Fig. 2 with g_m, g_{mb}, r_o, and all the parasitic capacitances. **(5%)**

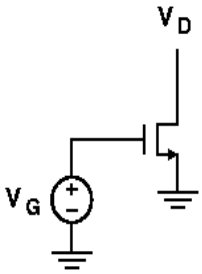

Fig. 2

3. Sweep V_G in Fig. 2 with a constant V_D, the C_{GS} and C_{GD} curves are shown in Fig. 3. **(10%)**
   (a) Find values of C1, C2, and C3 in W, L, C_{ox}, and C_{ov}. (6%)
   (b) Define the operation regions I, II, and III. (4%)

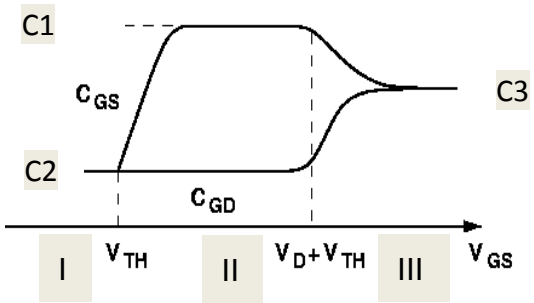

Fig. 3

4. Write down the drain current equations of MOSFET in triode and saturation region with channel length modulation effect. **(5%)**

5. Fig. 5 is a layout of CMOS inverter. **(5%)**
   (a) Identify and index all the name of layers. (2.5%)
   (b) Make the orders of masks in semiconductor process flow. (2.5%)

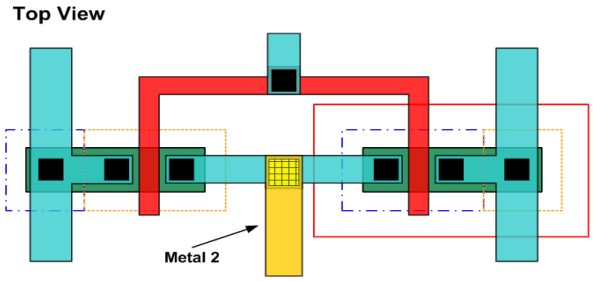

Fig. 5

6. Derive the equation of voltage gain V_{out}/V_{in} of amplifier as shown in Fig. 6 in terms of $g_{m<n>}$, $g_{mb<n>}$ and $r_{o<n>}$ **(5%)**

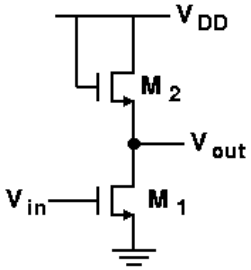

Fig. 6

7. Assume $r_o = \infty$, $g_{mb} \neq 0$ in the circuit of Fig. 7. **(10%)**
   (a) Sketch the small signal equivalent circuit. (3%)
   (b) Find the short circuit transconductance G_m of this amplifier. (3%)
   (c) Find the voltage gain V_{out}/V_{in}. (4%)

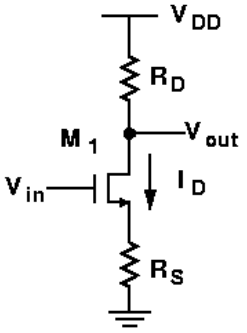

Fig. 7

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8. A source follower as shown in Fig. 8. **(10%)**
   (a) Sketch the small signal equivalent circuit. (3%)
   (b) Derive the equation V_{out}/V_{in} of amplifier in terms of $g_{m<n>}$, $g_{mb<n>}$, and R_S. Assume there is no λ effect. (4%)
   (c) Derive output impedance R_{out} with Rs=∞. (3%)

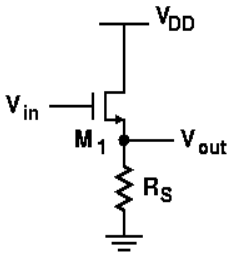

Fig. 8

9. A differential pair is shown in Fig. 9. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV and $|V_{th}|$ = 0.5V. The $I_D(M_3)$ = 20uA, g_{m1} = g_{m2} = 2mA/V, R_{D1} = R_{D2} = 100kΩ, $r_o(M_1)$ = $r_o(M_2)$ = $r_o(M_3)$ = 100kΩ, and V_{DD} = 1.8V. **(10%)**
   (a) Find the differential gain $A_{v.DM}$. (2.5%)
   (b) Find the common-mode gain $A_{v.CM}$. (2.5%)
   (c) Find the maximum differential input signal range. (2.5%)
   (d) Find the input common mode range. (2.5%)

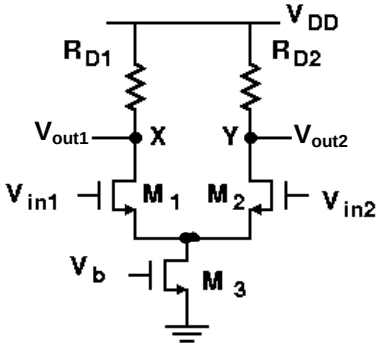

Fig. 9

10. Use the amplifier and bias condition in Fig. 9, assume g_{m1} = 1mA/V and g_{m2} = 2mA/V. **(5%)**
    (a) Find the common mode to differential mode gain $A_{v.CM\text{-}DM}$. (2.5%)
    (b) Assume $A_{v.DM}$ = the value in 11(a), find the *CMRR*. (2.5%)

11. A current mirror as shown in Fig. 11, assume all MOSs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.5V, I_{REF} = 10uA, $(W/L)_2/(W/L)_1$ = 4, and V_{DD} = 1.8V. **(5%)**
    (a) Find the minimum output voltage V_p for correct current mirror operation. (2.5%)
    (b) Find the optimum output voltage V_p for exactly accurate current ratio. (2.5%)

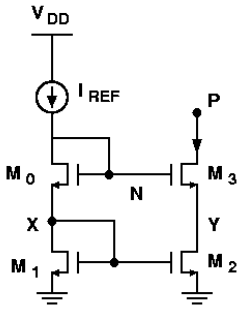

Fig. 11

12. A cascode current mirror as shown in Fig. 12, assume all MOSs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.5V, I_{REF} = 10uA, g_m = 2mA/V, r_o = 100kΩ, $(W/L)_3/(W/L)_1$ = $(W/L)_4/(W/L)_2$ = 4, and V_{DD} = 1.8V. **(5%)**
    (a) Find the minimum V_b and related output voltage V_{out} for correct current mirror operation. (2.5%)
    (b) Find the output resistance R_{out}. (2.5%)

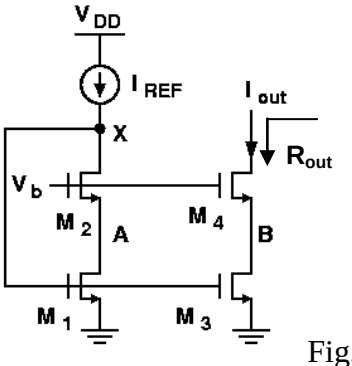

Fig. 12

13. A differential to single-ended amplifier is shown in Fig. 13. Assume all the MOSFETs are biased with $|V_{ov}|$ = 200mV, $|V_{th}|$ = 0.5V, r_o = 100kΩ, and g_m = 2mA/V. The $I_D(M_5)$ = 20uA and V_{DD} = 1.8V. **(10%)**
    (a) Find the minimum input DC bias voltage. (2.5%)
    (b) Find the maximum output swing V_{out}. (2.5%)
    (c) Find the differential gain $V_{out}/(V_{in1}-V_{in2})$. (2.5%)
    (d) Assume $A_{v.CM} = 1/(2g_m r_o)$, find the CMRR. (2.5%)

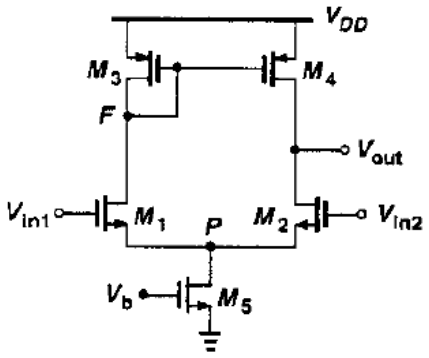

Fig. 13

14. Answer the following questions with TRUE or FALSE: **(15%)**
    (a) Silicide is used to reduce the sheet resistance of metal. (1%)
    (b) The voltage gain of source follower is independent of body effect. (1%)
    (c) Common gate amplifier is commonly used as current buffer due to its low output impedance. (1%)
    (d) Junction capacitance is proportional to depletion width and area. (1%)
    (e) The threshold voltage of nMOS is increased by n+ channel implantation. (1%)
    (f) The depletion width of p/n ratio (W_p/W_n) in diode is correlated to doping concentration (N_A/N_D) as $W_p/W_n = N_A/N_D$. (1%)
    (g) Hot carrier effect is due to the high lateral electrical field of channel. (1%)
    (h) The main free carrier in pMOS is hole and from source/drain. (1%)
    (i) The transconductance g_m of MOSFET is proportional to V_{ov} at known constant biasing current. (1%)
    (j) The channel charge of MOSFET is proportional to W*L and overdrive voltage V_{ov} as well. (1%)
    (k) The output resistance of MOSFET at saturation region is proportional to bias current. (1%)
    (l) The drain current of nMOS at subthreshold region is exponential proportional to applied V_{gs}. (1%)
    (m) For nMOS at triode region, $C_{GS} = C_{GD} = C_{GB}$. (1%)
    (n) The output impedance and gain of common-source amplifier can be increased by cascade structure. (1%)
    (o) The r_o of MOSFET will be decreased at high V_{DS} bias due to the DIBL effect.

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