1. An amplifier with feedback capacitor $C_F$, open-loop gain –A, and equivalent circuit as shown in Fig. 1. Find $Z_1$ and $Z_2$ using Miller effect. **(5%)**

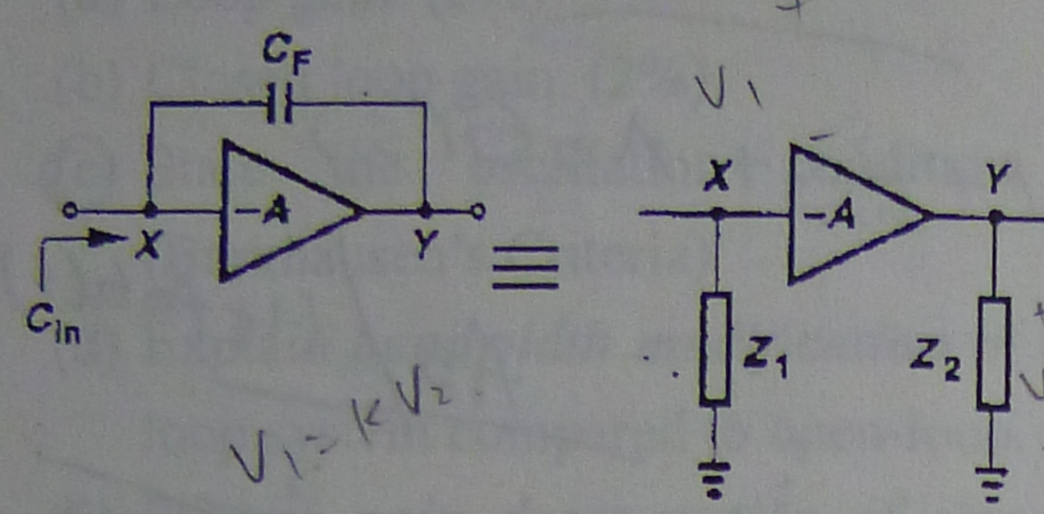


Fig. 1

2. A common source amplifier with C loading is shown in Fig. 2. (assume $r_o = \infty$, $|A_v| >> 1$) **(5%)**
   (a) Use Miller effect to find the equivalent $C_{in}$ at node X and $C_{out}$ at node $V_{out}$. (2.5%)
   (b) Find the corelated input pole $\omega_{in}$ and output pole $\omega_{out}$. (2.5%)

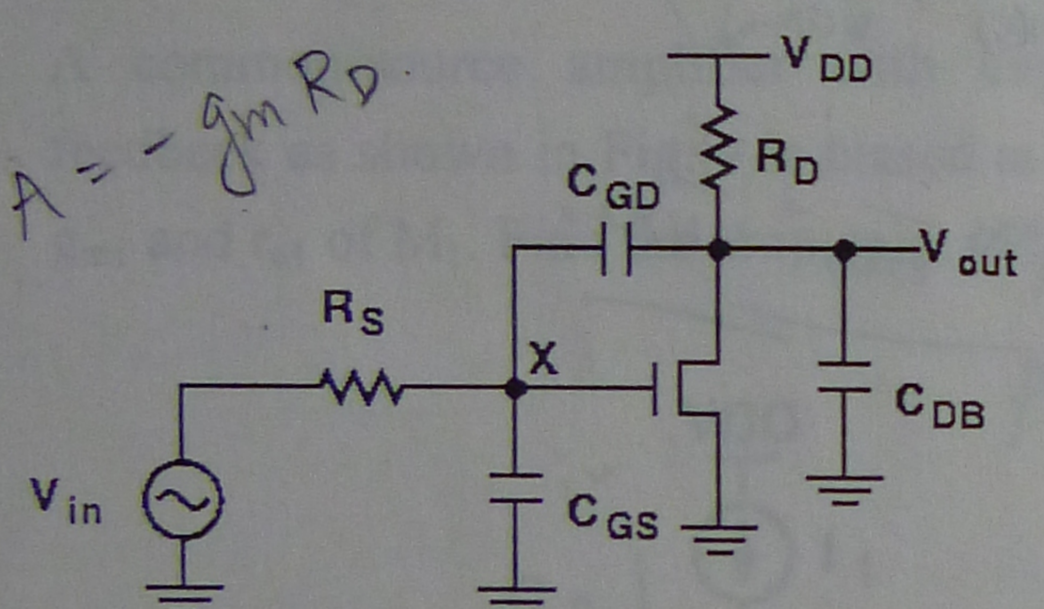


Fig. 2

3. A differential pair with capacitance loading is shown in Fig. 3 **(5%)**
   (a) Find the node of dominant pole and express it in terms of $r_{ox}$ and $C_x$. (2.5%)
   (b) Find the node of second pole and express it in terms of $g_{mx}$, $r_{ox}$ and $C_x$. (2.5%)

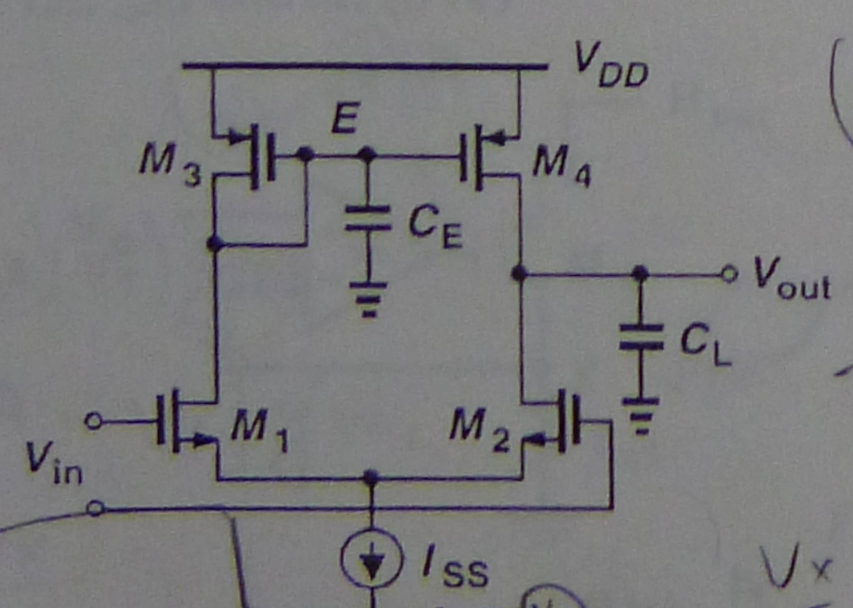


Fig. 3

4. Assume there is a resistor with thermal noise = 4KTR **(5%)**
   (a) Draw **two** equivalent circuits of the resistor with noise voltage source and noise current source, respectively. (2.5%)
   (b) Sketch frequency response of the noise power spectral density (PSD v.s. f). (2.5%)

5. A R-C low-pass filter is shown in Fig. 5. The resistor's thermal noise = 4KTR. Derive the total noise power at output node. **(5%)**

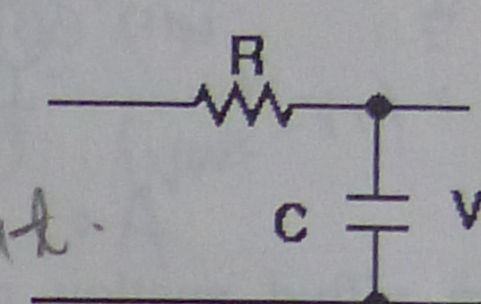


Fig. 5

6. A common source follower is shown in Fig. 6. The thermal noise and flicker noise of $M_1$ are $\overline{I_n^2} = 4kTg_m(\frac{2}{3})$ and $\overline{V_n^2} = \frac{K}{C_{ox}WL}\cdot\frac{1}{f}$. **(10%)**
   (a) Derive the input referred noise $\overline{V_{n,in}^2}$ due to thermal noise. **(5%)**
   (b) Derive the input referred noise $\overline{V_{n,in}^2}$ due to flicker noise. **(5%)**

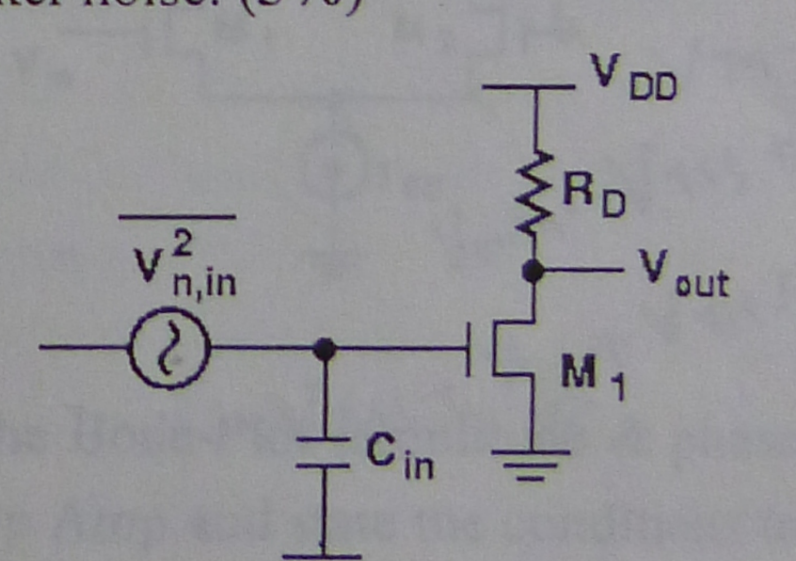


Fig. 6

7. Explain the definitions and purposes of the following terminologies. **(10%)**
   (a) Common mode feedback. (2%)
   (b) Noise power spectrum density. (2%)
   (c) Flicker noise in MOS device. (2%)
   (d) Slewing in an Op Amp. (2%)
   (e) Phase margin. (2%)

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8. A general block diagram of feedback system is shown in Fig. 8. Assume $H(s) = A_0/[1+(s/\omega_0)]$, answer the following definitions of terminology. **(10%)**
   (a) Loop gain. (2%)
   (b) Closed loop gain. (2%)
   (c) State the oscillation condition. (2%) (Barkhausen's Criteria)
   (d) Explain *bandwidth modification* of closed-loop system compared to open-loop. (2%)
   (e) Explain *gain degeneration* of closed-loop system compared to open-loop. (2%)

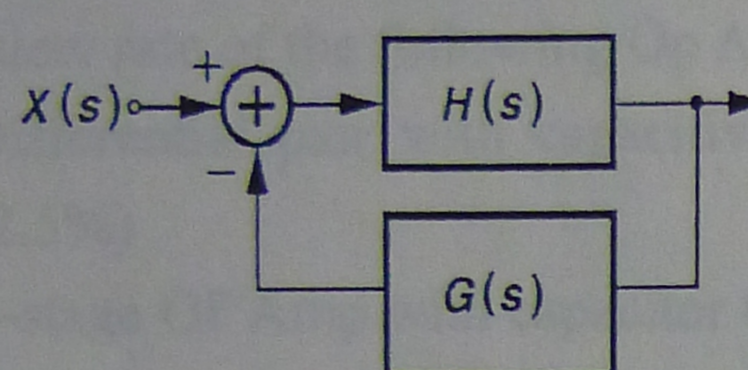


Fig. 8

9. A common-source amplifier with capacitive feedback as shown in Fig. 9 is biased at $I_1$ with $g_{m1}$ and $r_{o1}$ of $M_1$. Find the loop gain. **(5%)**

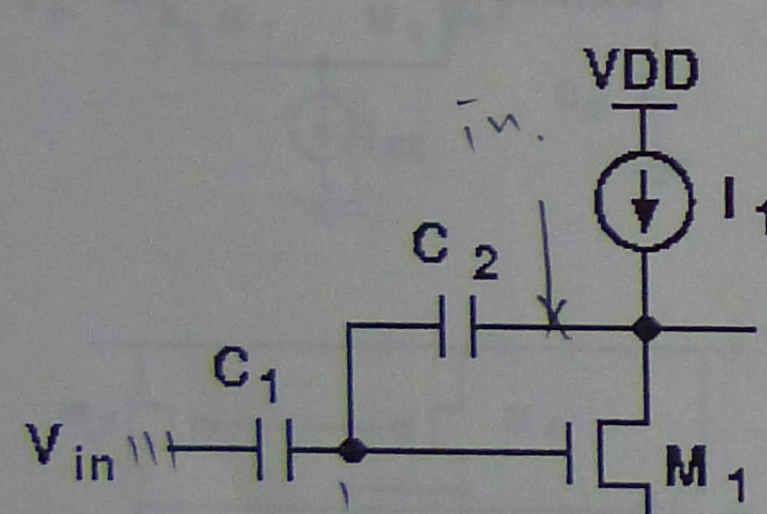


Fig. 9

10. An impedance boosting circuit is as shown in Fig. 10 with $g_{m2}$ and $r_{o2}$ of $M_2$, find the $R_{out}$ in term of $r_{ox}$, $g_{mx}$ and A. **(5%)**

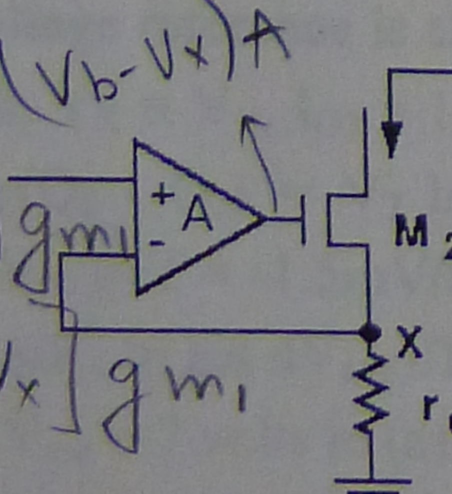


Fig. 10

11. A common-source amplifier with resistive feedback as shown in Fig. 11 is biased with $g_{m1}$ and $r_{o1}$ of $M_1$. **(10%)**
   (a) Find the feedback factor. (2%)
   (b) Find the open-loop gain with loading effect. (4%)
   (c) Find the closed-loop gain $V_{out}/V_{in}$. (4%)

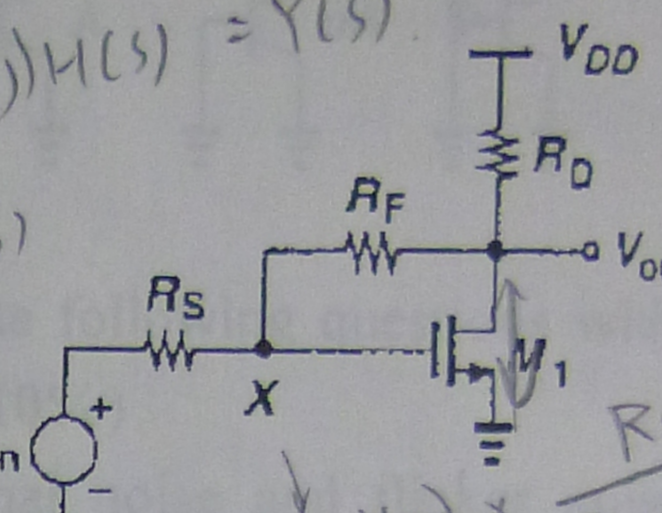


Fig. 11

12. A unity-gain voltage buffer implemented by telescopic Op Amp is shown in Fig. 12. Find the maximum output voltage swing. **(5%)**

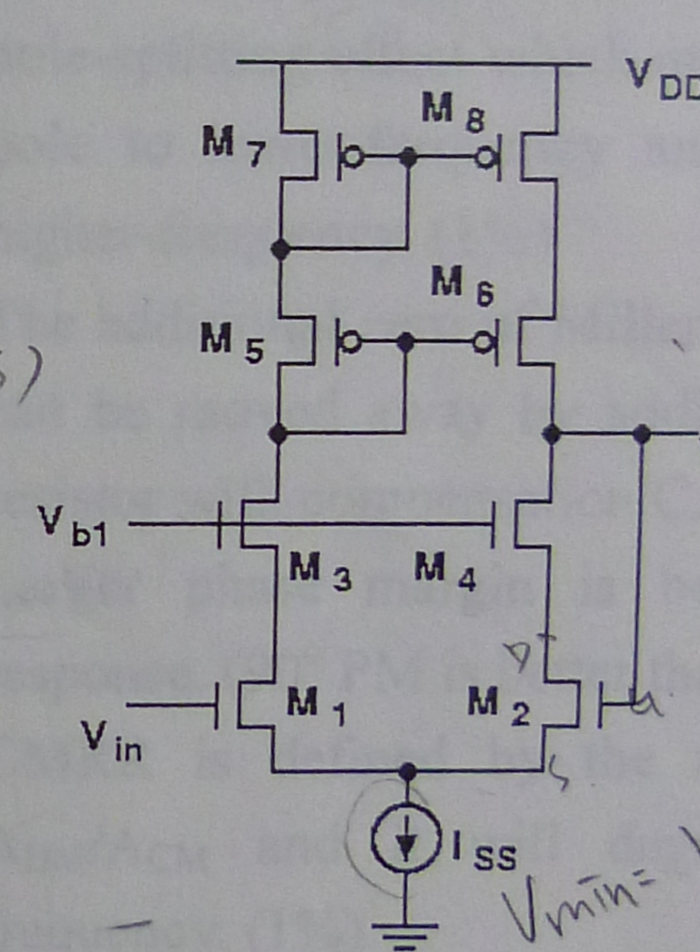


Fig. 12

13. Sketch the Bode-Plot (amplitude & phase) of a 2-pole Op Amp and state the conditions to get a phase margin as 45°. **(5%)**

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14. A fully-differential amplifier is shown in Fig. 14. Add necessary biases and the common-mode feedback circuit on it, sketch the complete circuit. **(5%)**

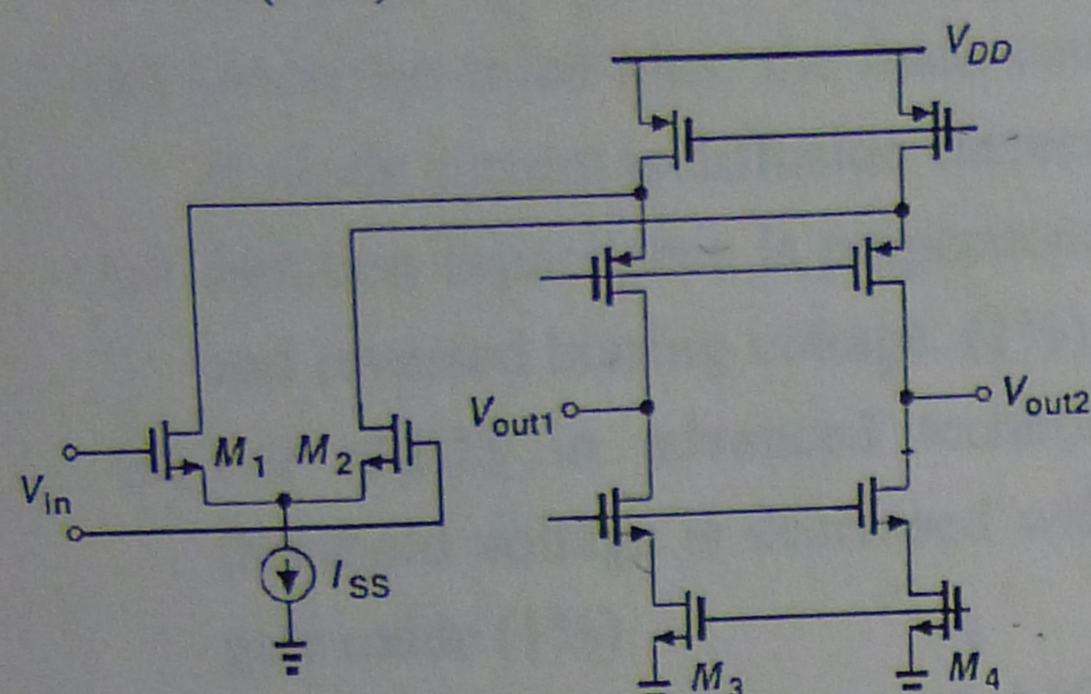


Fig. 14

15. Find slew rate of the following Op Amps. **(5%)**

(a) Differential pair with capacitive feedback. (2.5%)

(b) 2-stage OP Amp with capacitor $C_C$. (2.5%)

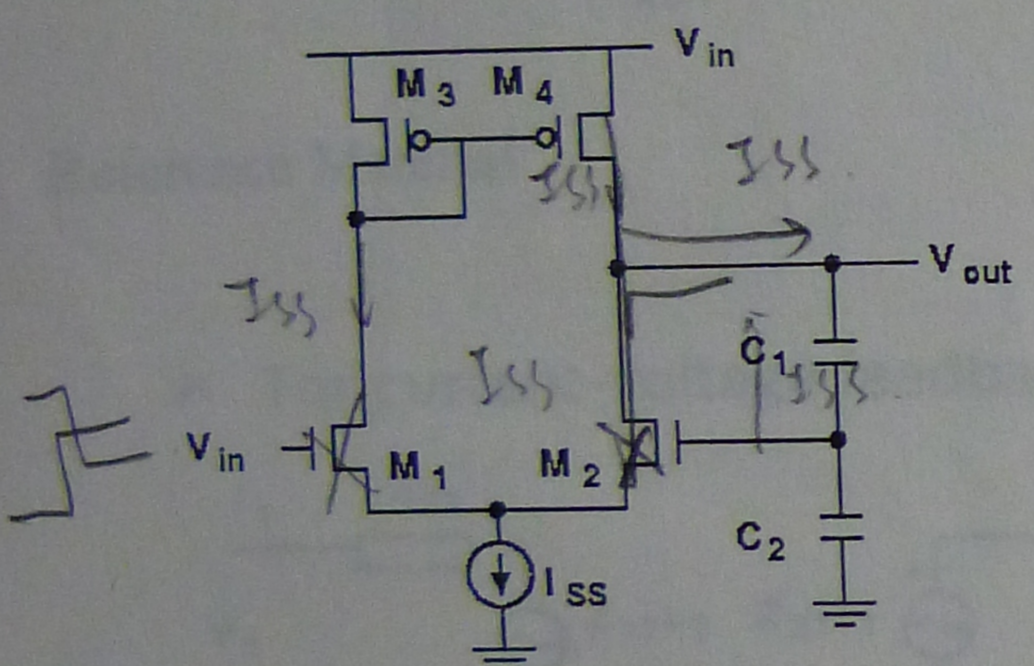


Fig. 15(a)

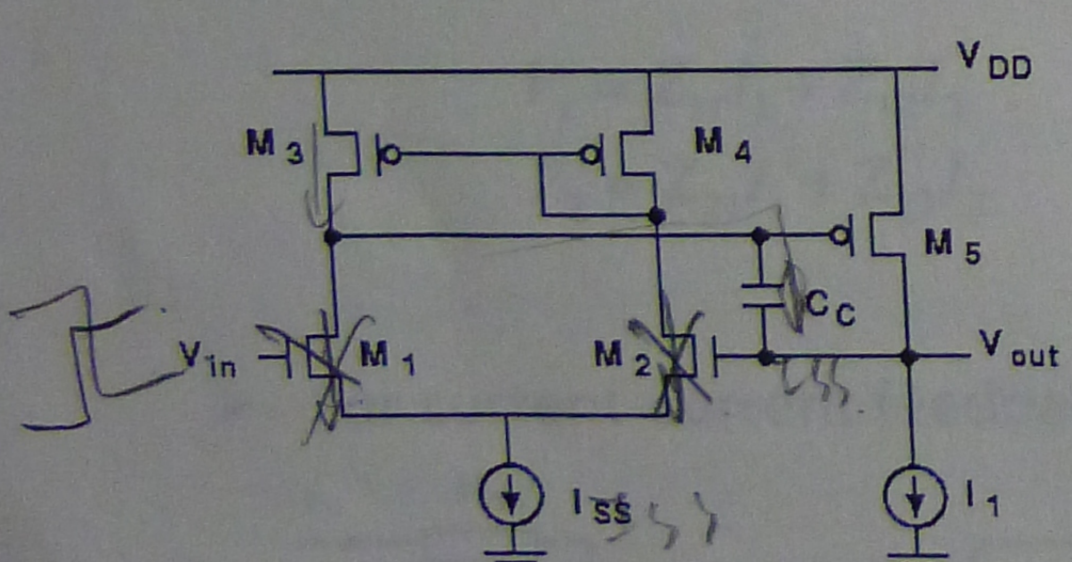


Fig. 15(b)

16. A bandgap voltage reference is shown in Fig. 16. Assume n = 8, $V_X = V_Y$, $I_{D3} = I_{D4} = I_{D5}$, $V_{BE3}$ = 0.75V, $\Delta V_{BE}(Q_1 - Q_2) = V_T \ln(n)$, $dV_T/dT$ = 0.08mV/K, $dV_{BE3}/dT$ = -1.5mV/K. **(5%)**

(a) Design $R_2/R_1$ to get $dV_{out}/dT = 0$. (2.5%)

(b) Find the $V_{out}$ = ? volts in (a). (2.5%)

$V_{BE} = 0.75$

$V_{out} - V_E = const$

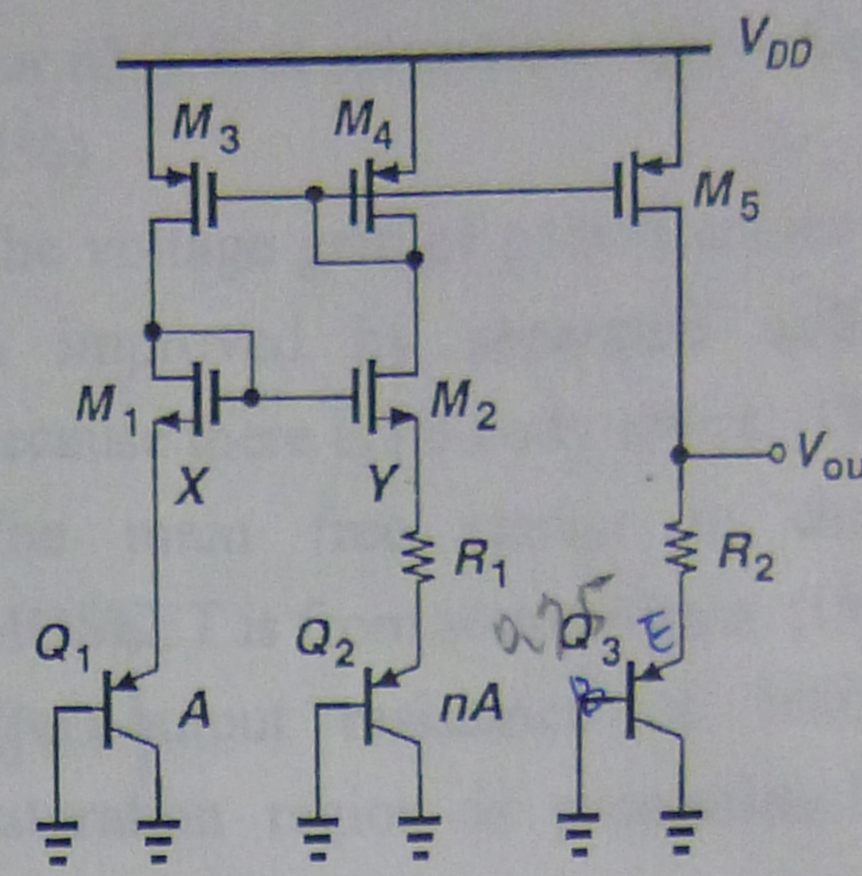


Fig. 16

17. Answer the following questions with TRUE or FALSE: **(10%)**

(a) Thermal noise and flicker noise of MOS device are white noise. (1%)

(b) The Miller compensation of 2-stage OP AMP is to make the dominant pole located at output node. (1%)

(c) Miller compensation will result in a pole-splitting effect which moves dominant pole to lower-frequency and 2nd pole to higher-frequency. (1%)

(d) The additional zero of Miller compensation can be moved away by adding a shunting resistor with compensation C. (1%)

(e) Larger phase margin is better for step response. (90° PM is better than 60°). (1%)

(f) CMRR is defined by the ratio between $A_{DM}/A_{CM}$ and it will degrade at high frequency. (1%)

(g) Usually the noise types in a circuit are from device and environmental noise. (1%)

(h) Most of the noise sources in circuits are correlated. (1%)

(i) The linear response happened only when Op Amp enter the slewing condition. (1%)

(j) Port impedance in feedback system will be decreased by shunt connection and increased by series connection. (1%)

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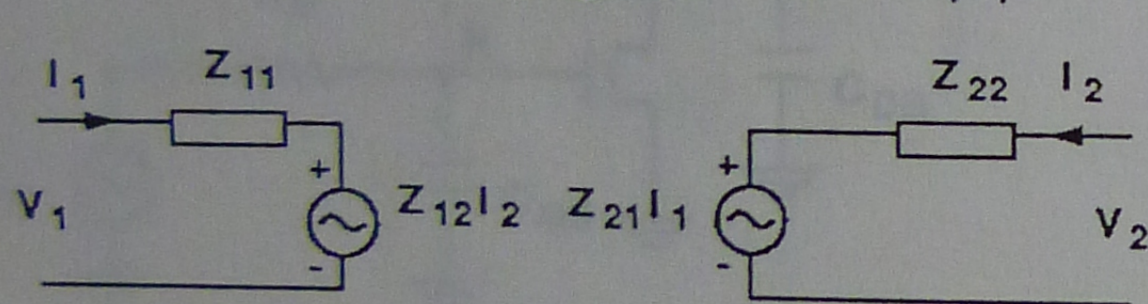
18. Answer the following questions with TRUE or FALSE: **(10%)**
    - (a) Silicide is used to decrease the sheet resistance of layers in IC process. (1%)
    - (b) Under reversed bias, the main contribution of diode current is diffusion current. (1%)
    - (c) Junction capacitance is proportional to area and reversed biasing voltage. (1%)
    - (d) For nMOS in advanced technology, the threshold voltage is decreased with thinner gate oxide (1%)
    - (e) The transconductance $g_m$ of MOSFET is proportional to *bias current* $I_D$ at fixed W/L dimension. (1%)
    - (f) For nMOS at saturation region, $C_{GS} > C_{GD}$. (1%)
    - (g) The voltage gain of pMOS source follower is improved by separated well design, because there is no body effect. (1%)
    - (h) The main free carrier in channel of MOSFET is from source/drain. (1%)
    - (i) The output resistance of MOSFET at saturation region is proportional to bias current $I_D$. (1%)
    - (j) PTAT current source is usually implemented by the positive temperature coefficient of $V_{BE}$. (1%)

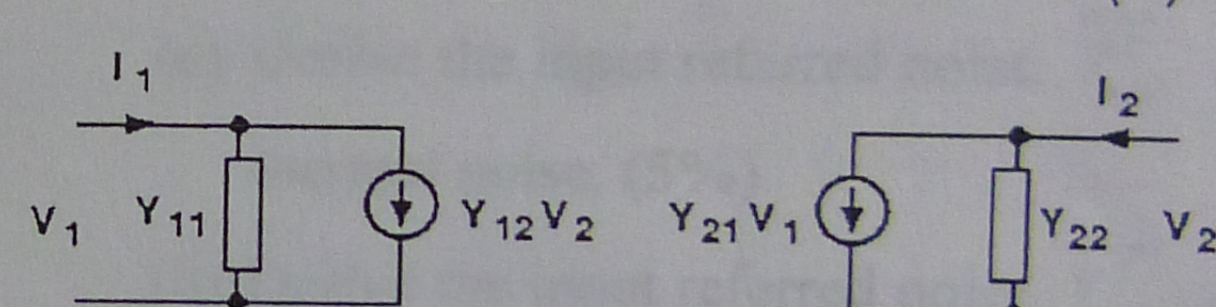
Reference Material

➢ For current-voltage feedback (Z)



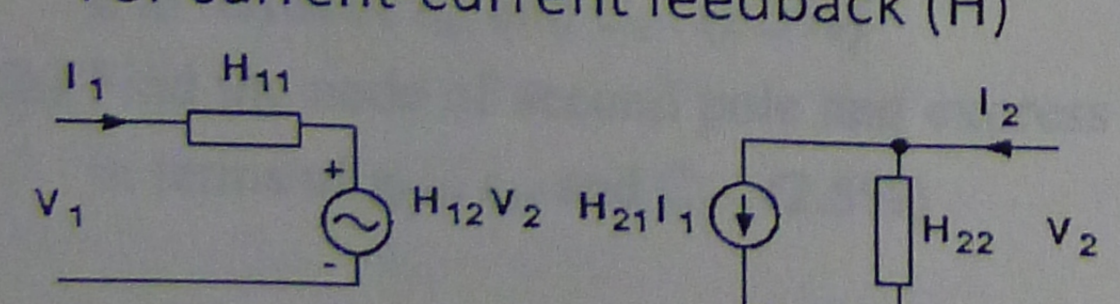

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

➢ For voltage-current feedback (Y)



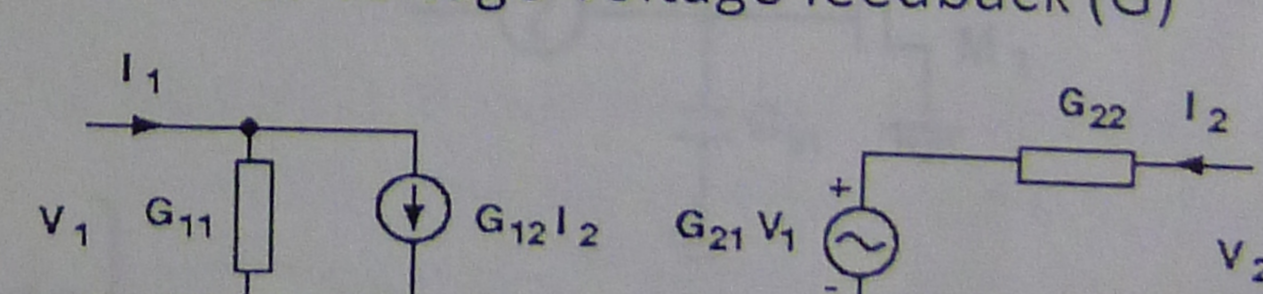

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

➢ For current-current feedback (H)

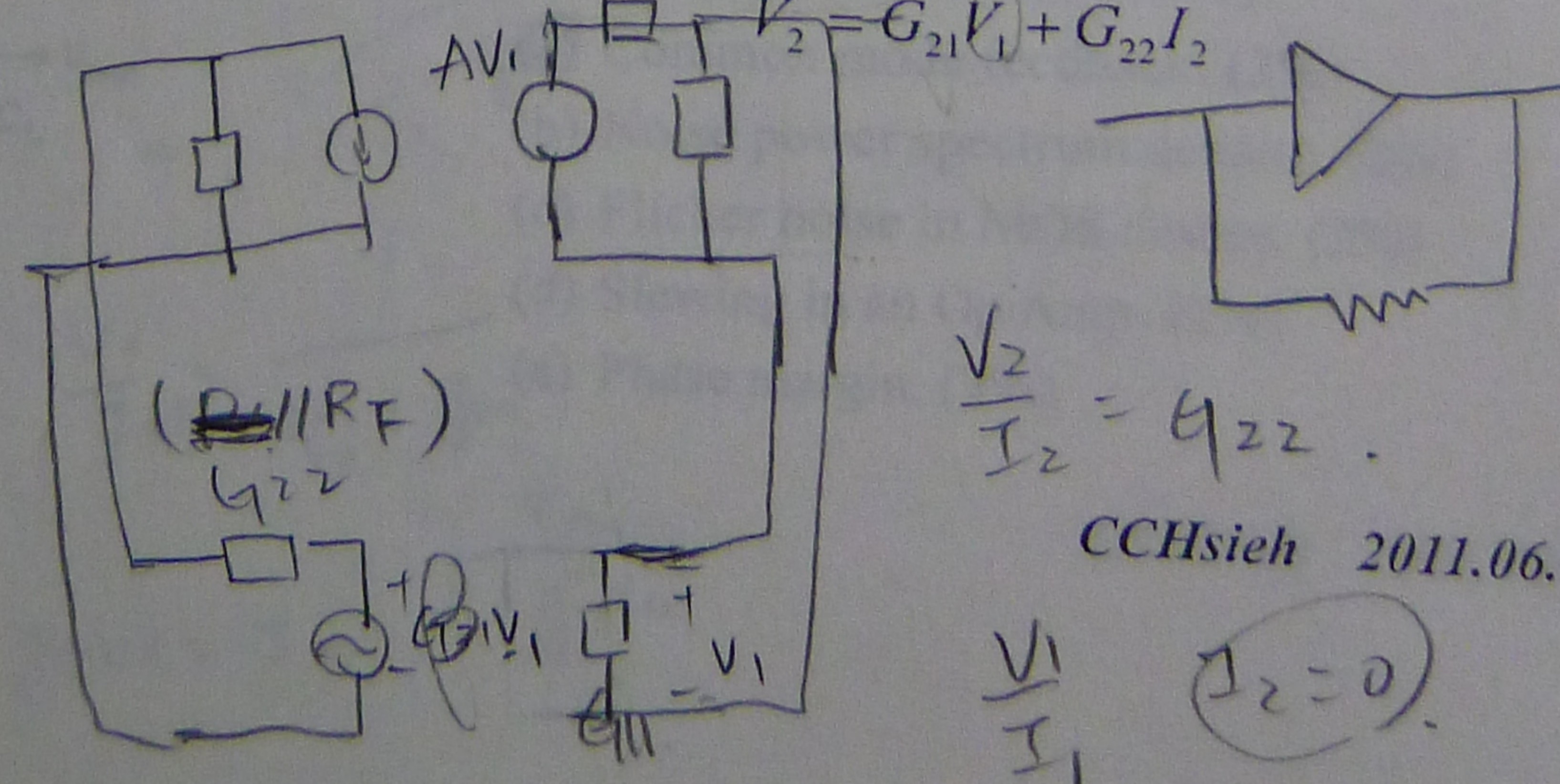



$$V_1 = H_{11}I_1 + H_{12}V_2$$
$$I_2 = H_{21}I_1 + H_{22}V_2$$

➢ For voltage-voltage feedback (G)




$$I_1 = G_{11}V_1 + G_{12}I_2$$
$$V_2 = G_{21}V_1 + G_{22}I_2$$



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