CHAPTER 9

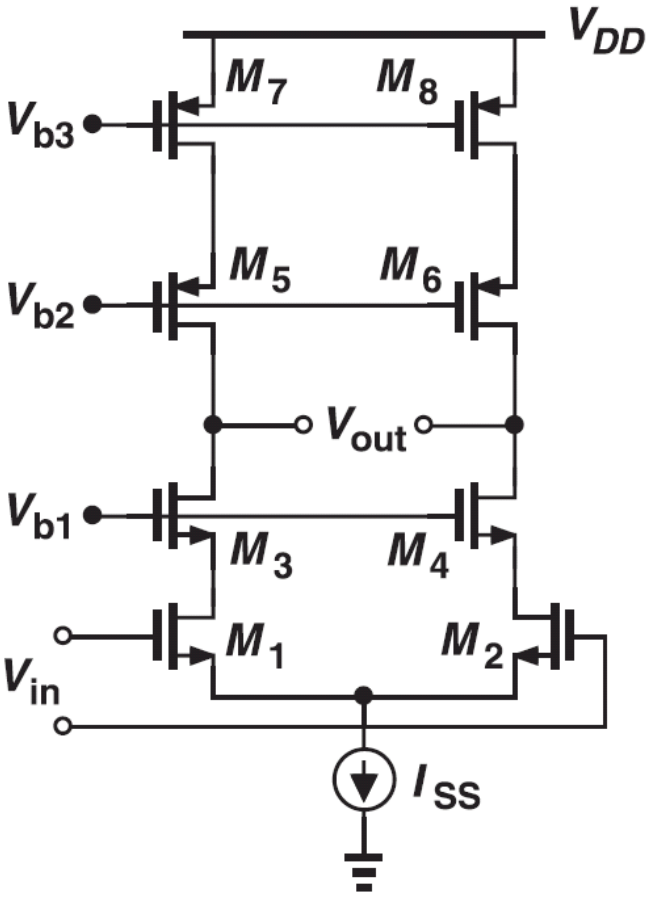
Operational Amplifiers

Outline

1. **General Consideration**
2. One-Stage Op Amps / Two-Stage Op Amps
3. Gain Boosting
4. Common-Mode Feedback
5. Input Range / Slew Rate
6. Power Supply Rejection / Noise in Op Amps

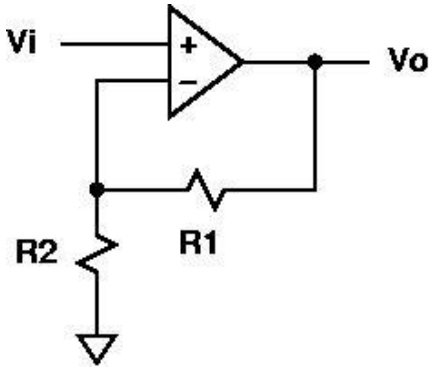
General Consideration

- Operational amplifiers (OP amps) are in general part of many analog and mixed-signal systems – ranging from DC bias generation to high speed amplification or filtering.
- Ideal characteristics
  - Very high voltage gain (several hundred thousand).
    - A high open-loop gain is necessary to suppress nonlinearity.
  - High input impedance.
  - Low output impedance.
  - Other considerations
    - Speed.
    - Output voltage swings.
    - Power dissipation.



Closed-Loop Application

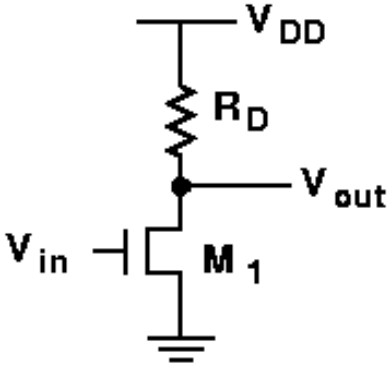
- The open loop gain of an op amp determines the precision of the feedback system employing the op amp.



$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1+\frac{R_2}{R_1+R_2}A_1} = \frac{R_1+R_2}{R_2}\frac{A_1}{\frac{R_1+R_2}{R_2}+A_1}$$

to get $(1+R_1/R_2)=10$ *If* $A_1 >> 10$

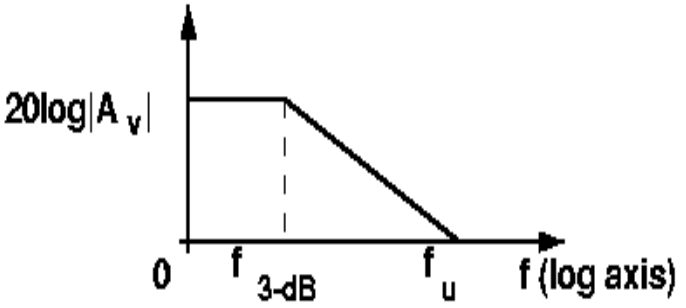
$$\frac{V_{out}}{V_{in}} \approx \left(1+\frac{R_1}{R_2}\right)\left(1-\frac{R_1+R_2}{R_2}\frac{1}{A_1}\right)$$



- Relative gain error is represented as $\frac{R_1+R_2}{R_2A_1} = \frac{1+R_1/R_2}{A_1}$
- To achieve a gain error less than 1%, we must have $A_1 > 1000$.
- With open-loop implementation using common source gain stage.
  - It is extremely difficult to guarantee an error less than 1%.
  - The variations in the $\mu_{n,p}$ and t_{ox} of the transistor and the value of the resistor typically yield an error greater than 20%.

OP Properties

- The small signal bandwidth is usually defined as the "unity-gain" frequency, f_u .



- Large signal bandwidth
  - OP amps must operate with large transient signals.
  - Nonlinear phenomena make it difficult to characterize the speed by merely small-signal properties such as the open-loop response.

- Output swings
  - Most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitudes.
  - The need for large output swings has made fully differential op amps quite popular – roughly doubling the swing.
  - The maximum voltage swing trades with device size and bias currents and hence speed.

OP Properties

- Linearity
  - Open loop op amps suffer from substantial nonlinearity.
  - The issue of nonlinearity is tackled by two approaches
    - Using fully differential implementations to suppress even-order harmonics.
    - Allowing sufficient open-loop gain such that the closed-loop feedback system achieves adequate linearity.
- Noise and offset
  - The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality.
- Supply rejection
  - Fully differential topologies are preferred.

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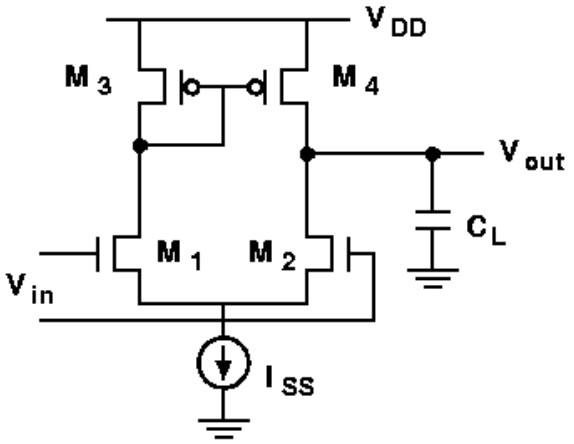
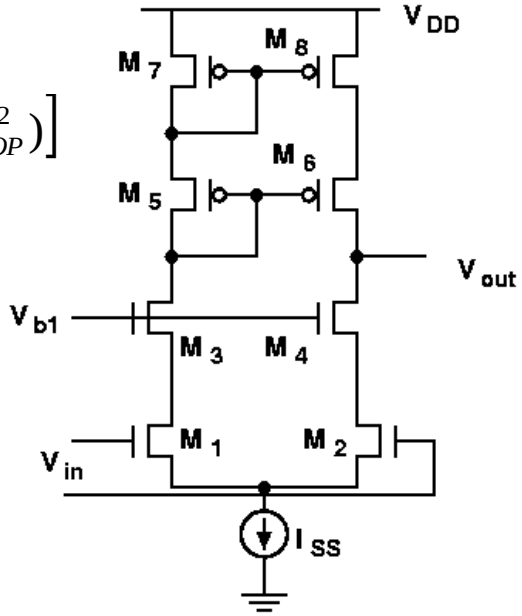
One Stage Op Amps

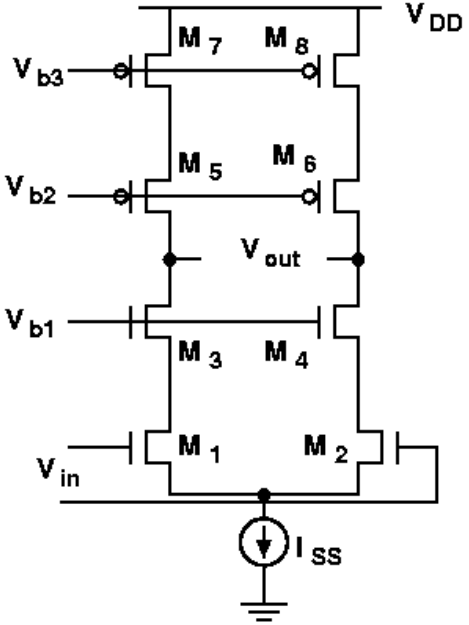
- The small-signal, low frequency gain is $g_{mN}(r_{ON} \parallel r_{OP})$
- The bandwidth is usually determined by the load capacitance C_L.
- The circuit suffers from noise contributions of M_1-M_4 , 2 input devices + 2 load devices.

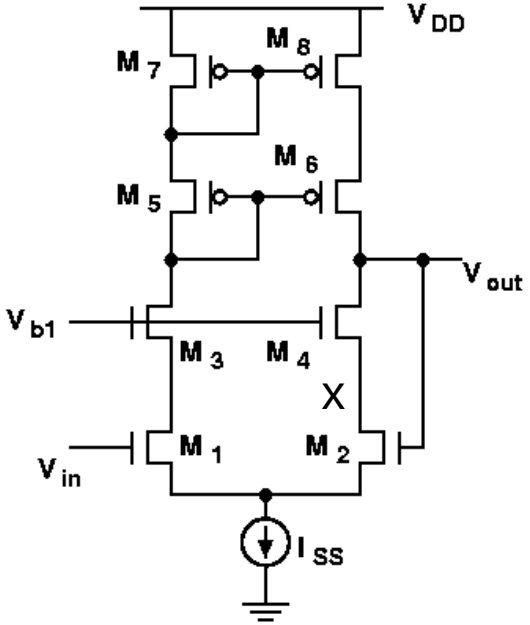


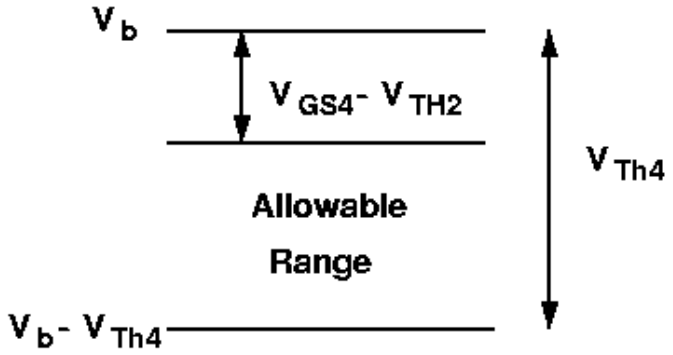
- Differential cascode op amps
- The small-signal, low frequency gain is $g_{mN}\left[(g_{mN}r_{ON}^2 \parallel g_{mP}r_{OP}^2)\right]$
- High gain at the cost of output swing and additional poles.
- These configurations are also called "telescopic" cascode op amps.



Telescopic Op Amplifiers







- The output swing = $2[V_{DD}-(V_{OD1}+V_{OD3}+V_{CSS}+|V_{OD5}|+|V_{OD7}|)]$, V_{ODj} = V_{ov} of M_j.
- Difficulty in shorting their inputs and outputs, e.g. , to be as a unity-gain buffer.
- For $V_X = V_{b1} - V_{GS4}$ $V_{out} \le V_X + V_{TH2}$ $V_{out} \ge V_{b1} - V_{TH4}$

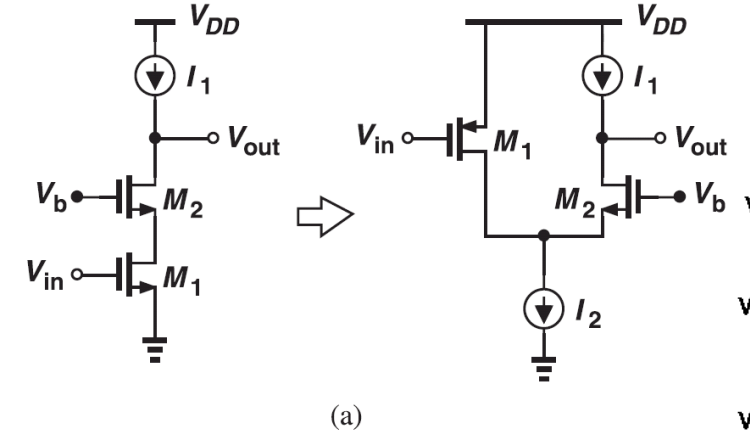
$$V_b - V_{TH4} \le V_{out} \le V_b - V_{GS4} + V_{TH2}$$

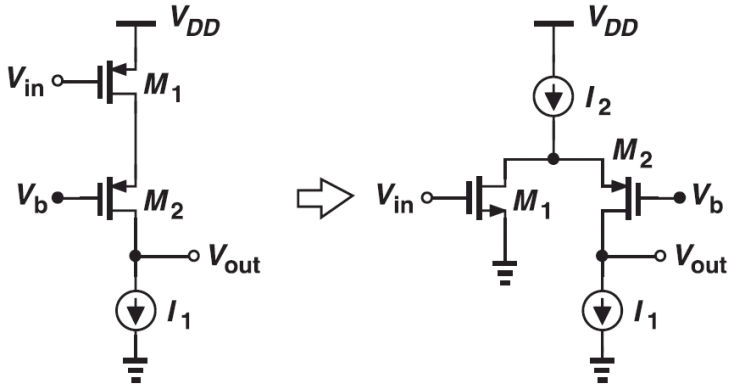
$$V_{max} - V_{min} = V_{TH4} - (V_{GS4} - V_{TH2}) = V_{TH2} - V_{OV4} \le V_{TH2}$$

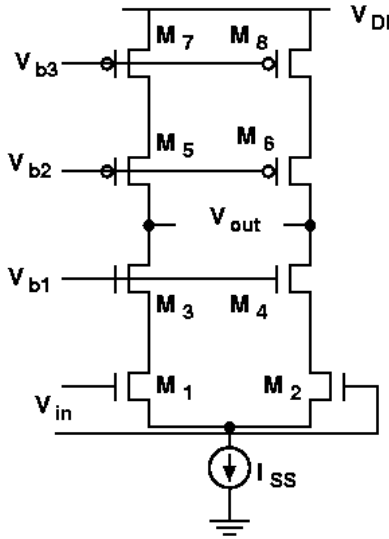
- Maximize the output swing by minimizing the V_{ov} of M_4 but always less than V_{TH2}.

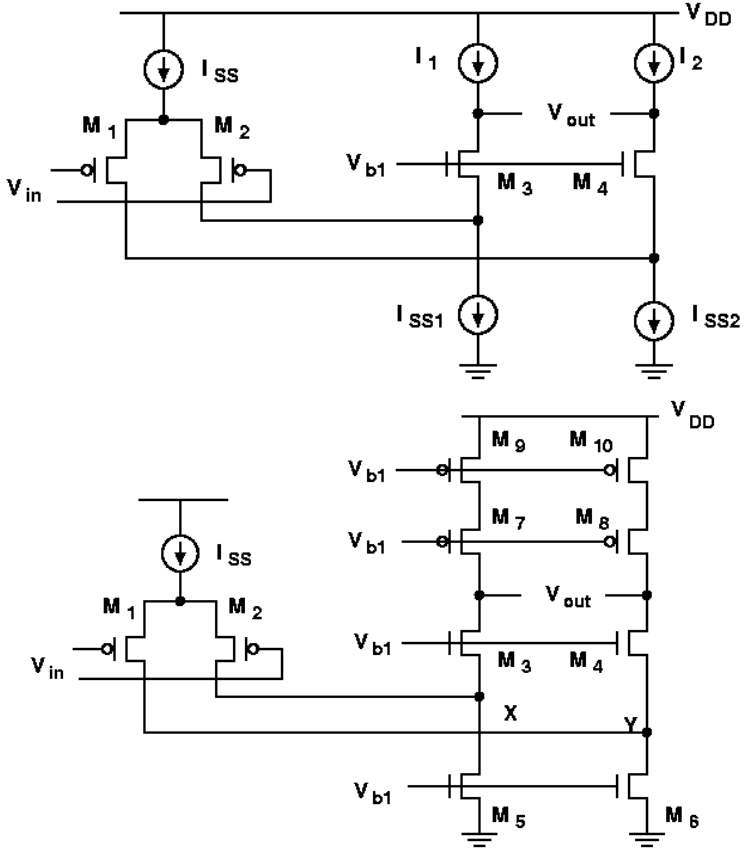
Folded Cascode Circuits

- To alleviate the drawbacks of telescopic cascode op amps. $A_v = g_{m1} R_{out} V_{in}$









$$I_{SS1} = I_{SS}/2 + I_{D3}$$

- The maximum output voltage swing (each side)

$$V_{OD3} + V_{OD5} < V_{swing} < V_{DD} - (|V_{OD7}| + |V_{OD9}|) \qquad V_{p-p} = V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|)$$

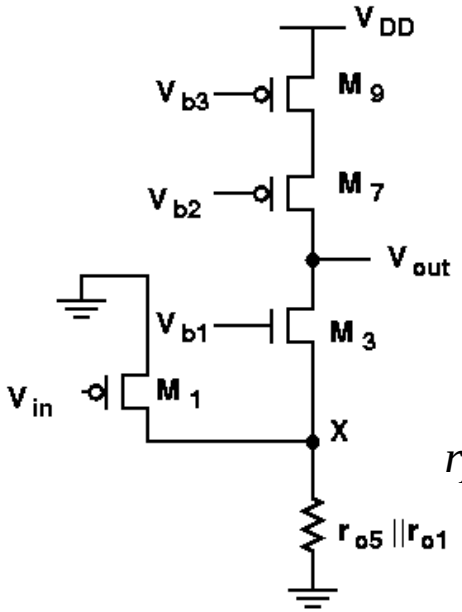
Folded Cascode Op Amp - Half Circuit

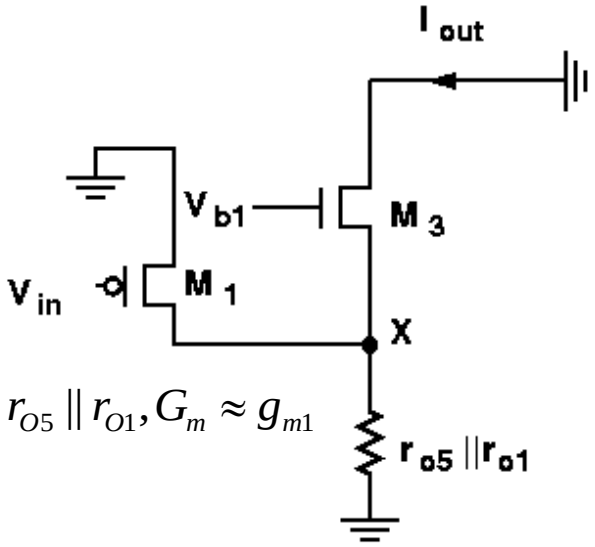
- Conversion gain –lower than that of telescopic OP
  - PMOS input differential pair exhibits a lower transconductance.
  - Lower resistance at node X.
  - The conversion gain in general lower than that of telescopic architecture.

$$R_{OP} \approx (g_{m7} + g_{mb7}) r_{O7} r_{O9}, \quad R_{ON} \approx (g_{m3} + g_{mb3}) r_{O3} (r_{O1} \| r_{O5})$$

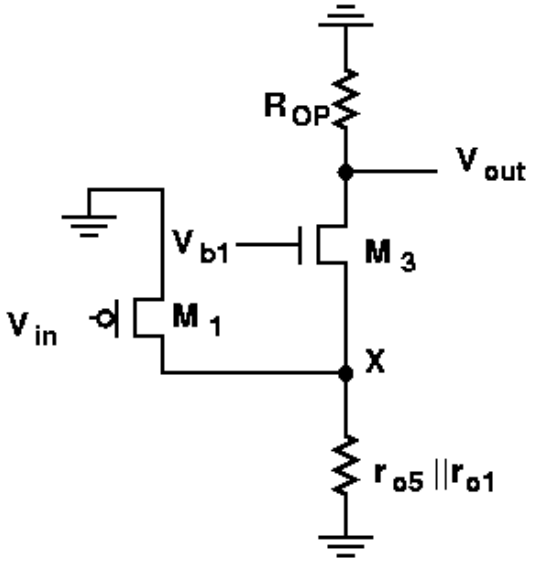
$$R_{out} = R_{OP} \| R_{ON}, \quad |A_v| = G_m R_{out}$$

$$|A_v| \approx g_{m1} \{ (g_{m3} + g_{mb3}) r_{O3} (r_{O1} \| r_{O5}) \| (g_{m7} + g_{mb7}) r_{O7} r_{O9} \}$$



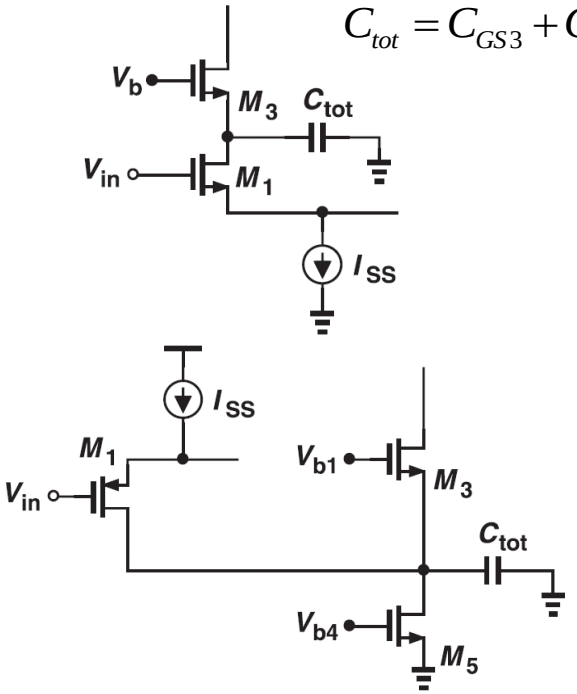


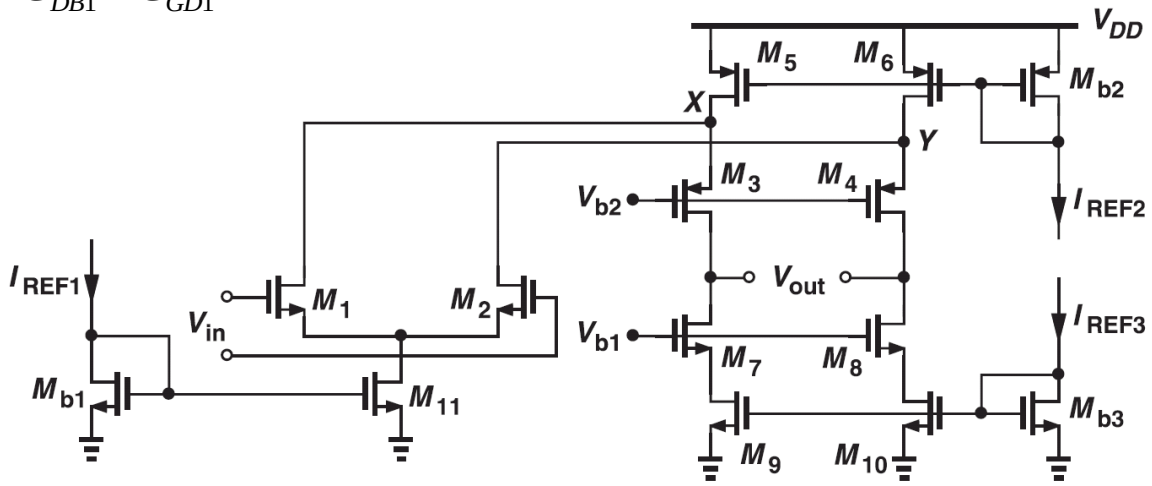
$$r_X << r_{O5} \| r_{O1}, G_m \approx g_{m1}$$



N-input Folded Cascode Op Amps

$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1}$$





$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1} + C_{GD5} + C_{DB5}$$

$$R_{tot} = 1/g'_{m3} \parallel r_{O5} \parallel r_{O1} \approx 1/g'_{m3}$$

- Non-dominant pole frequency is determined by $C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1} + C_{GD5} + C_{DB5}$
- A folded-cascode op amp may use NMOS input and PMOS cascode transistors
  - Higher gain.
  - At the cost of lowering the pole at the folding point.
  - M3 suffers from a lower g_m and M5 contributes substantial capacitance.

Comparison to Telescopic

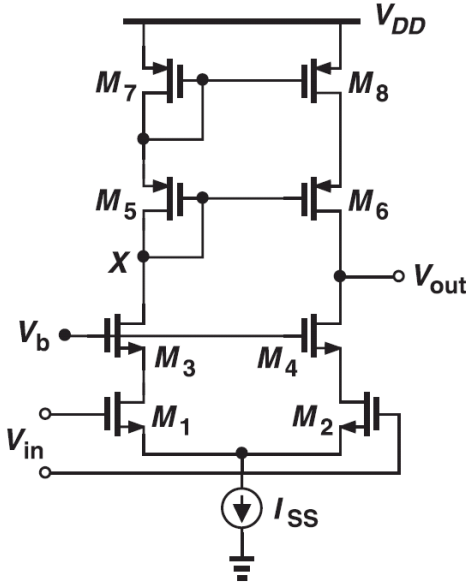
- Summary for “folded cascode” OP in comparison to “telescopic” OP
  - Advantage : wider swing, the input and output can be shorted together, the choice of the input common-mode level is easier.
  - Disadvantage : Higher power, lower voltage gain, lower pole frequency.

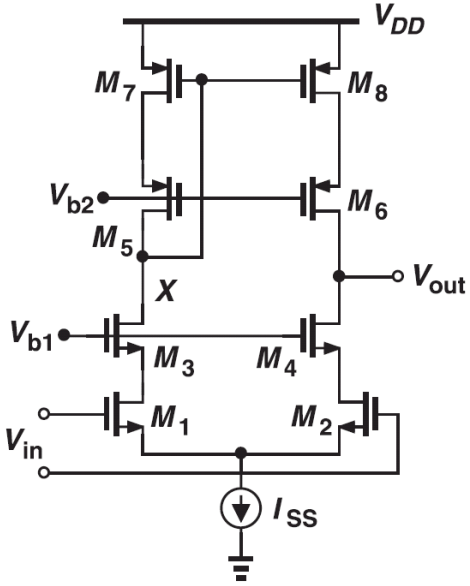
Cascode OP Amps / Single-Ended

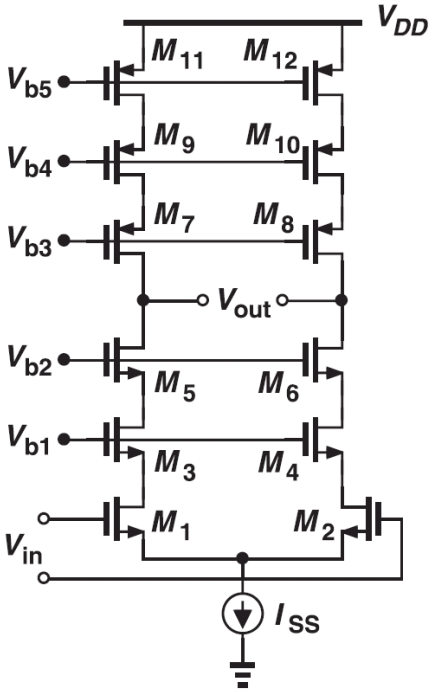
- Cascode OP using wide swing current mirror.
- For single-ended OP
  - It provides only half the output voltage swing.
  - It contains a mirror pole at node X, thus limiting the speed of feedback systems employing such an amplifier.
- Triple Cascode

$$A_V \approx \frac{1}{2}(g_m r_O)^3,$$

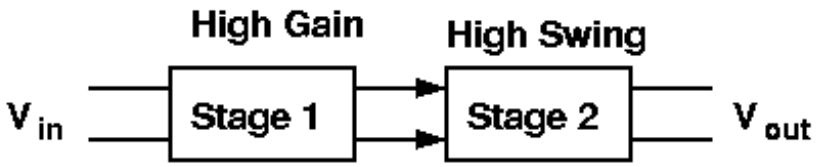
$$V_X = V_{DD} - |V_{GS5}| - |V_{GS7}|, \quad V_{out(\max)} = V_{DD} - |V_{GS5}| - |V_{GS7}| + |V_{TH6}|$$

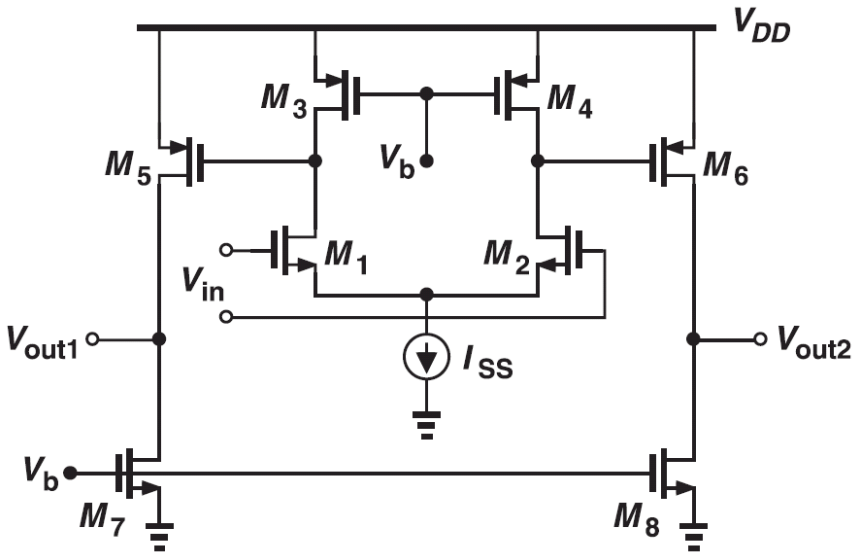






Two-Stage OP Amps

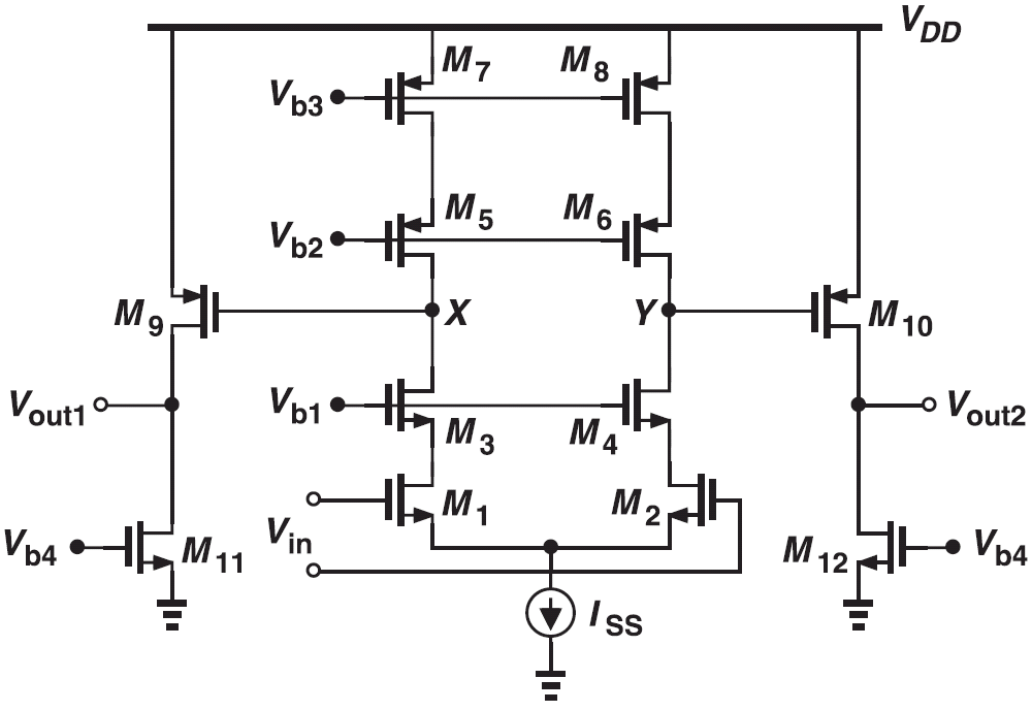




- A two-stage configuration isolates the gain and swing requirement.
- The first stage provides a high gain. $A_{V1} \approx g_{m1,2}\left(r_{O1,2} \parallel r_{O3,4}\right)$
- The second stage provides large swing. $A_{V2} \approx g_{m5,6}\left(r_{O5,6} \parallel r_{O7,8}\right)$
- The overall gain is comparable to that of a cascode op amp, but the swing is equal to $V_{DD} - |V_{OD5,6}| - V_{OD7,8}$

Two-Stage OP Amps + Cascode

- Two stage op amp employing cascode



$$A_V \approx \left\{ g_{m1,2} \left[\left(g_{m3,4} + g_{mb3,4} \right) r_{O3,4} r_{O1,2} \right] \| \left[\left(g_{m5,6} + g_{mb5,6} \right) r_{O5,6} r_{O7,8} \right] \right\}$$
$$\times \left[g_{m9,10} \left(r_{O9,10} \| r_{O11,12} \right) \right]$$

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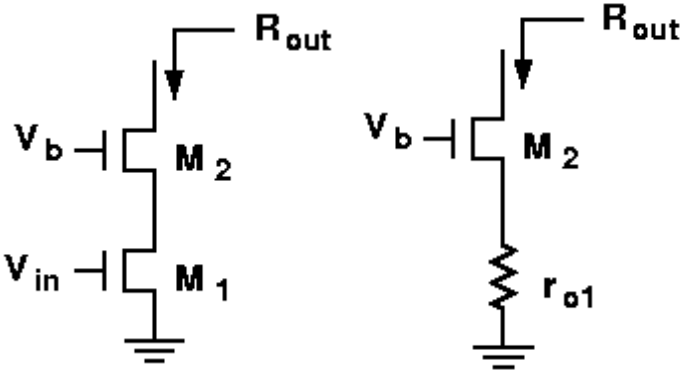
Gain Boosting

- Increasing the output impedance by feedback.

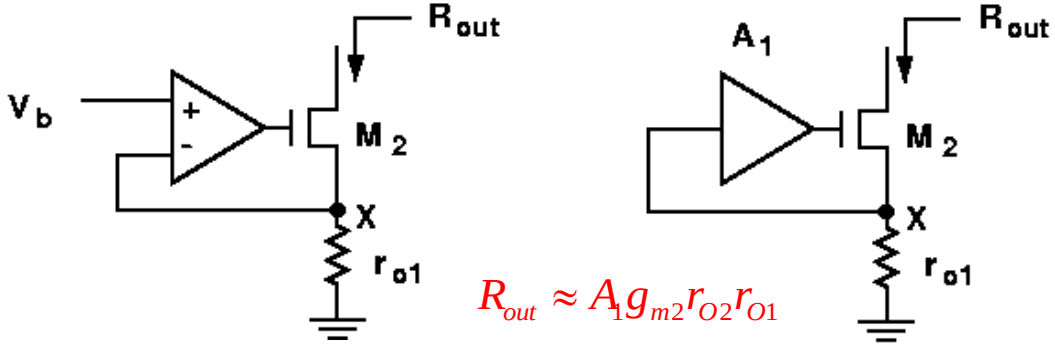
$$R_{out} = g_{m2} r_{O2} r_{O1}$$

- The small signal voltage produced across r_{O1} is proportional to the output current.
- $V_{gs2} = V_b - V_{ro1}$.
- M_2 in current voltage feedback.

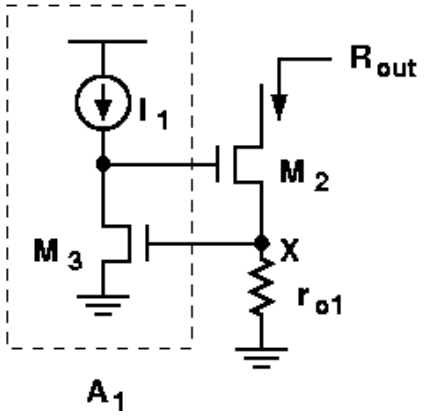


$$R_{out} = g_{m2} r_{O2} r_{O1}$$

- Gain boosting in cascode stage (Regulated Cascode)
  - Forces V_x to be equal to V_b, such that voltage variations at the drain of M_2 affect V_x to a lesser extent.
  - For small signal operation, V_b is set to zero.



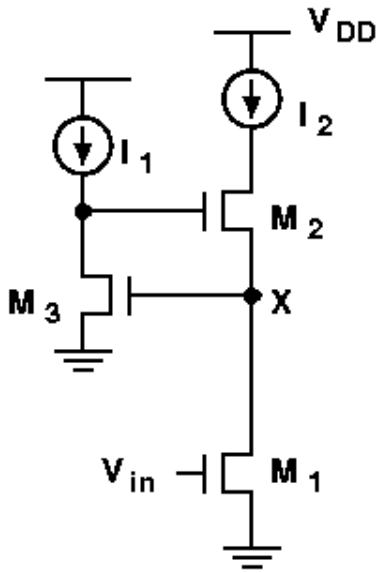
$$R_{out} \approx A_1 g_{m2} r_{O2} r_{O1}$$



Gain Boosting in Cascode Stage

- The overall voltage gain is equal to

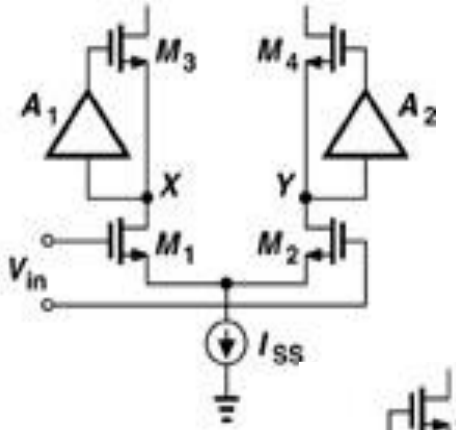
$$|A_v| \approx g_{m1}(g_{m2}r_{O2}r_{O1})(g_{m3}r_{O3})$$

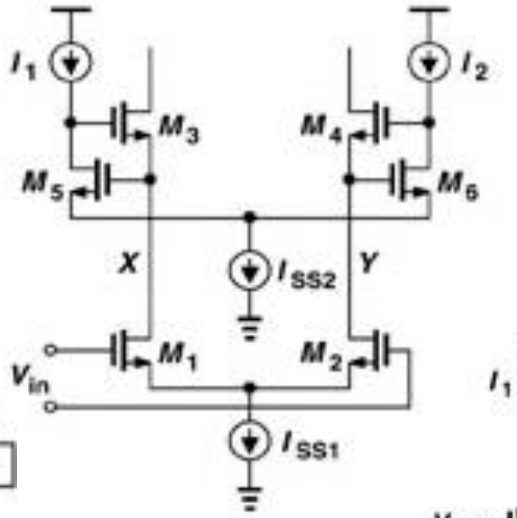


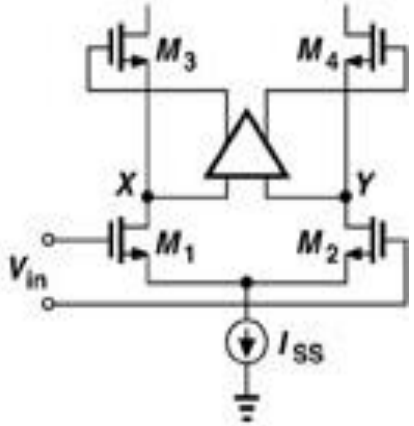
- The gain is similar to that of a triple cascode.
- Consider the output swing
  - $V_x = V_{GS3}$ $V_{out(min)} = V_{OD2} + V_{GS3}$
- For simple cascode, $V_{out(min)} = V_{OD2} + V_{OD1}$
- The auxiliary amplifier limits the output swing.

Gain Boosting in Cascode Stage

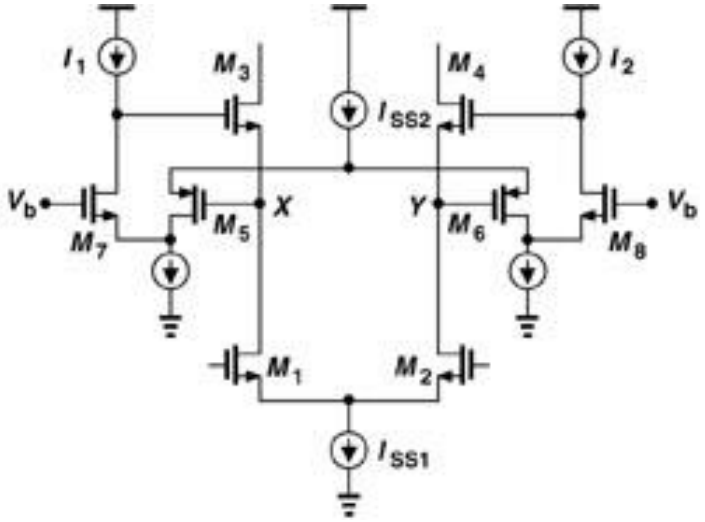
- The minimum level at the drain of M3 is equal to $V_{out(min)} = V_{OD3} + V_{GS5} + V_{ISS2}$
- If nodes X and Y are sensed by a PMOS pair, the minimum value of V_X and V_Y is not dictated by the gain-boosting amplifier.
  - In this case, $V_{out(min)} = V_{OD1,2} + V_{OD3,4} + V_{ISS1}$



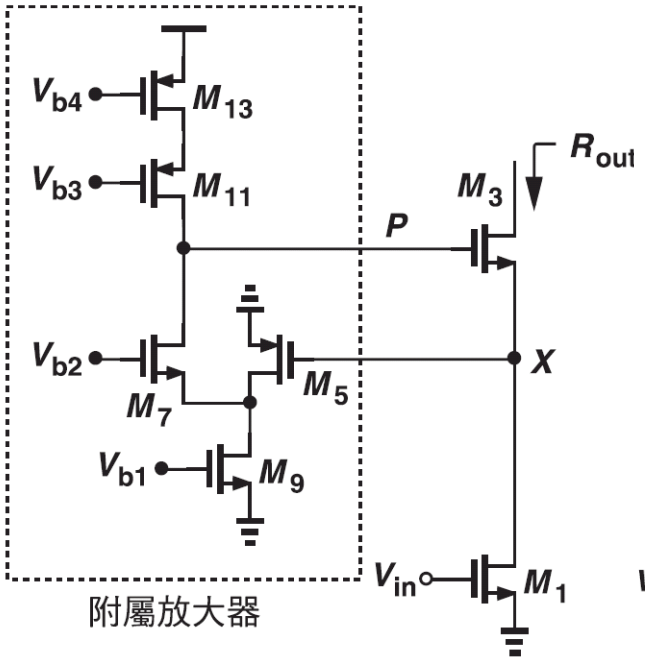


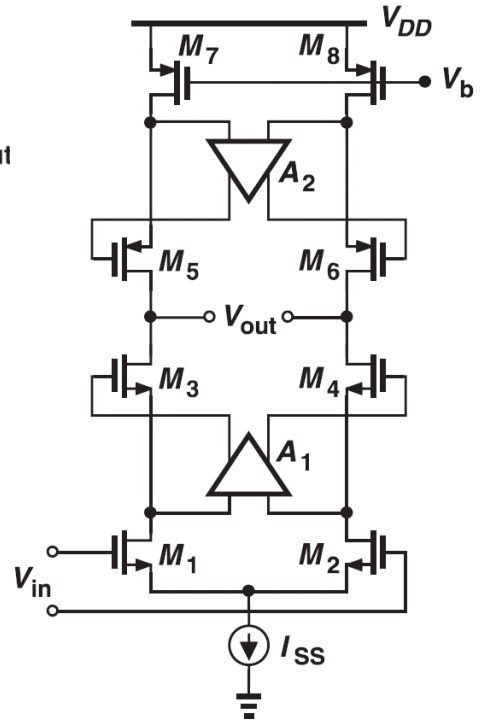


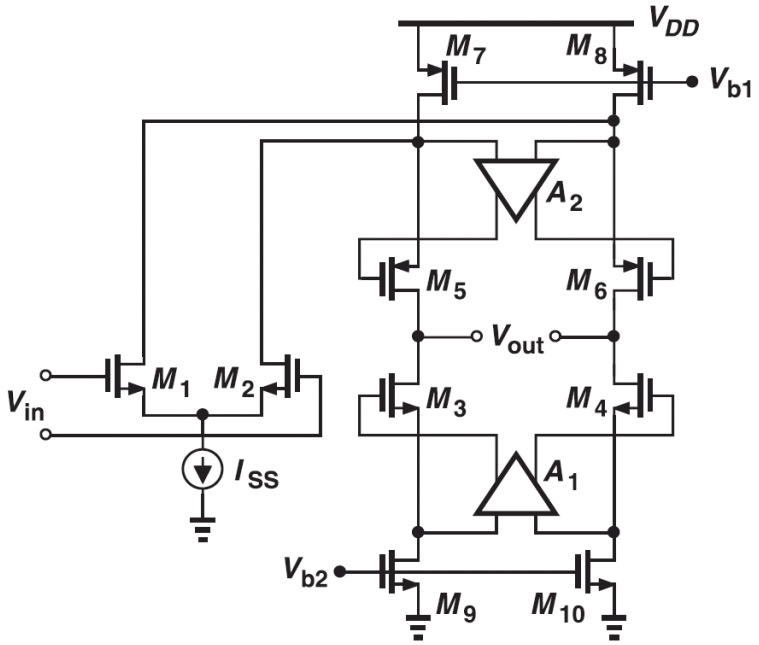
Folded-cascode as aux amplifier



Gain Boosting / Signal Path & Load







- For maximum output swings, A_2 must employ an NMOS input differential pair.
- A_1 can employ a PMOS input differential pair.
- The gain boosting amplifier introduces its own poles.
- In a g-b op amp, most of the signal directly flows through the cascode devices to the output. Only a small "error" component is processed by the g-b amplifier.

Performance Comparison

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

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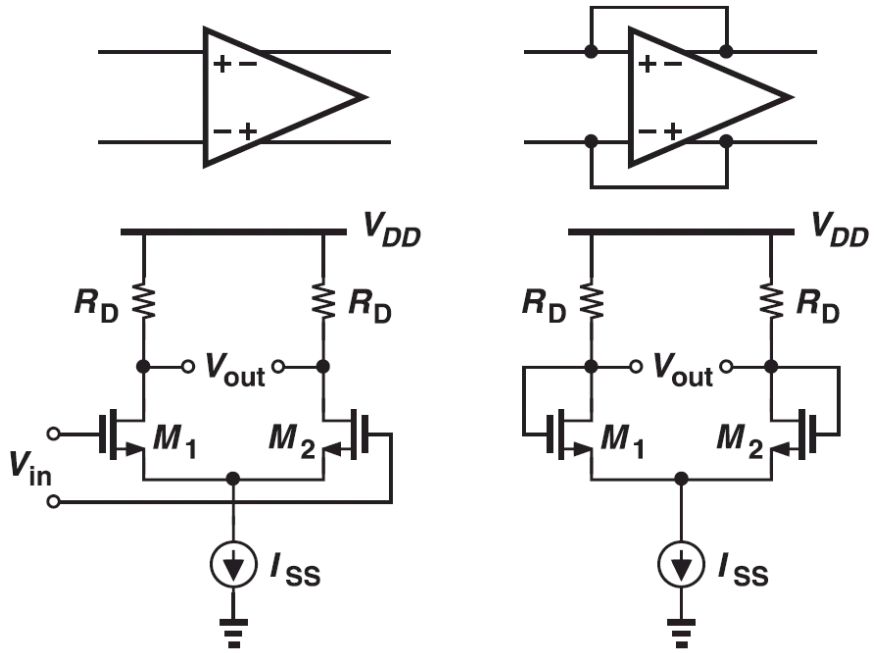
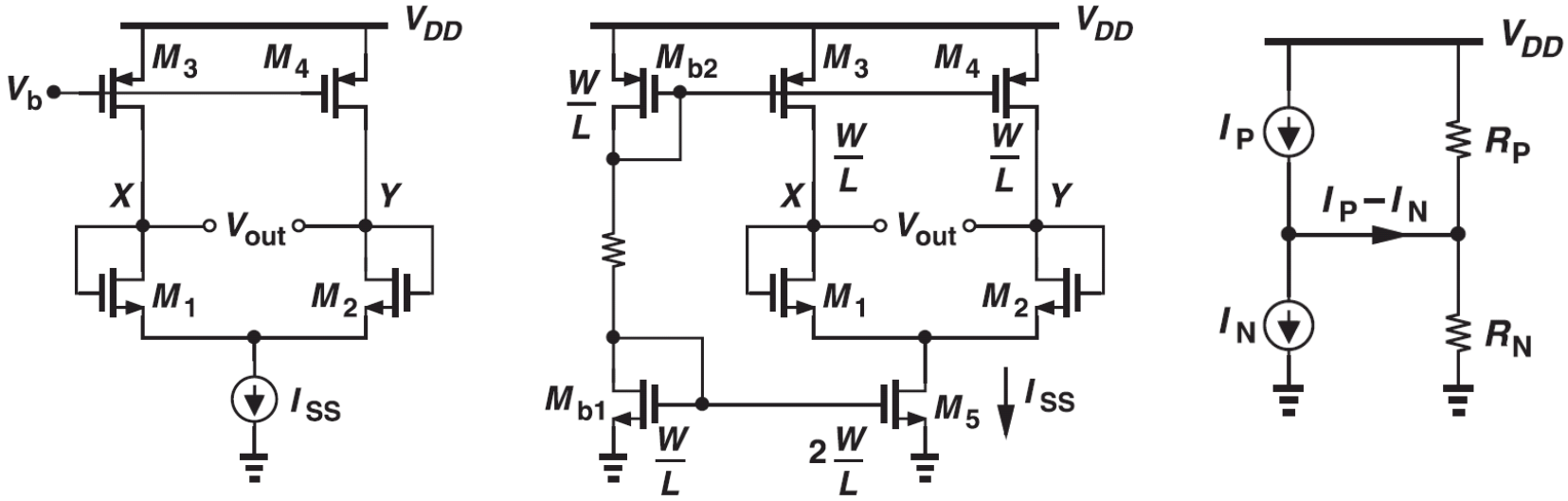
Common Mode Feedback

- Advantages of differential architecture
  - Higher noise immunity.
  - Higher output swing.
  - No mirror poles, thus achieving a higher closed-loop speed.
  - High-gain differential circuits require “common-mode feedback” (CMFB).



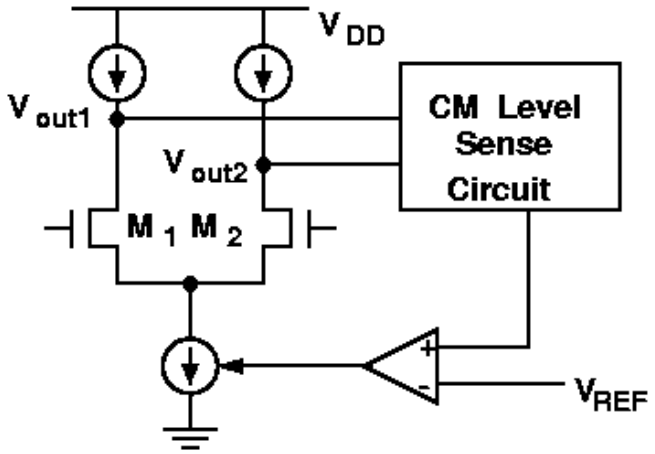
- For differential negative feedback, we short the inputs and outputs.
- In this case,
  - $V_{o,cm} = V_{DD} - I_{SS} R_D/2$

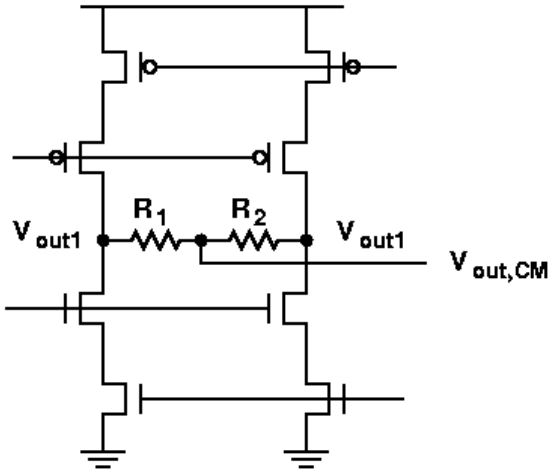
High-Gain DP with I/O Shorted



- For high gain DP with active load, assume $I_{D1} = I_{D2} = I_{SS}/2$ with I/O shorted.
- The output CM levels depends on how close I_{D3} and I_{D4} are to $I_{SS}/2$.
- If the drain currents of M_3 and M_4 in the saturation region are slightly greater than $I_{SS}/2$, *both* M_3 *and* M_4 *must enter the triode region,* $I_D(M_3, M_4)$ *fall to* $I_{SS}/2$.
- if $I_{D3,4} < I_{SS}/2$, then both V_X and V_Y *must drop,* M_5 *enters the triode region.*
- In high gain amplifiers, the ΔI of I_P and I_N must flow through the intrinsic r_o of the amplifier, creating an output voltage change of $(I_P - I_N)(R_P \,//\, R_N)$.
- The voltage error may be large, thus driving the p-type or n-type current source into the triode region.

Conceptual Topology of CM Feedback



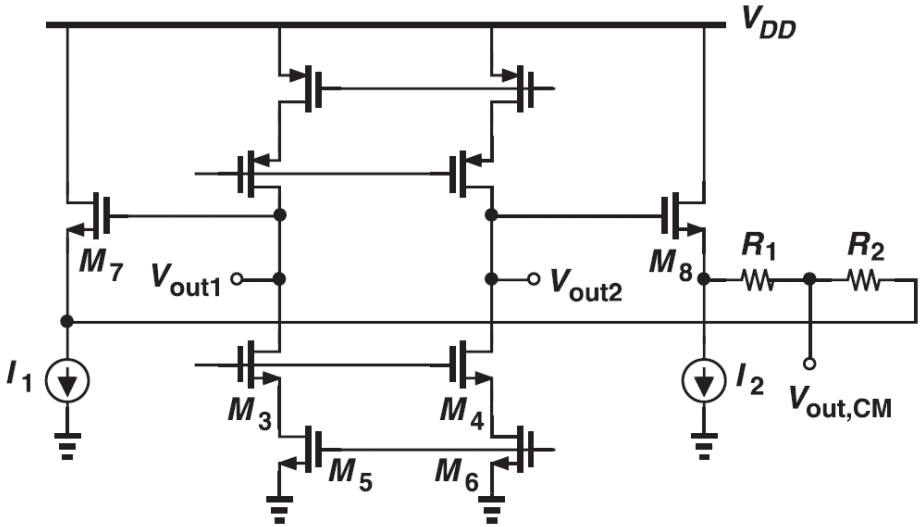


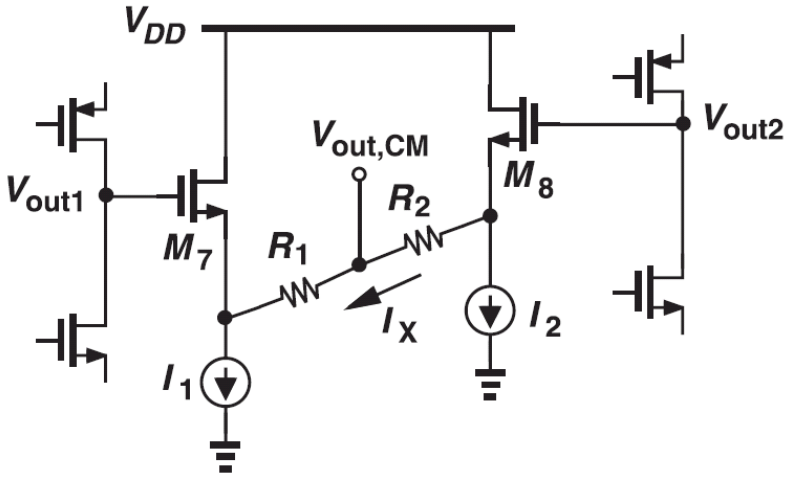
- The output common mode level is quite sensitive to device properties and mismatches and it can not be stabilized by means of *differential* feedback.
- The *task of common mode feedback*
  - Sensing the output CM level*, comparison with a reference, and returning the error to the amplifier's bias network.*
- Sense the output common mode level by a voltage divider

$$V_{out,CM} = (R_1 V_{out2} + R_2 V_{out1}) / (R_1 + R_2) = (V_{out1} + V_{out2}) / 2 \quad \cdots \quad \text{if } R_1 = R_2$$

- R_1 and R_2 must be much greater than the output impedance of the op amp so as to avoid lowering the open loop gain – large area and capacitance.

Common Mode Feedback Topology





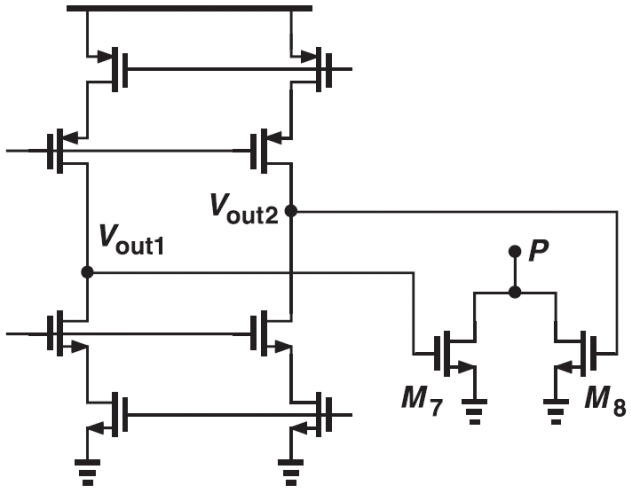
- To eliminate the resistive loading, we can interpose source followers between each output and its corresponding resistor.
- R_1 and R_2 or I_1 and I_2 must be large enough to ensure that M_7 or M_8 is not "starved" when a large differential swing appears at the output, i.e.,

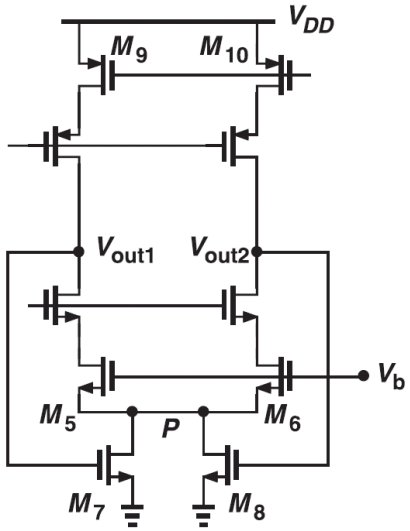
$$I_X \approx (V_{out2} - V_{out1})/(R_1 + R_2), \quad I_1 = I_X + I_{D7}, \quad I_{D7} = I_1 - I_X > 0$$

- Otherwise, I_{D7} drops to '0' and $V_{out,CM}$ no longer be the true output CM level.
- The differential output swing is limited.

$$V_{out1,\min} = V_{GS7} + V_{I1} \quad \text{with CMFB} \qquad V_{out1,\min} = V_{OD3} + V_{OD5} \quad \text{without CMFB}$$

CM Sensing with Triode MOSFET



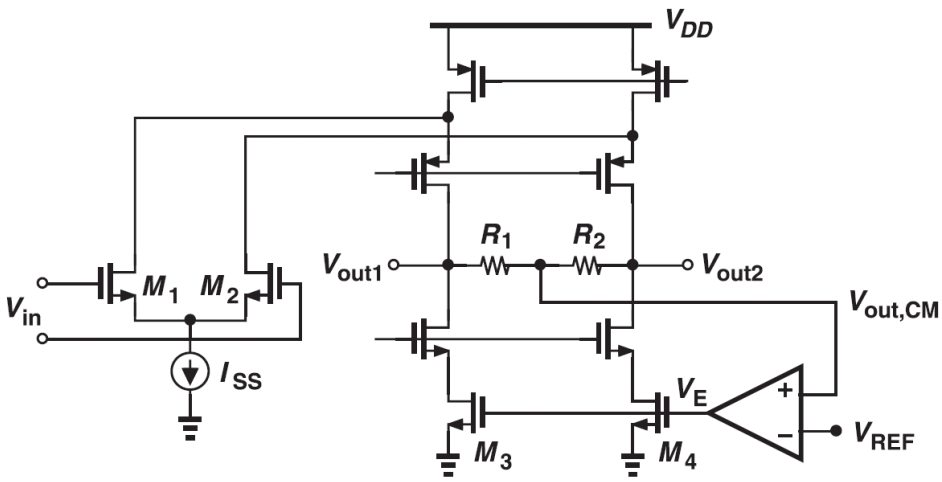


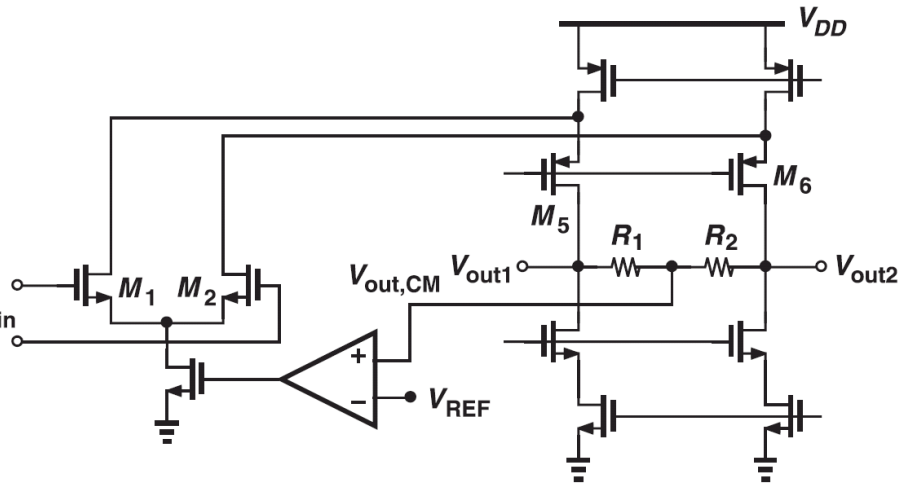
- Identical transistors M7 and M8 operate in deep triode region, introducing a total resistance between *P* and ground equal to

$$R_{tot} = R_{on7} \parallel R_{on8} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out1} - V_{TH})} \parallel \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out2} - V_{TH})} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out1} + V_{out2} - 2V_{TH})}$$

- R_{tot} is a function of $V_{out1} + V_{out2}$ but independent of $V_{out2} - V_{out1}$.
- If the outputs rise together, then R_{tot} drops.
- The use of M_7 and M_8 limits the output voltage swings. $V_{out,min} = V_{TH7,8}$
- If V_{out1} drops from the equilibrium CM level to one V_{TH} above ground and V_{out2} rises by the same amount, then M_7 enters the saturation region.

Sensing / Controlling Output CM Level





- We employ a simple amplifier to detect the ΔV of $V_{out,CM}$ and V_{REF}, applying the result to the NMOS current sources with negative feedback.

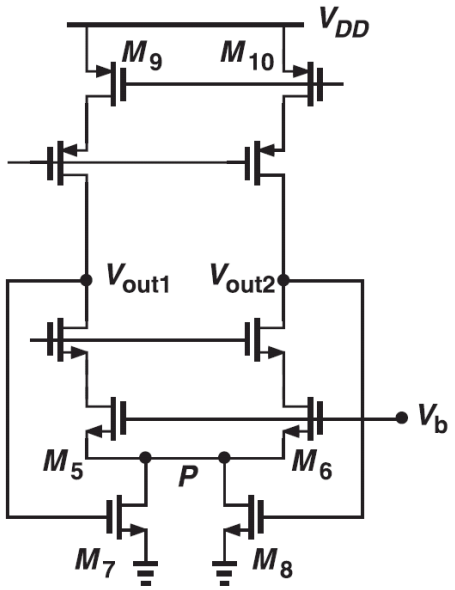
$$\text{If } V_{out,CM}\uparrow \Rightarrow V_E\uparrow \Rightarrow I_{D3},\ I_{D4}\uparrow \Rightarrow V_{out,CM}\downarrow$$

- The feedback can be applied to the PMOS current sources as well.
- The feedback may control only a fraction of the I_{source} to allow optimization of the settling behavior, i.e., the I_{source} can be decomposed into two parallel devices, one biased at a constant I and the other driven by the error amplifier.
- In a folded-cascode op amp, the CM feedback may control the tail current of the input differential pair.

$$\text{If } V_{out,CM}\uparrow \Rightarrow I_{D1},\ I_{D2}\uparrow \Rightarrow V_{out,CM}\downarrow$$

CMFB Using Triode Devices

- The output CM voltage is directly converted to a resistance or a current, prohibiting comparison with a reference voltage.
- $R_{on7} \,||\, R_{on8}$ adjusts the bias current of M_5 and M_6.
- The output CM level sets $R_{on7} \,||\, R_{on8}$ *such that* I_{D5} *and* I_{D6} *exactly balance* I_{D9} *and* I_{D10}.
- Assuming $I_{D9} = I_{D10} = I_D$, we must have

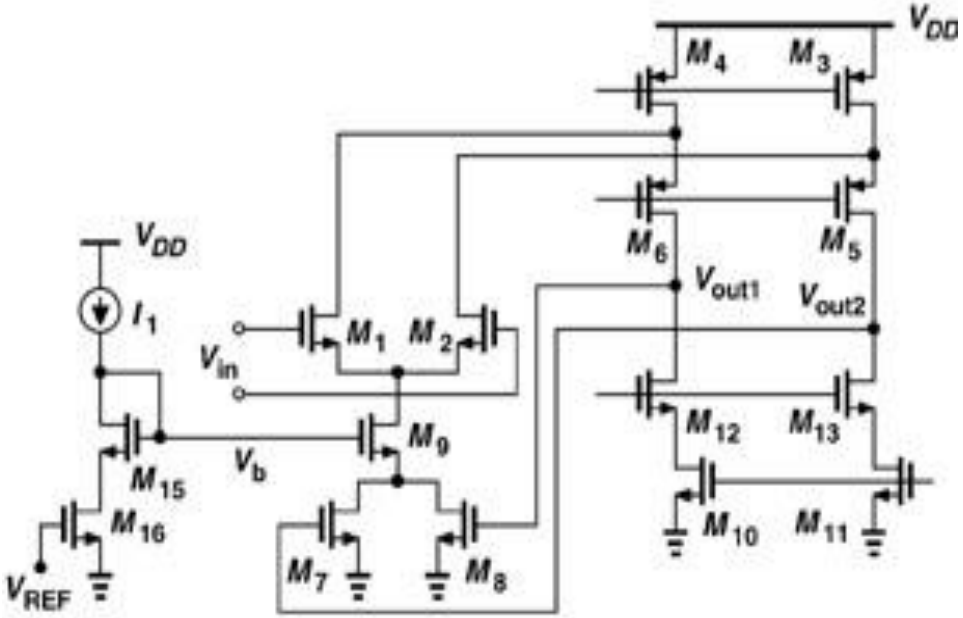


$$V_b - V_{GS5} = 2I_D\left(R_{on7} \,||\, R_{on8}\right), \qquad R_{on7} \,||\, R_{on8} = \frac{V_b - V_{GS5}}{2I_D}$$

$$\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}\left(V_{out1} + V_{out2} - 2V_{TH}\right)} = \frac{V_b - V_{GS5}}{2I_D}, \quad V_{out1} + V_{out2} = \frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}}\frac{1}{V_b - V_{GS5}} + 2V_{TH}$$

- Disadvantages
  - The value of the output CM level is a function of device parameters.
  - The voltage drops across $R_{on7} \,||\, R_{on8}$ limits the output voltage swings.
  - M_7 *and* M_8 are usually quite wide devices ➔ large capacitance at the output.
  - $V_{out,CM}$ is somewhat sensitive to the value of V_b.

Modification of CMFB

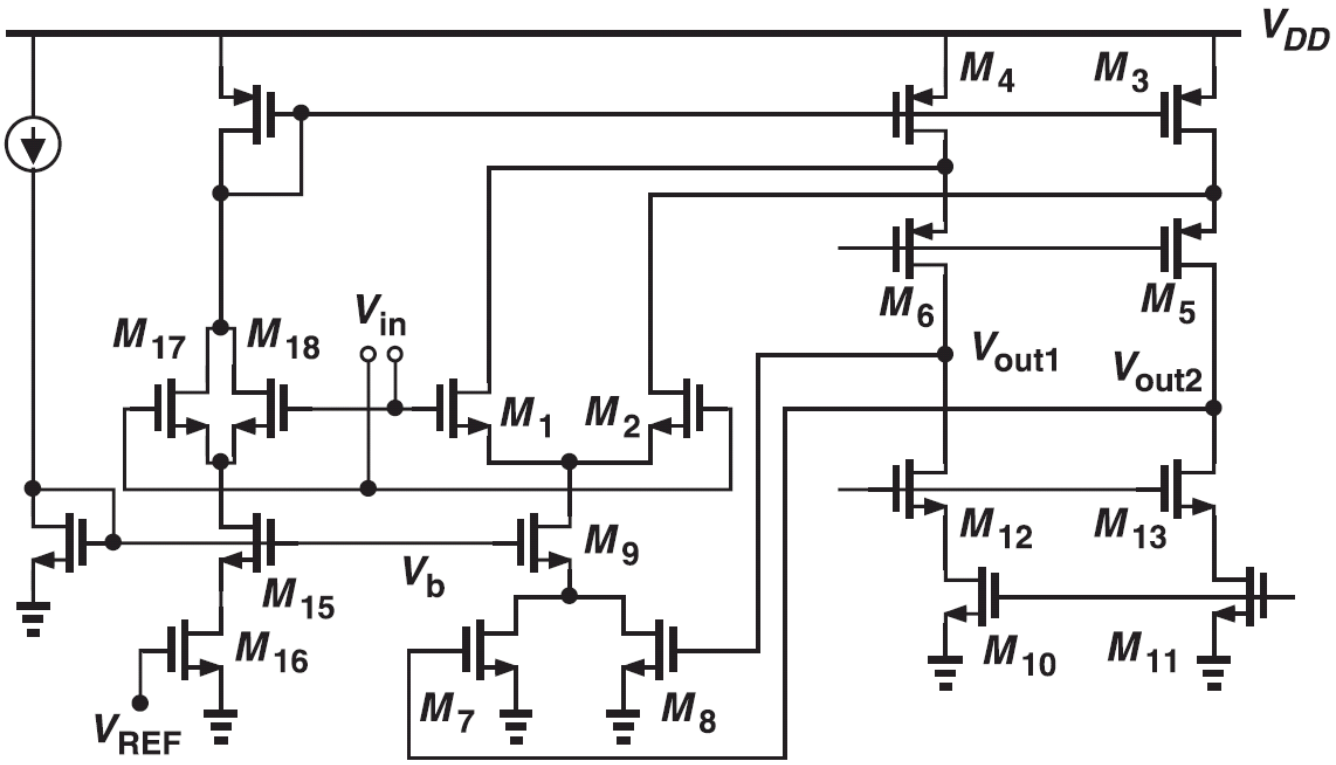


- Define V_b by a current mirror arrangement such that I_{D9} tracks I_1 and V_{REF}.
- Suppose

$$(W/L)_{15} = (W/L)_9 \qquad (W/L)_{16} = (W/L)_7 + (W/L)_8$$

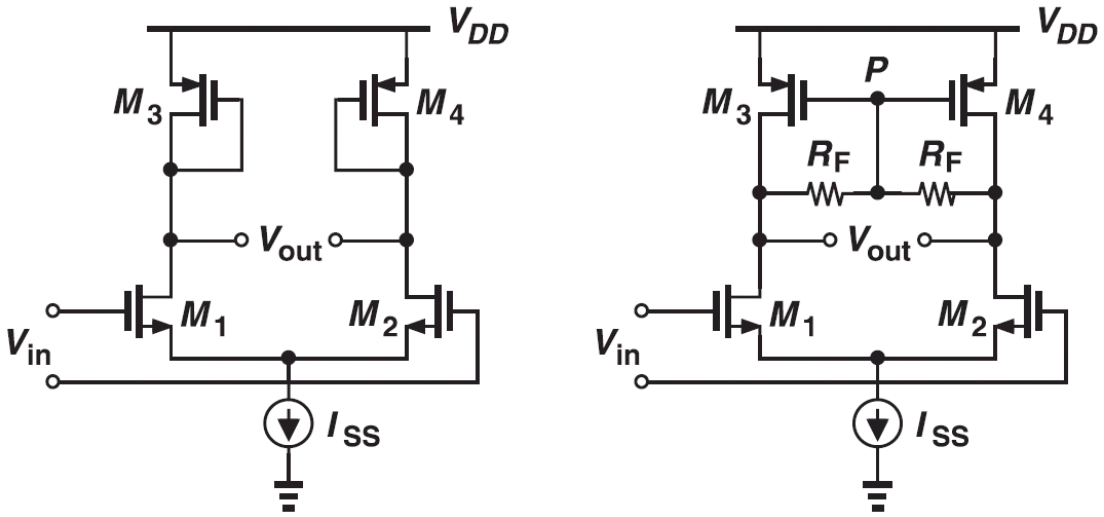
- Thus ***$I_{D9} = I_1$ only if $V_{out,CM} = V_{REF}$.***
- The circuit produces an output CM level equal to a reference but it requires no resistors in sensing ***$V_{out,CM}$***.
- In practice, since $V_{DS15} \neq V_{DS9}$, channel length modulation results in a finite error.

Suppress Error Due to r_O



- Transistors M_{17} and M_{18} reproduce at the drain of M_{15} a voltage equal to the source voltage of M1 and M2.
- $V_{DS15} = V_{DS9}$

DP using Diode-Connected Loads



- Differential pair with diode connected load
  - The output CM level, V_{DD} - $V_{GS3,4}$ is relatively well-defined, but the voltage gain is quite low.
- For differential changes at V_{out1} and V_{out2}, node P is virtual ground and the gain can be expressed as

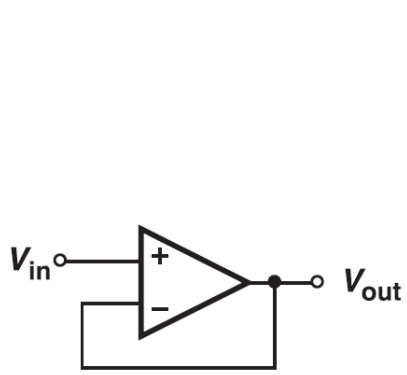
$$A_v = g_{m1,2}\left(r_{O1,2} \parallel r_{O3,4} \parallel R_F\right)$$

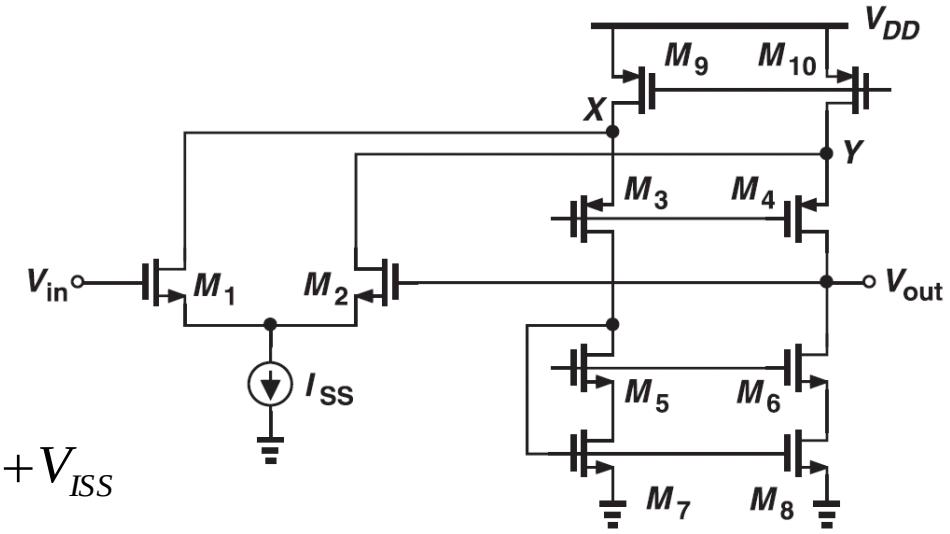
- For common mode levels, M_3 and M_4 operate as diode-connected devices.
- Fully differential two stage op amps require two CMFB networks.

Outline

1. General Consideration
2. One-Stage Op Amps / Two-Stage Op Amps
3. Gain Boosting
4. Common-Mode Feedback
5. **Input Range / Slew Rate**
6. Power Supply Rejection / Noise in Op Amps

Input Range Limitations

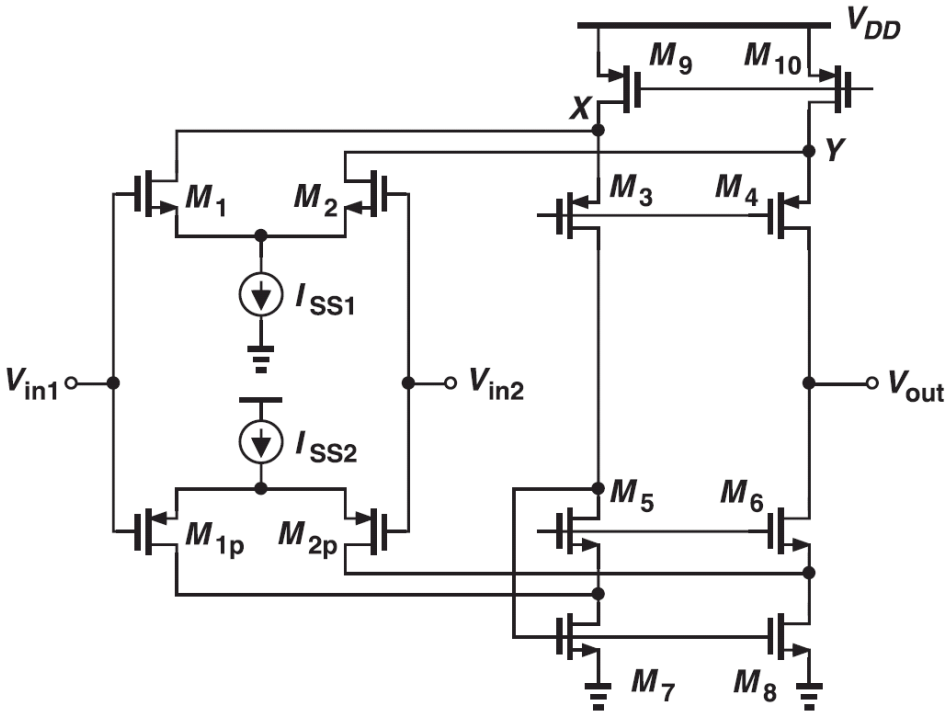


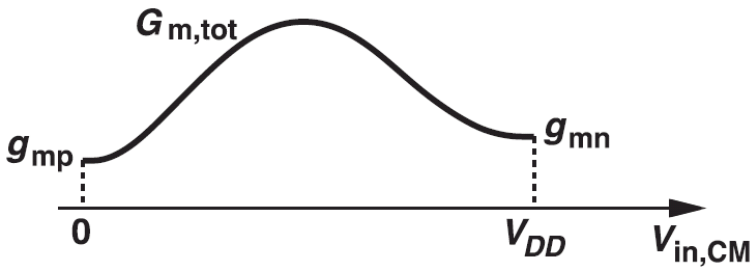


$$V_{in,\min} \approx V_{out,\min} = V_{GS1,2} + V_{ISS}$$

- The input CM level may need to vary over a wide range in some applications.
- The voltage swings may be limited by the input differential pair rather than the output cascode branch.
- If $V_{out} < V_{in,min}$, I_{SS} enters the triode region and the transconductance of the differential pair decreases.
- The limitation can be overcome if the transconductance can somewhat be restored.

Extension of Input CM Range

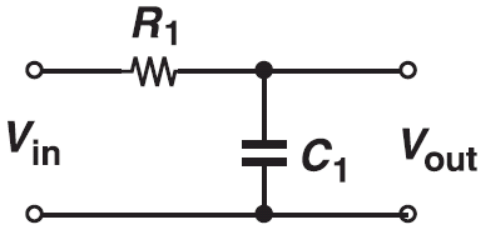


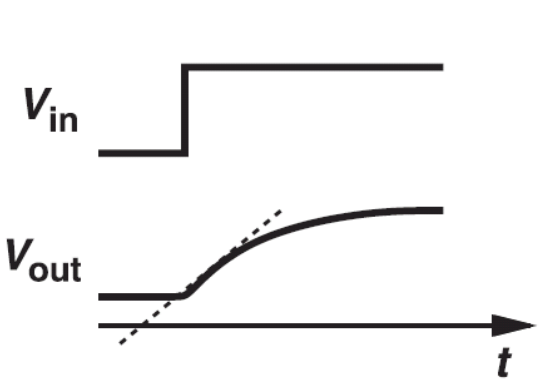


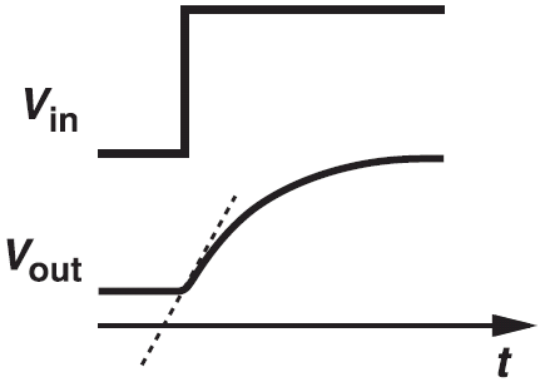
- Incorporate both NMOS and PMOS DPs such that when one is "dead", the other is "alive".

- The variation of the overall g_m of the two pairs as the input CM level changes.
- Many properties of the circuit, including gain, speed, and noise vary.
- For minimizing input transconductance variation
  - Ref R. Hogervost et al, " A Compact Power Efficient 3-V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", JSSC, pp.1505-1513, Dec 1994

Slew Rate







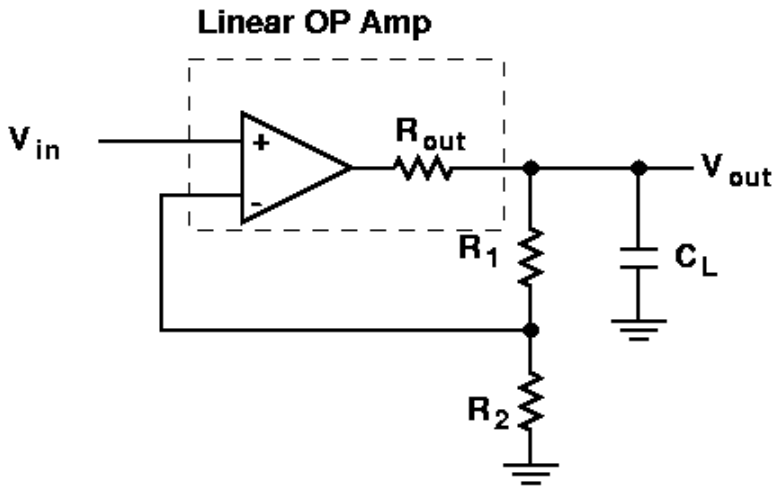
- Op amps used in feedback circuits exhibit a large-signal behavior called “slewing”.
- Linear system vanishes during slewing.
- Consider a simple RC network (http://en.wikipedia.org/wiki/RC_circuit)

$$V_{out} = V_0\left[1 - \exp\left(-t/\tau\right)\right] \qquad \tau = RC \qquad \frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\frac{-t}{\tau}$$

- The slope of the step response is proportional to the final value of the output.
- ***Linear System*** : If we double the input amplitude, the output signal level must double at every point.

Step Response of Linear OP Amp

- Assume the op amp is linear



$$\left[\left(V_{in}-V_{out}\frac{R_2}{R_1+R_2}\right)A-V_{out}\right]\frac{1}{R_{out}}=\frac{V_{out}}{R_1+R_2}+V_{out}C_L s$$

If $R_1+R_2 >> R_{out}$

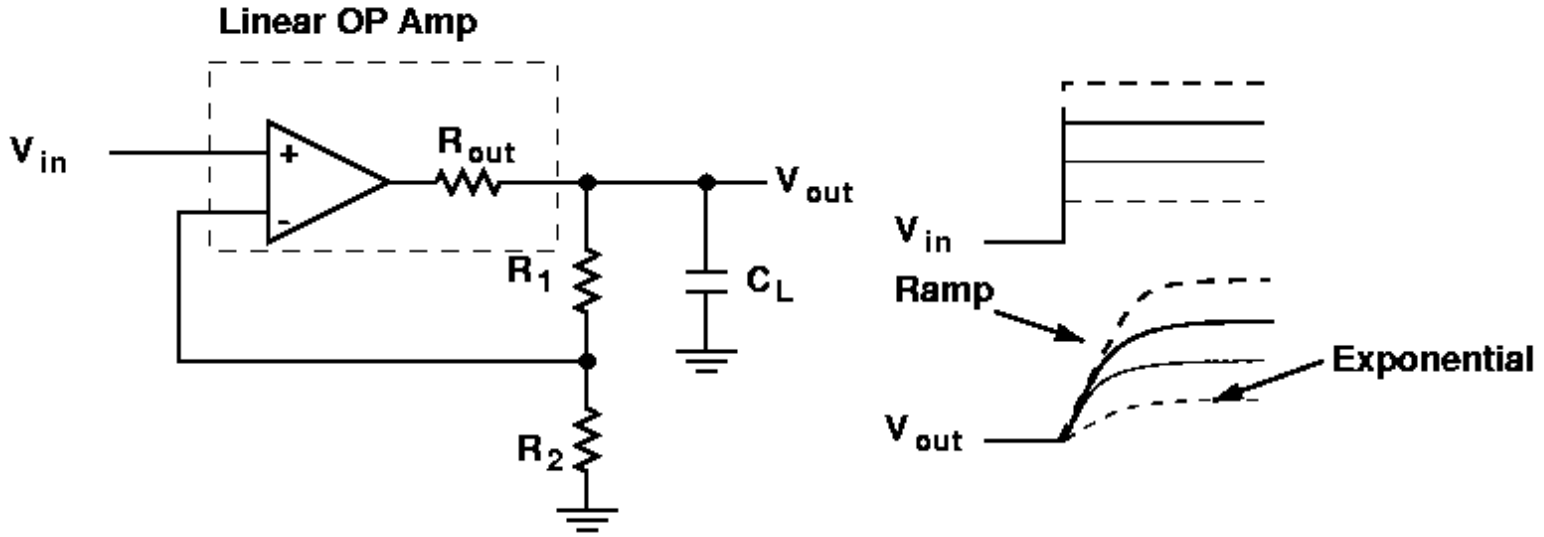
$$\frac{V_{out}}{V_{in}}(s)\approx\frac{A}{\left(1+\frac{AR_2}{R_1+R_2}\right)\left[1+\frac{R_{out}C_L}{1+AR_2/(R_1+R_2)}s\right]}$$

- Both the low-frequency gain and the time constant are divided by $1+AR_2/(R_1+R_2)$
- The step response is given by

$$V_{out}(t)=V_0\frac{A}{1+\frac{AR_2}{R_1+R_2}}\left[1-\exp\frac{-t}{\frac{R_{out}C_L}{1+AR_2/(R_1+R_2)}}\right]\text{u(t)}$$

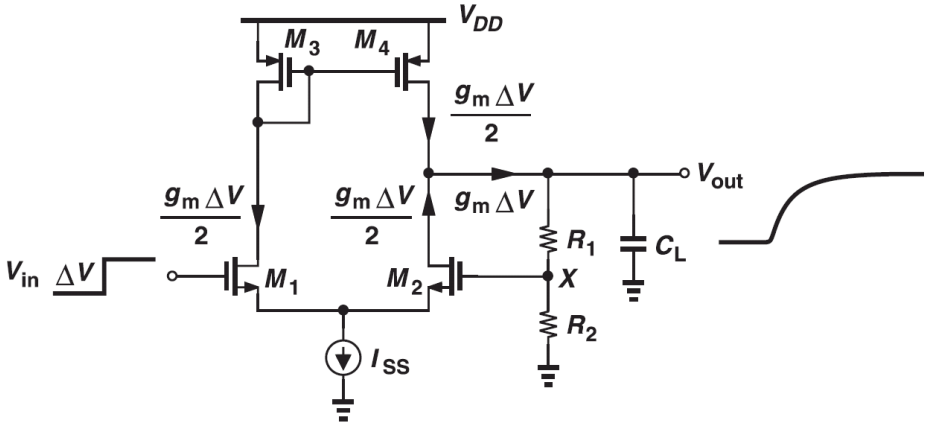
- Linear Settling : the slope is proportional to the final value (***exponential response***).

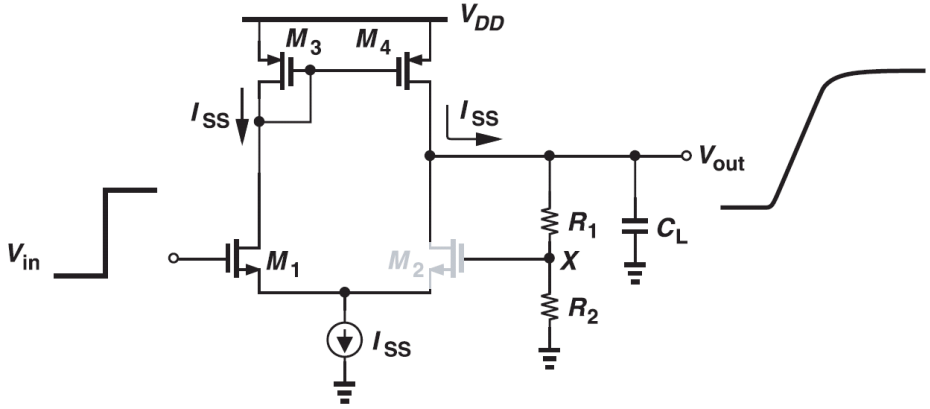
Slewing in an OP Amp Circuit

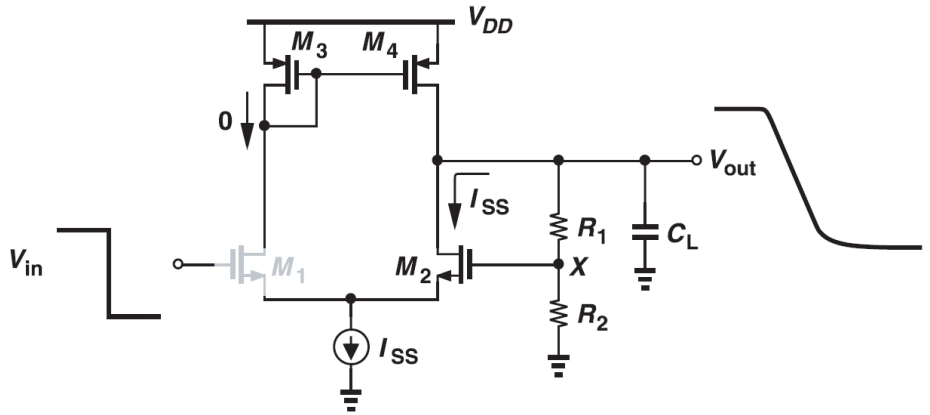


- The step response of the circuit begins to deviate from linear response as the input amplitude increases.
- The response to sufficiently small inputs follows the exponential curve, but with large input steps, the output displays a linear ramp having a constant slope.
- Under this condition, the op amp experiences slewing and call the slope of the ramp the “slew rate”.

Slewing During Transition







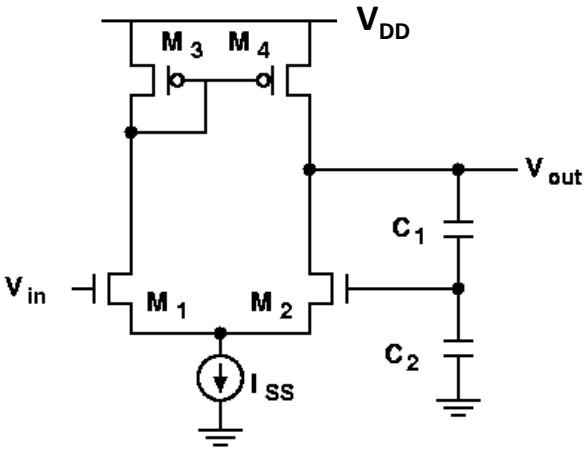
- Assume that $R_1 + R_2$ is quite large.
- If V_{in} experiences a change of ΔV, I_{D1} increases by $g_m \Delta V/2$.
- The total small-signal $I_{out} = g_m \Delta V$.
- I_{out} will charge C_L, but as V_{out} rises, so does V_X, ΔV of V_{G1} and V_{G2} ↓, hence I_{out} ↓.

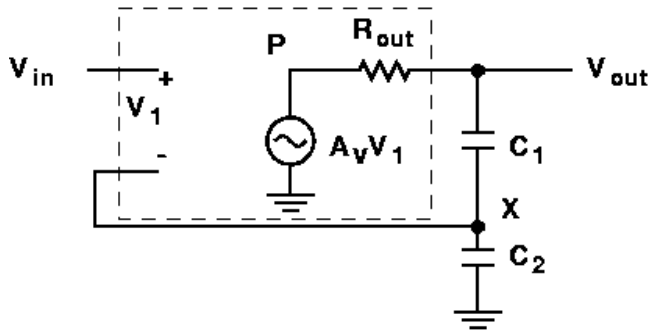
- If ΔV is so large that M_1 absorbs all of I_{SS}, M_2 is turned off, generating a ramp output with a slope equal to I_{SS}/C_L (feedback is broken). (neglect I of R_1, R_2)
- $V_X \rightarrow V_{in}$, M_2 turns on, and the circuit returns to linear operation.

Slewing During Transition

- Large signal speed is limited by the slew rate because the current available to charge and discharge the dominant capacitor in the circuit is small.
- The input-output relationship during slewing is nonlinear.
- To amplify a sinusoid $V_o \sin \omega_o t$, *its slew rate must exceed* $V_o \omega_o$.

Feedback Amplifier Example





$$A_v = g_{m1,2}\left(r_{O2} \parallel r_{O4}\right),$$

$$R_{out} = r_{O2} \parallel r_{O4},$$

$$V_X = \frac{C_1 V_{out}}{C_1 + C_2},$$

$$V_P = \left(V_{in} - \frac{C_1}{C_1 + C_2} V_{out}\right) A_v$$

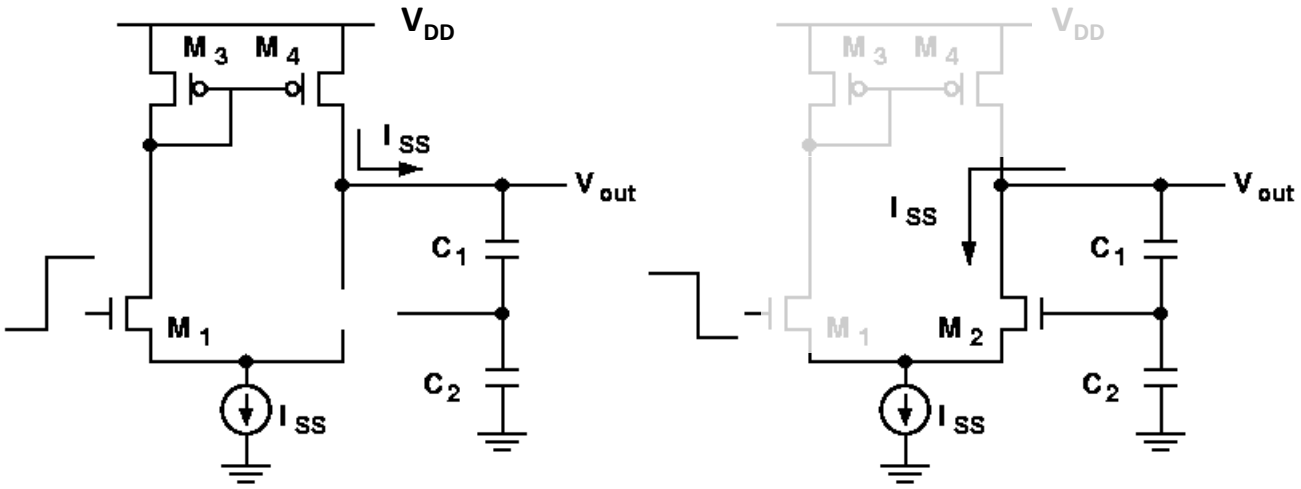
$$\left[\left(V_{in} - \frac{C_1}{C_1 + C_2} V_{out}\right) A_v - V_{out}\right] \frac{1}{R_{out}} = V_{out} \frac{C_1 C_2}{C_1 + C_2} s$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_v}{1 + A_v \frac{C_1}{C_1 + C_2} + \frac{C_1 C_2}{C_1 + C_2} R_{out} s} = \frac{A_v / \left[1 + A_v C_1 / (C_1 + C_2)\right]}{1 + \frac{C_1 C_2}{C_1 + C_2} R_{out} s / \left(1 + A_v \frac{C_1}{C_1 + C_2}\right)}$$

- Both the low-frequency gain and the time constant of the circuit have decreased by a factor of $1 + A_v C_1 / (C_1 + C_2)$
- Unity step response $V_{out}(t) = \frac{A_v}{1 + A_v \frac{C_1}{C_1 + C_2}} V_0 \left(1 - \exp\frac{-t}{\tau}\right) u(t), \quad \tau = \frac{C_1 C_2}{C_1 + C_2} \frac{R_{out}}{1 + A_v \frac{C_1}{C_1 + C_2}}$

Feedback Amplifier Slewing

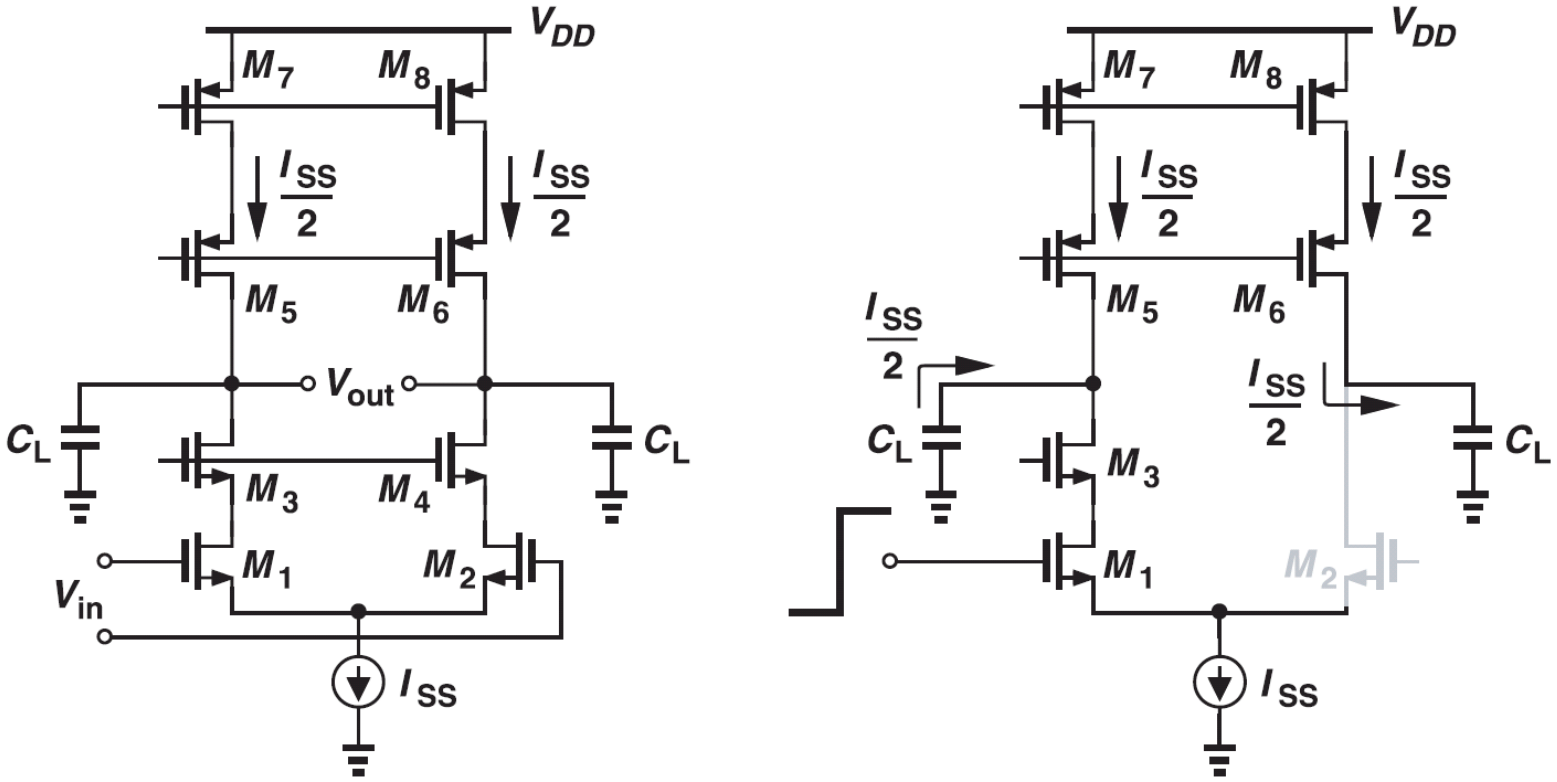
- Positive & Negative Slewing



$$V_{out}(t) = \frac{I_{SS}t}{\left[\frac{C_1C_2}{C_1+C_2}\right]}$$ positive step,

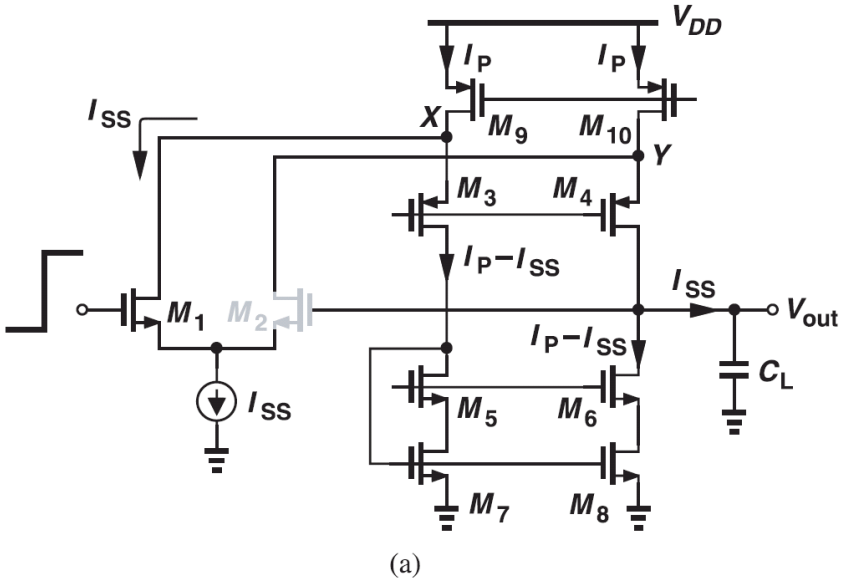
$$V_{out}(t) = \frac{-I_{SS}t}{\left[\frac{C_1C_2}{C_1+C_2}\right]}$$ negative step

Slewing in Telescopic Op Amp

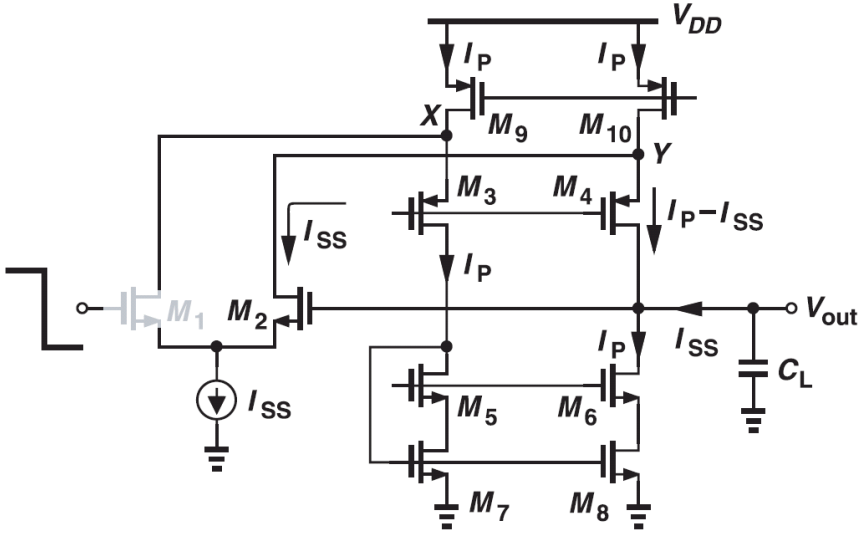


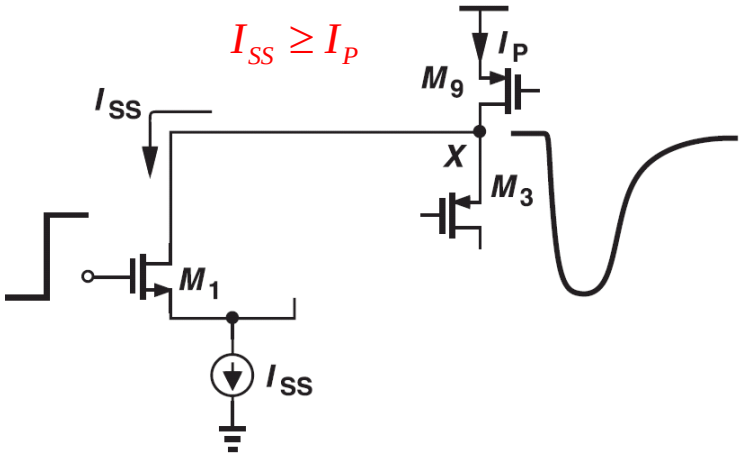
- When a large differential input is applied, M_1 or M_2 turns off.
- V_{out1} and V_{out2} appear as ramps with slopes equal to $\pm I_{SS}/2C_L$
- V_{out1} - V_{out2} exhibits a slew rate equal to I_{SS}/C_L.

Slewing in Folded Cascode Op Amp



(a)

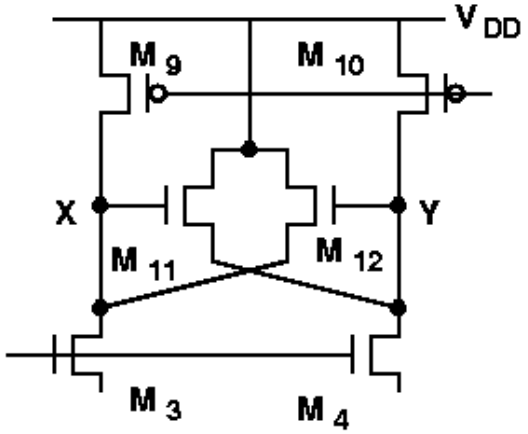




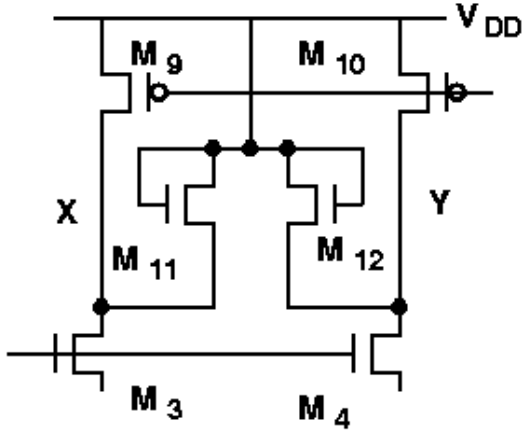
- PMOS current sources I_P.
- The current that charges / discharges C_L is equal to I_{SS}.
- Slew rate ~ I_{SS}/C_L.
- The SR is independent of I_P if $I_P \geq I_{SS}$
- If $I_{SS} \geq I_P$,then during slewing M_3 turns off, and V_X falls to a low level such that M_1 and the tail current source enters the triode region.

Clamp Circuit to Limit Swings

- The difference between I_{SS} and I_P now flows through M_{11} or M_{12}, requiring only enough drop in V_X or V_Y to turn on one of these transistors.



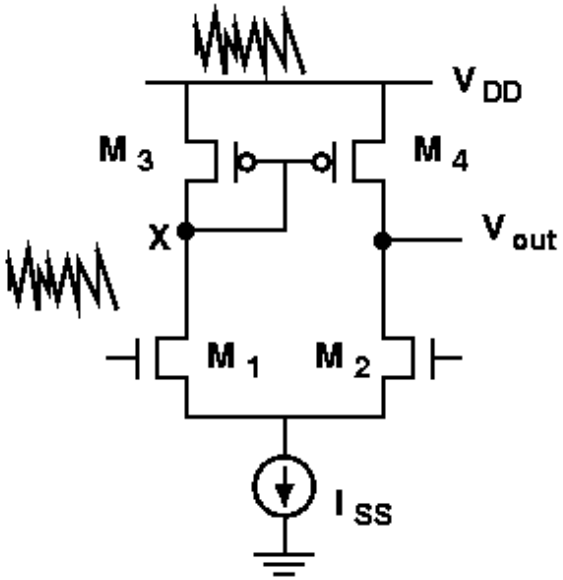
- M_{11} and M_{12} clamp the two diodes directly to VDD.
- The equilibrium value of V_X and V_Y is usually higher than V_{DD} -V_{THN}, M_{11} and M_{12} are off during small-signal operation.
- Trade-offs encountered in increasing the slew rate
  - Slew rate ↑ → I_{SS} ↑ → (W/L) ↑ → Power dissipation ↑ → C_{in} ↑
  - If the device currents and widths scale together, ***$g_m r_o$ of each transistor and hence the open-loop gain of the op amp remain constant.***



Outline

1. General Consideration
2. One-Stage Op Amps / Two-Stage Op Amps
3. Gain Boosting
4. Common-Mode Feedback
5. Input Range / Slew Rate
6. **Power Supply Rejection / Noise in Op Amps**

Power Supply Rejection



$$PSRR \equiv \frac{A_{v,input-output}}{A_{v,V_{DD}-output}}$$

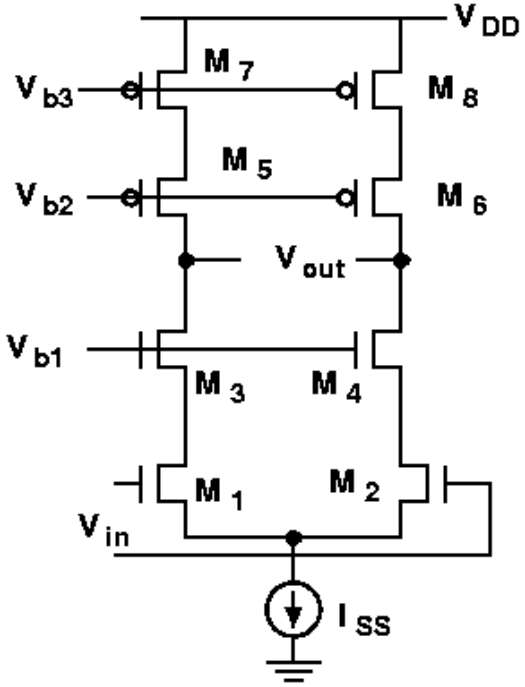
$$A_{v,input-output} = g_{mN}(r_{OP} \| r_{ON})$$

$$A_{v,V_{DD}-output} \approx 1$$

- OP amps are often applied from noisy lines and must therefore “reject” the noise adequately.
- If the circuit is perfectly symmetric, $V_{out} = V_X$. The diode connected device clamps node X to V_{DD}, thus $V_{out} \sim= V_{DD}$.
- The gain from V_{DD} to V_{out} is close to unity.
- The power supply rejection ratio PSRR ~ $g_{mN}(r_{OP}||r_{ON})$

Noise in Op Amps

- Change the gate voltage for each transistor by a small amount and predict the effect at the output.
- At relatively low frequencies, the cascode devices contribute negligible noise.
- M1-M2 and M7-M8 are the primary noises sources.
- The input-referred noise voltage per unit-bandwidth is given by (7-28, p.226, 239)
  - Similar to fully-differential amp.



$$\overline{V_n^2} = 4kT\left(2\frac{2}{3g_{m1,2}} + 2\frac{2g_{m7,8}}{3g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,}^2}{g_{m1,2}^2}$$

Noise in a Folded-Cascode Op Amp

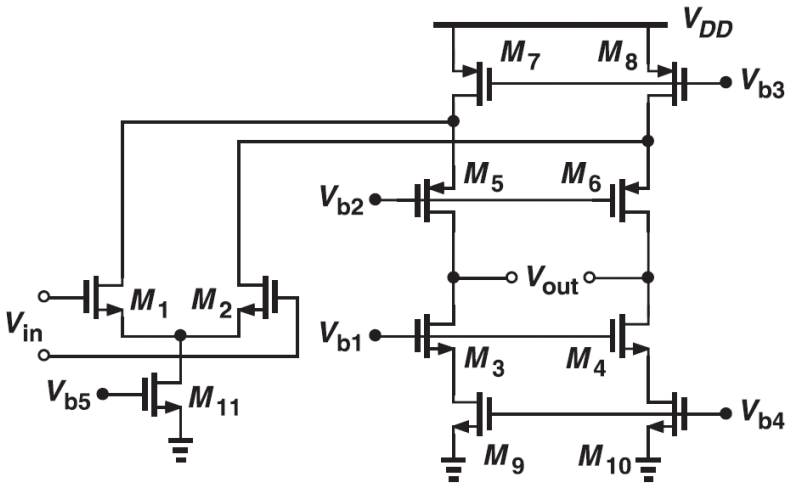
- At relatively low frequencies, the cascode devices contribute negligible noise.
- M_1-M_2, M_7-M_8, M_9-M_{10} are potentially significant noise sources.
- Consider thermal noise only, we first refer the noise of M7-M8 and M9-M10 to the output

$$\overline{V_{n,out}^2}\Big|_{M7,8} = 2\left(4kT\frac{2}{3g_{m7,8}}g_{m7,8}^2R_{out}^2\right)$$

$$\overline{V_{n,out}^2}\Big|_{M9,10} = 2\left(4kT\frac{2}{3g_{m9,10}}g_{m9,10}^2R_{out}^2\right)$$

- Adding the contribution of M_1-M_2, we obtain
  - Larger than telescopic amp.

$$\overline{V_{n,\text{int}}^2} = 8kT\left(\frac{2}{3g_{m1,2}}+\frac{2g_{m7,8}}{3g_{m1,2}^2}+\frac{2g_{m9,10}}{3g_{m1,2}^2}\right)$$



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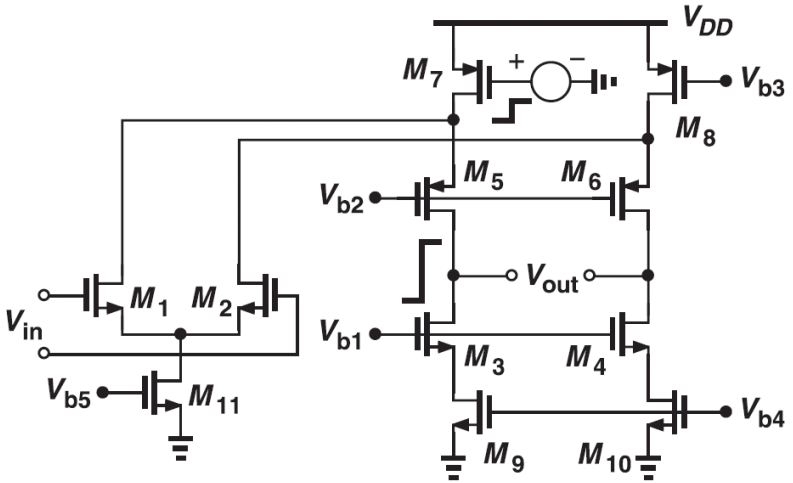


Noise in a Two Stage OP Amp

- The noise current of M_5 and M_7 flows through $r_{O5}||r_{O7}$, the input referred noise contribution of M_5-M_8 is

$$\overline{V_n^2}\Big|_{M5-8} = 2\times 4kT\frac{2}{3}(g_{m5}+g_{m7})(r_{O5}\|r_{O7})^2\frac{1}{g_{m1}^2(r_{O1}\|r_{O3})^2 g_{m5}^2(r_{O5}\|r_{O7})^2}$$

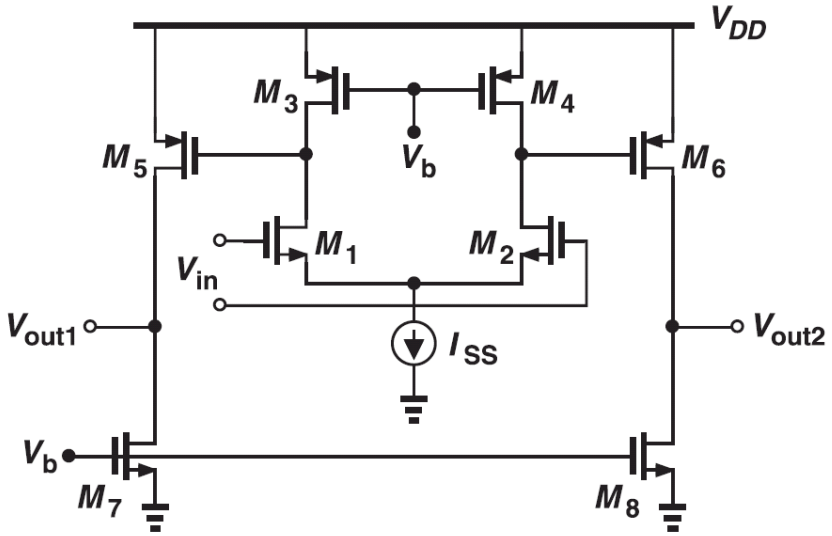
$$= \frac{16kT}{3}\frac{g_{m5}+g_{m7}}{g_{m1}^2(r_{O1}\|r_{O3})^2 g_{m5}^2}$$

- The noise due to M_1-M_4 is equal to

$$\overline{V_n^2}\Big|_{M1-4} = 2\times 4kT\frac{2}{3}\frac{g_{m1}+g_{m3}}{g_{m1}^2}$$

- It follows that

$$\overline{V_{n,tot}^2} = \frac{16kT}{3}\frac{1}{g_{m1}^2}\left[g_{m1}+g_{m3}+\frac{g_{m5}+g_{m7}}{g_{m5}^2(r_{O1}\|r_{O3})^2}\right]$$



  - The noise from M5~M8 is negligible, it's divided by gain of first stage.