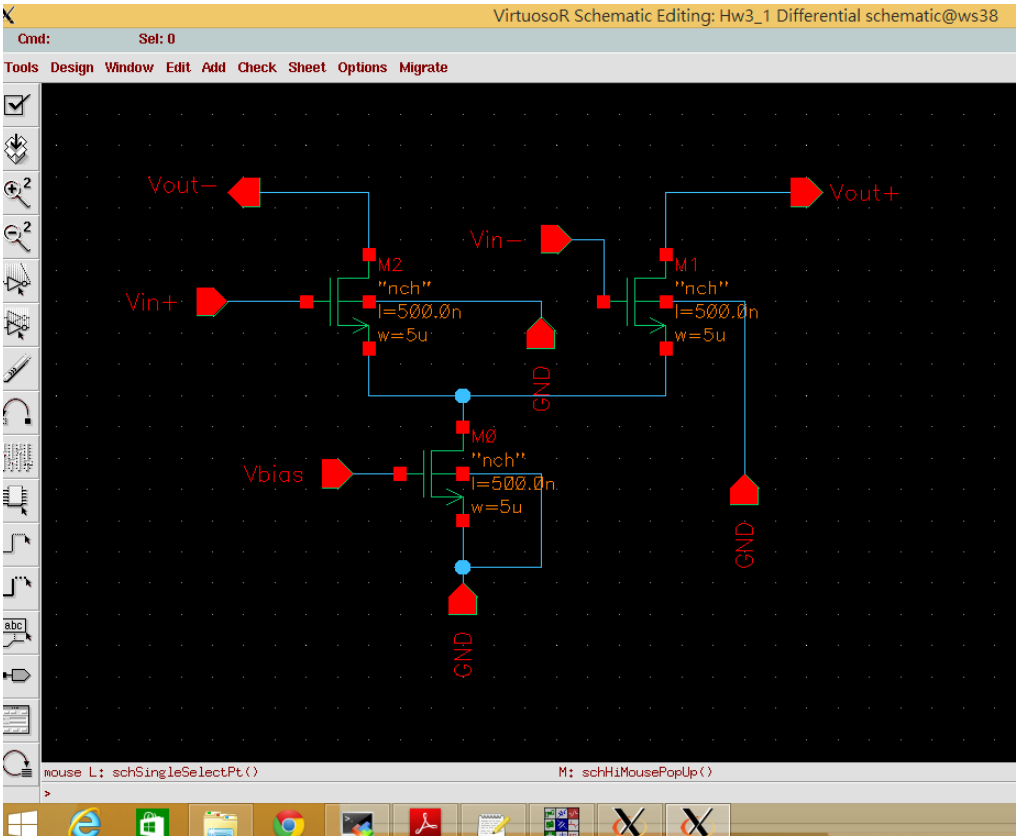
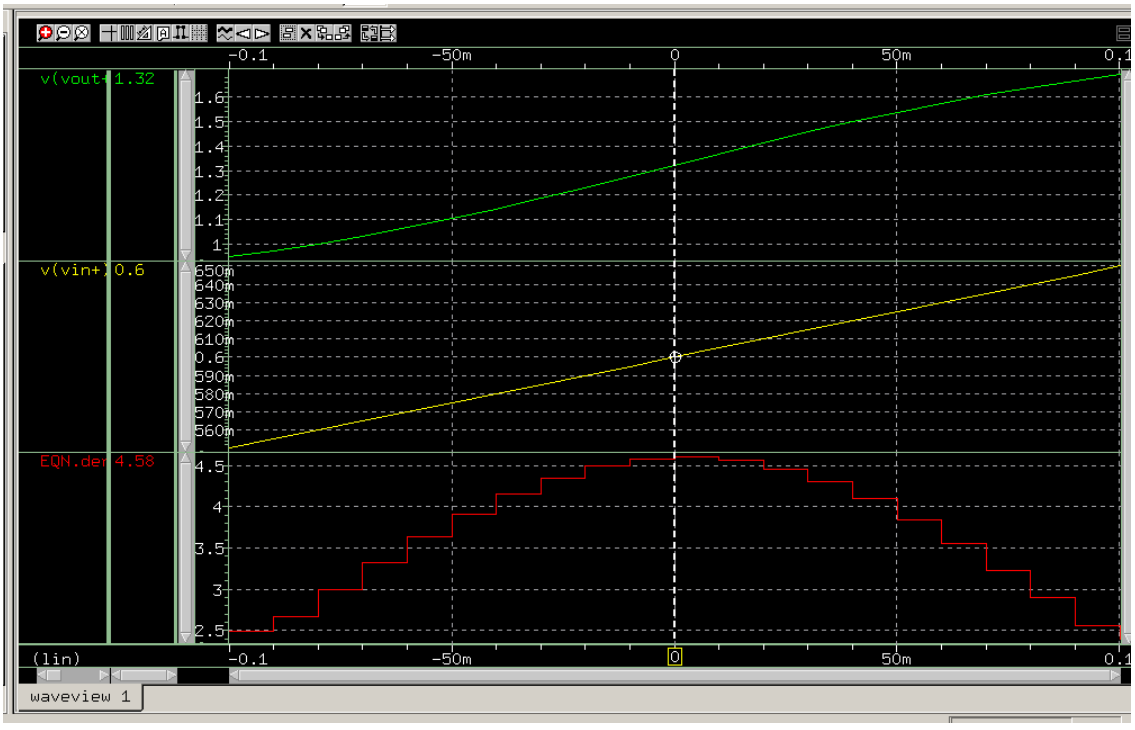
Analog IC Design & Analysis Homework 3 陳彥廷 102061146

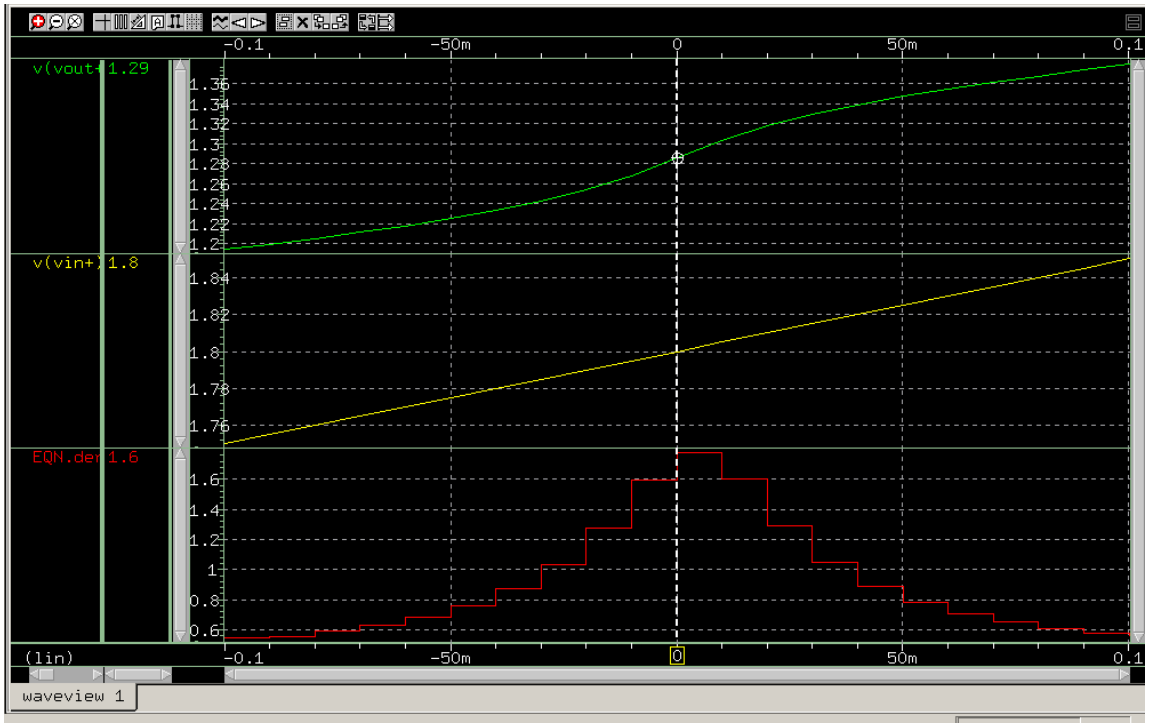
1.Composer：



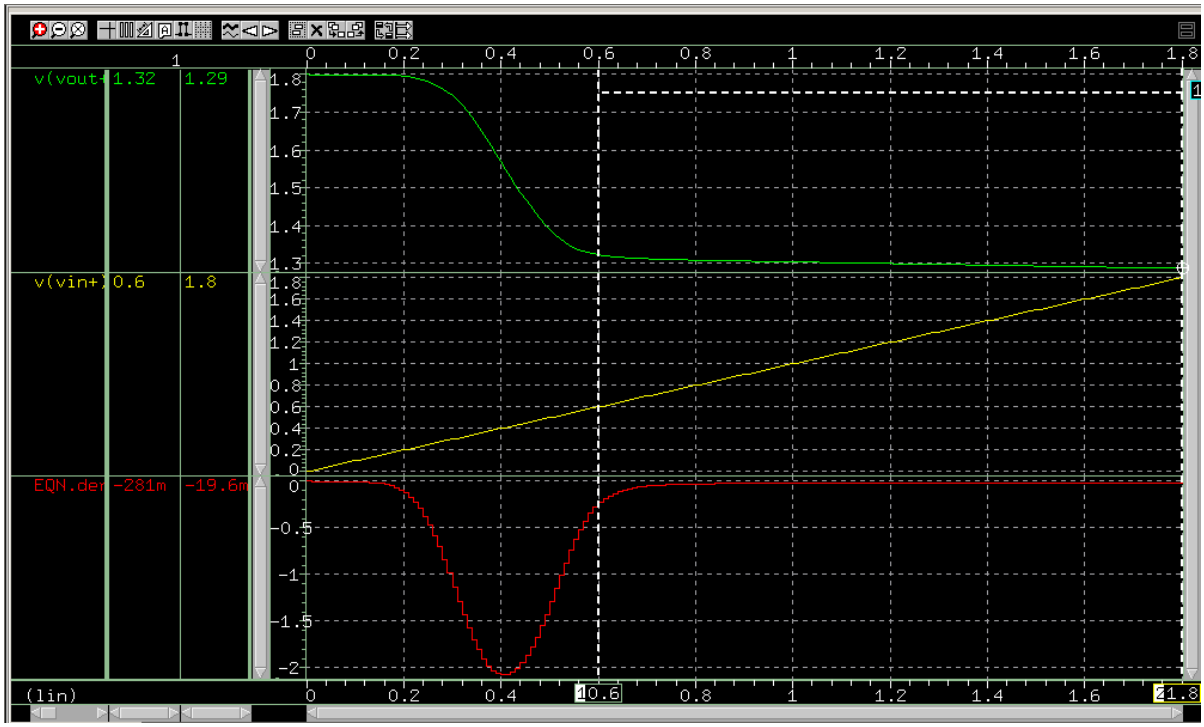
(a) The differential gain for the input common mode voltage = 0.6 V：



The differential gain for the input common mode voltage = 1.8 V：



The common mode gain for both the input common mode voltage = 0.6 and 1.8 V：



To simulate both A_{CM}&A_{DM}, part ofsimulation file should be as followed：

```
X0 GND Vbias Vin+ Vin- Vout+ Vout- Differential

VDD VDD GND 1.8
Vin1 Vin+ GND DC='Vcm' AC=0.5 180
Vin2 Vin- GND DC='Vcm' AC=0.5
RD1 VDD Vout- 200k
RD2 VDD Vout+ 200k
VbVbias GND DC=0.48

.op
.dc Vcm 0 1.8 0.01
*.dc Vdm -0.1 0.1 0.01
.ac DEC 100 100 1G
.end
```

The above is to find the common mode gain of the differential amplifier.

```
X0 GND Vbias Vin+ Vin- Vout+ Vout- Differential

VDD VDD GND 1.8
Vin1 Vin+ GND DC='Vcm+Vdm/2' AC=0.5 180
Vin2 Vin- GND DC='Vcm-Vdm/2' AC=0.5
RD1 VDD Vout- 200k
RD2 VDD Vout+ 200k
VbVbias GND DC=0.48

.op
*.dc Vcm 0 1.8 0.01
.dc Vdm -0.1 0.1 0.01
.ac DEC 100 100 1G
.end
```

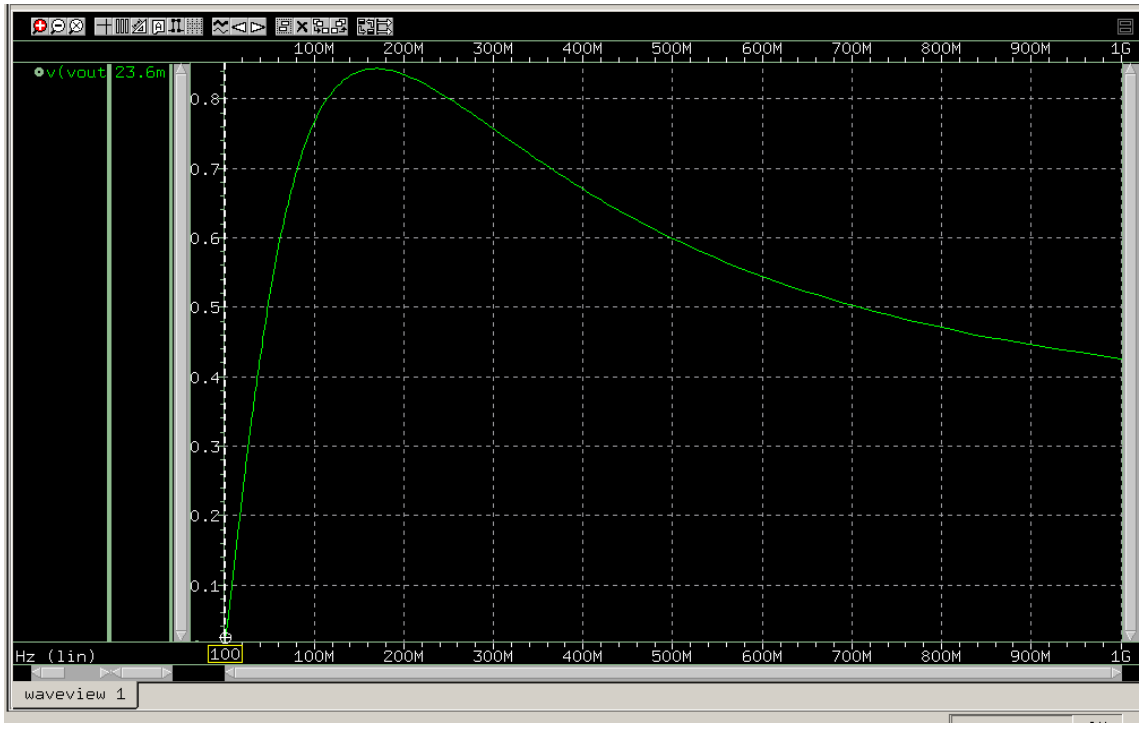
The above is to find the differential gain of the differential amplifier.

(b) The simulation result is shown below：

By hand calculation, the dominant pole frequency =1/[$(r_o // R_D)(1+|\frac{1}{A_{DM}}|)C_{GD}$]

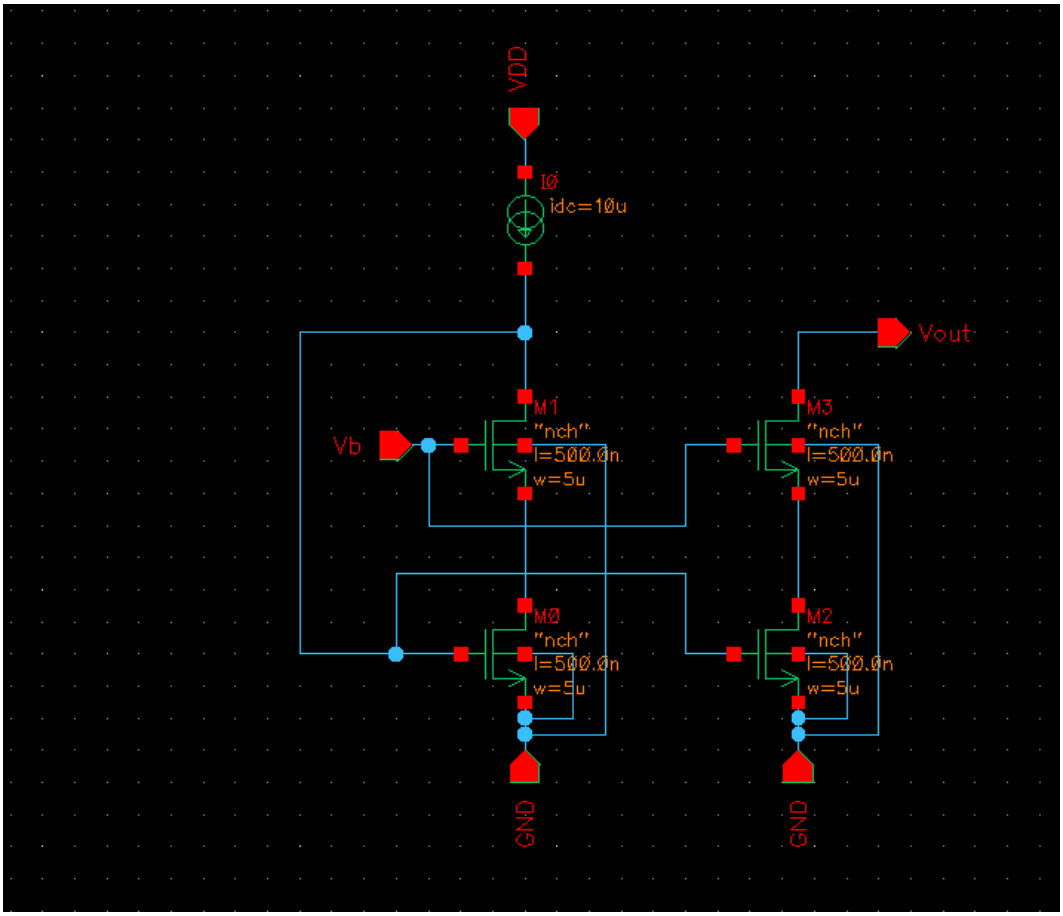
≒ 91.766 MHz based on the figures in .lis file.

(c) The simulation result is shown below：

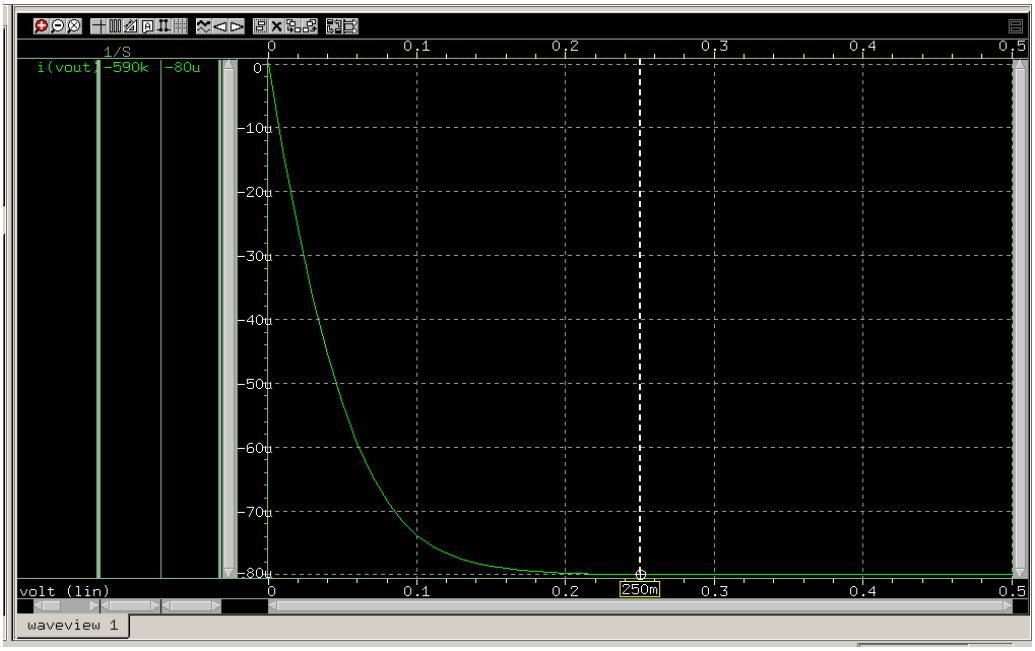


When the system reaches high frequency, the paths of the capacitances are short , making the output impedances drop. Therefore, A_{CM} also drops at high frequency.

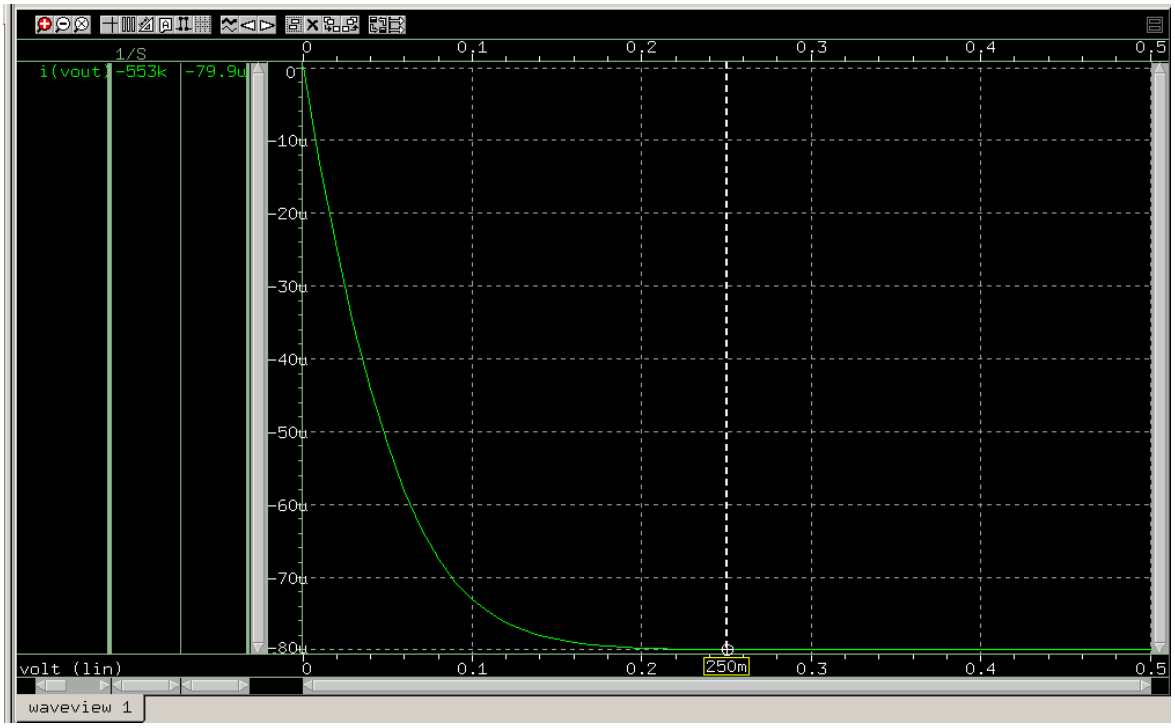
2. Composerfor Fig. 2. (a)：



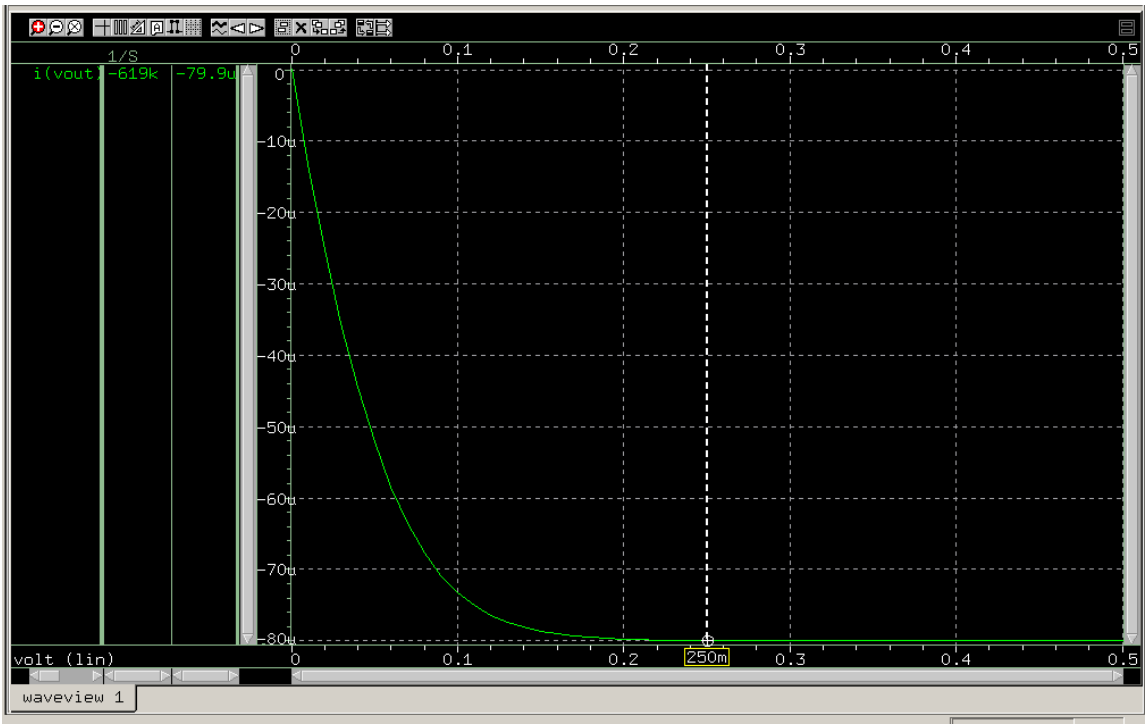
(a) The design results in the output impedance = 590 kΩ when V_{out} = 0.25 V. It's biasedwith the bias voltage 0.53 V and all the sizes of NMOS are 60 u / 15 u, but m = 24, 32, 3, 4 for M_4, M_3, M_2 and M_1 respectively.



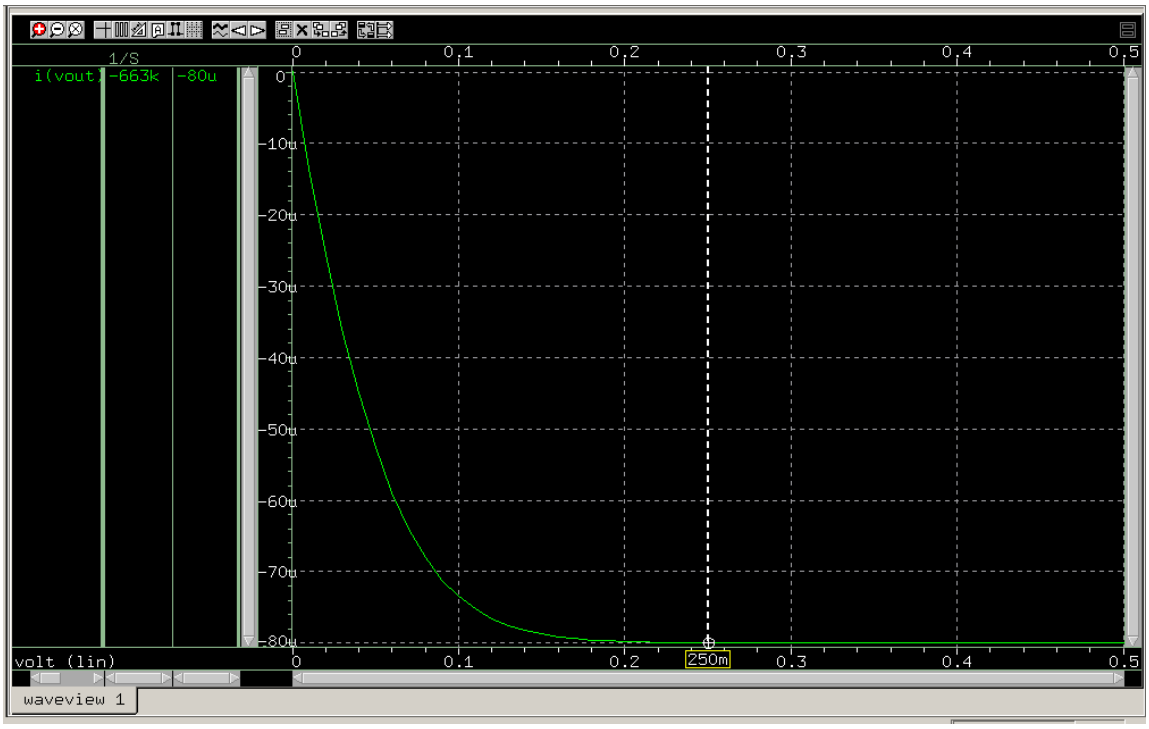
(b) The simulations are shown below：



R_{out} equals 553 kΩ when V_{out} = 0.25 V in SS corner.



R_{out} equals 619 kΩ when V_{out} = 0.25 V in TT corner.



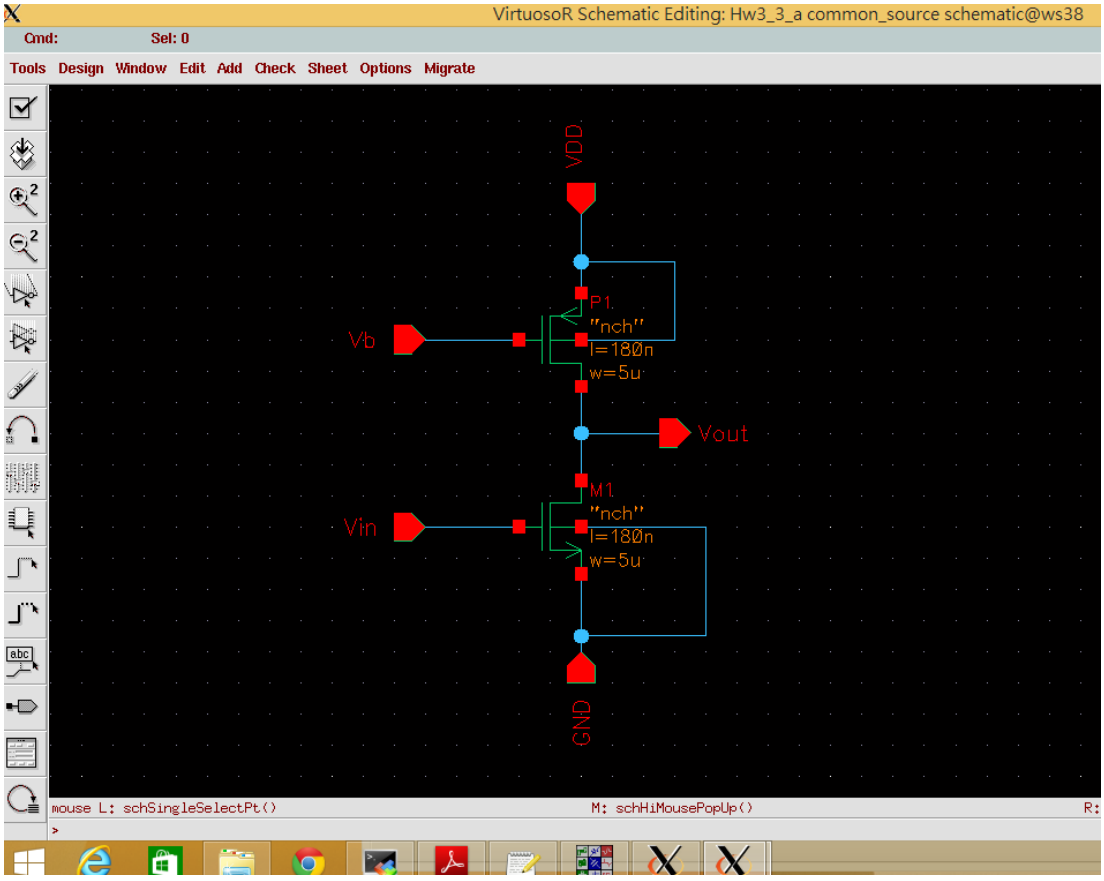
R_{out} equals 663 kΩ when V_{out} = 0.25 V in FF corner.

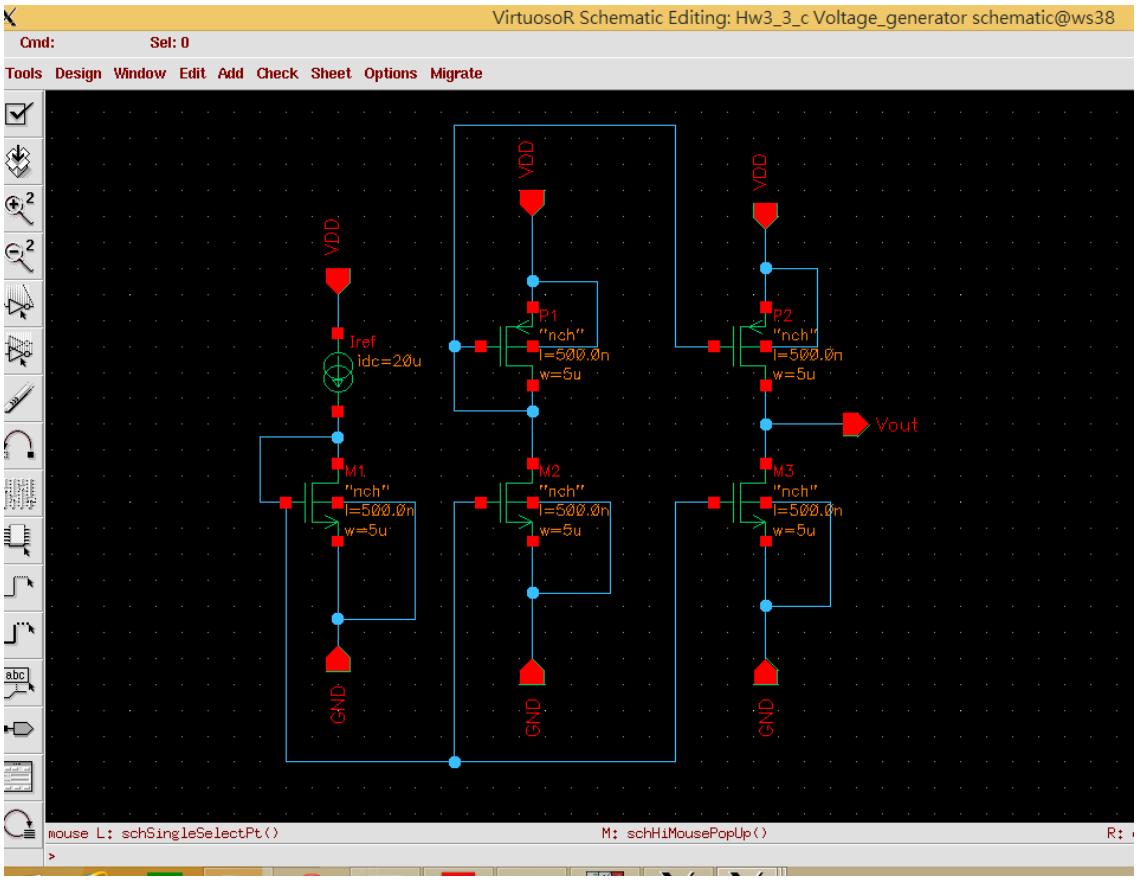
Comment：Using another current source to bias the original system in Fig. 2. (a) makes the system more stable without being interfered by process or corner

variations. In addition, we can find out that under the same conditions, the output impedance in FF corner > the one in TT corner > the one in SS corner.

(c) Since we manage to use another current source to replace V_b to make the systemmore stable, V_{GS_5} should be designed to be able to bias M_2 and M_4. On the other hand, M_6 should also be in the saturation region to make the system work fine. At last, we can also conclude that $V_{in1} = V_{TH} + 2V_{OV}$, $V_{in2} = V_{TH} + V_{OV}$, and $V_{out} = 2V_{OV}$.

3. Composer：





(a) Based on the .lis file, the sizes of PMOS and NMOS are 11 u / 2 u and 12.5 u / 3.05 u respectively with the bias voltage of PMOS = 1.207 V, causing the gain of the amplifier becomes 130.6901 in TT corner.

(b) In SF and FS corner, the devices enter the triode region, and therefore the gain drops extremely.

(c) The sizes of PMOS and NMOS remain the same as (a), while I_{REF} is designed to be 1.15 u, causing the gain in TT, SF & FS corner becomes 130.5436, 131.7857 and 130.0315 respectively, as shown below：

```
****      small-signal transfer characteristics

     v(vout)/v0                                =   130.5436
     input resistance at              v0       =   1.000e+20
     output resistance at v(vout)              =     4.5855x
```

The gain in TT corner

```
****     small-signal transfer characteristics

     v(vout)/v0                                =  131.7857
     input resistance at             v0        =  1.000e+20
     output resistance at v(vout)              =    4.7919x
```

The gain in SF corner

```
****     small-signal transfer characteristics

     v(vout)/v0                                =  130.0315
     input resistance at             v0        =  1.000e+20
     output resistance at v(vout)              =    4.5829x
```

The gain in FS corner

(d)The PMOS is directly biased by a voltage in Fig. 3. (a), and the process or corner variations will influence the bias condition, so the system will become less stable, and the devices may even enter the triode region. However, in Fig . 3. (b), the device is biased by a current source, leading to a current mirror and a voltage generator to send the stable signal to the output stage. Since the bias condition only depends on I_{REF} , the process variations may have few impact on the system.