2015 Analog IC Design Homework 3 ***due date: 04/30/2015***

1. Use composer and hsipce to simulate the differential pair as shown at Fig. 1 with Vdd=1.8V. (40%)
   (a) Design a differential pair with gain $A_{DM(\text{differential to differential})}$ >4.5 and $A_{CM(\text{in common – out common})}$<0.05 for both input common mode voltage = 0.6 and 1.8. (20%)
   (b) Simulate the frequency response of A_{DM} when input common mode voltage=0.9, and base on the simulation parameter of .lis file to calculate dominant pole. (10%)
   (c) Simulate the frequency response of A_{CM} when input common mode voltage=0.9, and identify what makes the A_{cm} deteriorate at the high frequency. (10%)

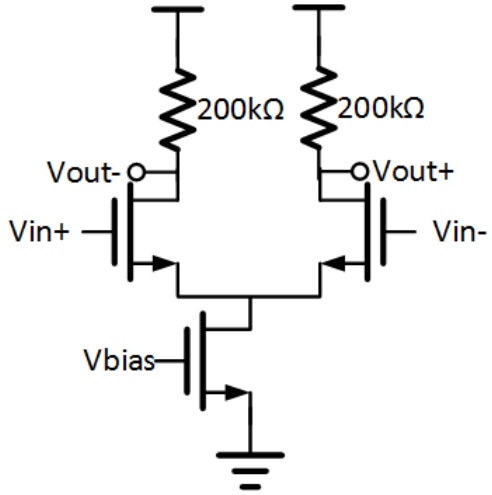

Fig. 1.

2. Design a 1:8 wide-swing cascade current source as shown in Fig. 2(a). (40%)
   (a) With I_{ref}=10uA (I_{our}=80uA), design the W/L sizes of M_1~M_4, and the dc bias V_b to get a minimum operational voltage at Vout<300mV and Rout>500kΩ. (15%)
   (b) Use the circuit structure as shown in Fig. 2(b) as a reference to design a bias generation circuit of Vb with I_{in}=10uA(I_{out}=80uA). Run the corner simulations with SS, TT, and FF to make sure Voutmin<300mV and comment the difference with using ideal voltage source as the bias in Fig. 2(a) (15%)
   (c) State the M5's and M6's (Fig. 2. (b)) design strategy and show in hand calculation. And express Vin1, Vin2, and Vout in terms of Vov and Vth. (10%)

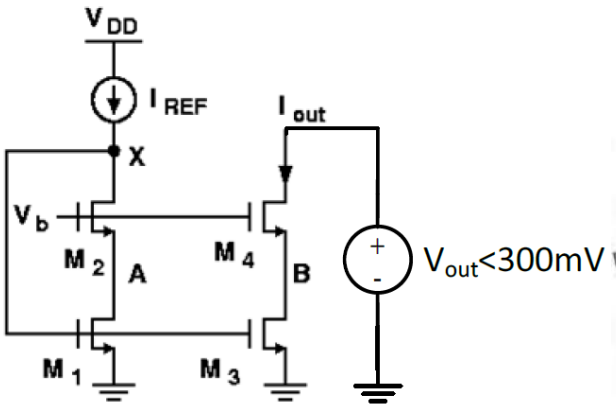

Fig. 2.(a)

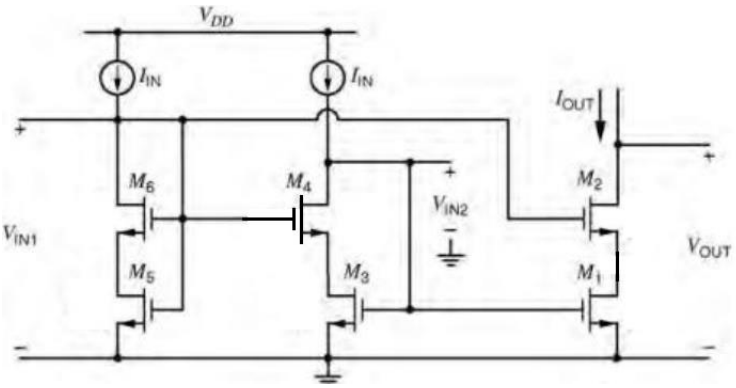

Fig. 2.(b)

by CCHsieh

3. Design a common-source amplifier with Vdd=1.8V as shown in Fig. 3. (20%)
   (a) Design the W/L sizes and Vb as shown in Fig. 3.(a) to get voltage gain Av=Vout/Vin>130. (5%)
   (b) Keep everything the same and simulate the gain under the SF and FS corner.
   (c) Design the W/L sizes and Iref as shown in Fig. 3.(b) to get voltage gain Av=Vout/Vin>130 for TT, SF, and FS corner. (5%)
   (d) Comment on the differences between (b) and (c). (10%)

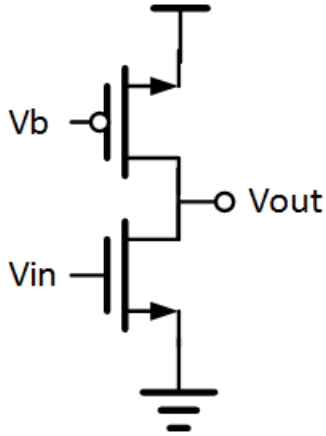

Fig. 3. (a)

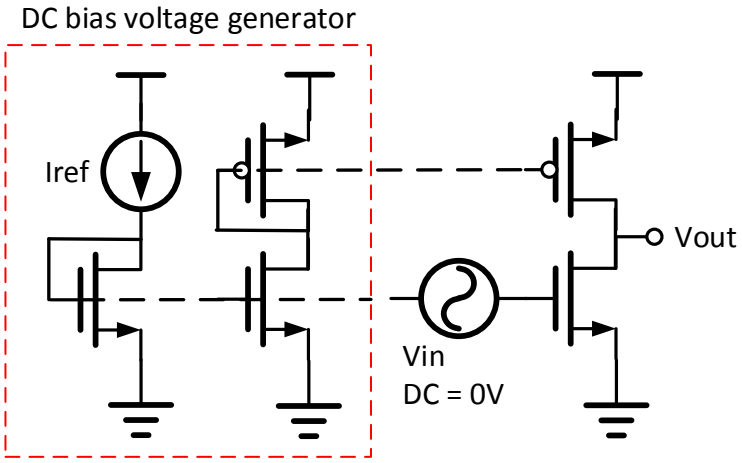

Fig. 3. (b)

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***