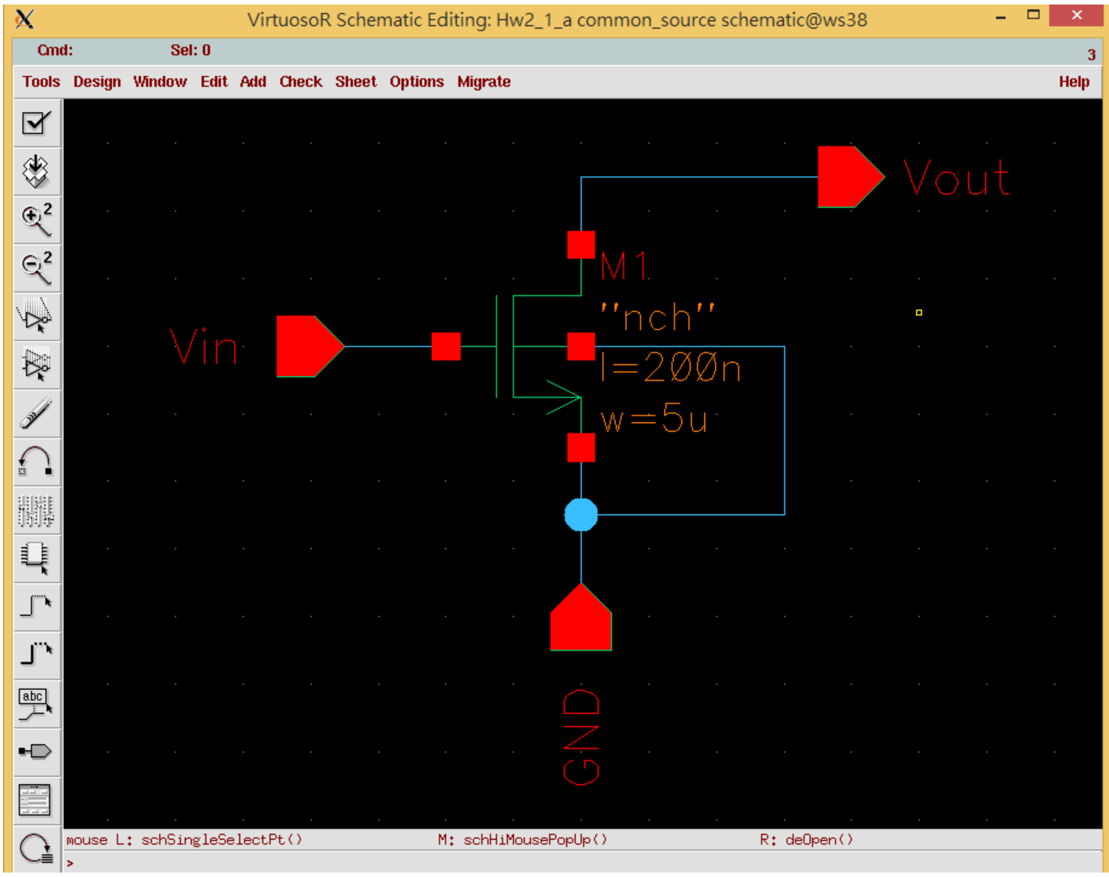
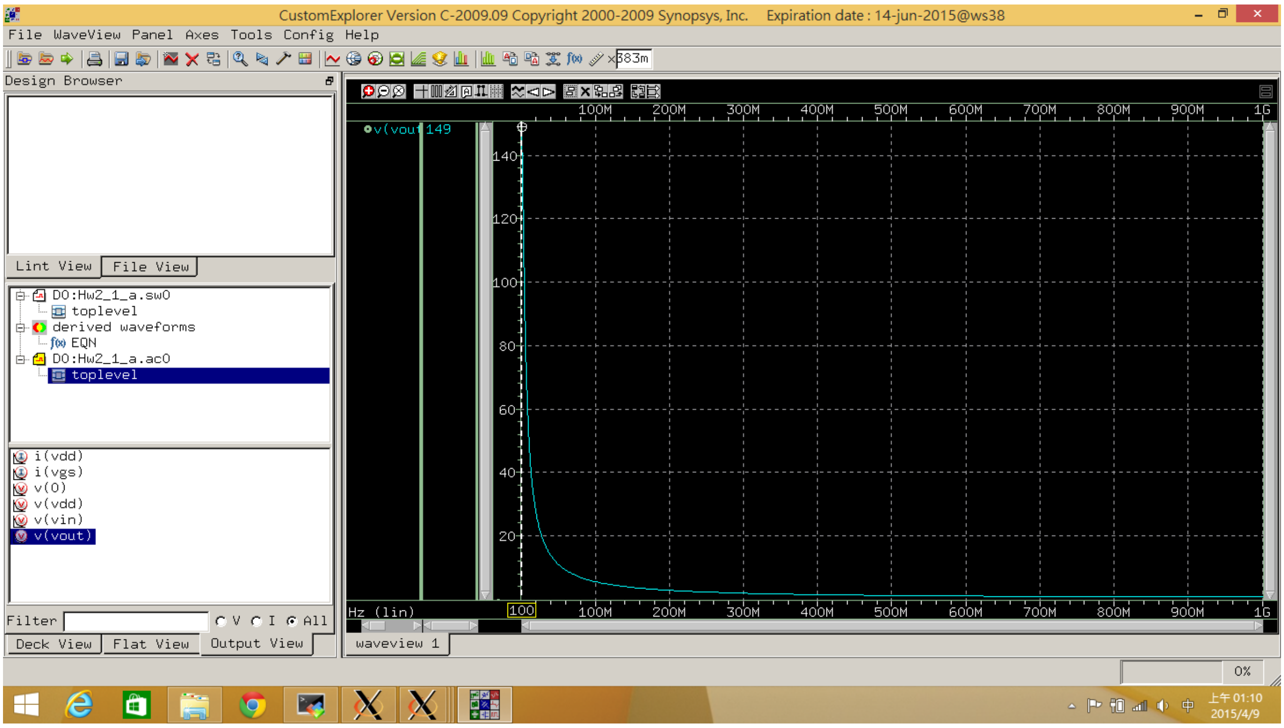
Analog IC Design & Analysis Homework 2 陳彥廷 102061146

1.(a) Composer：



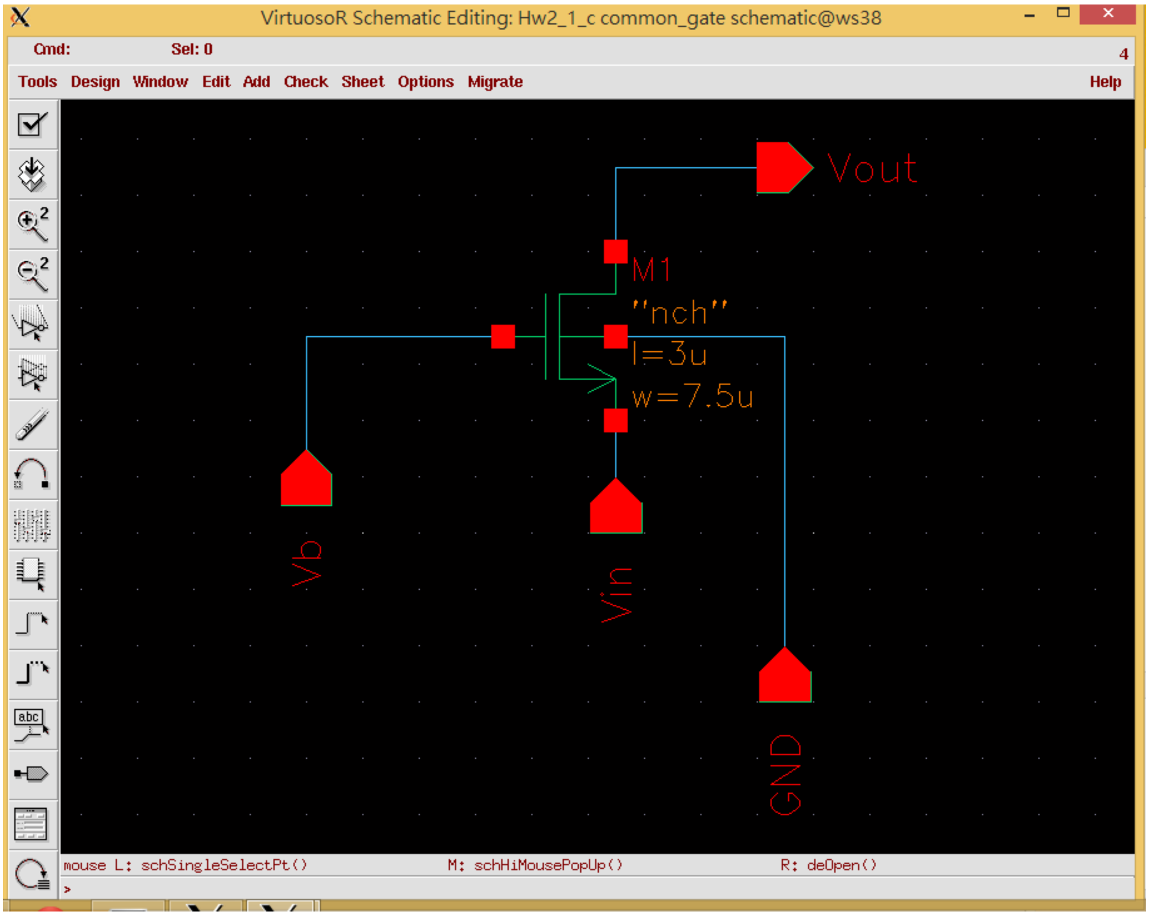
Waveform：



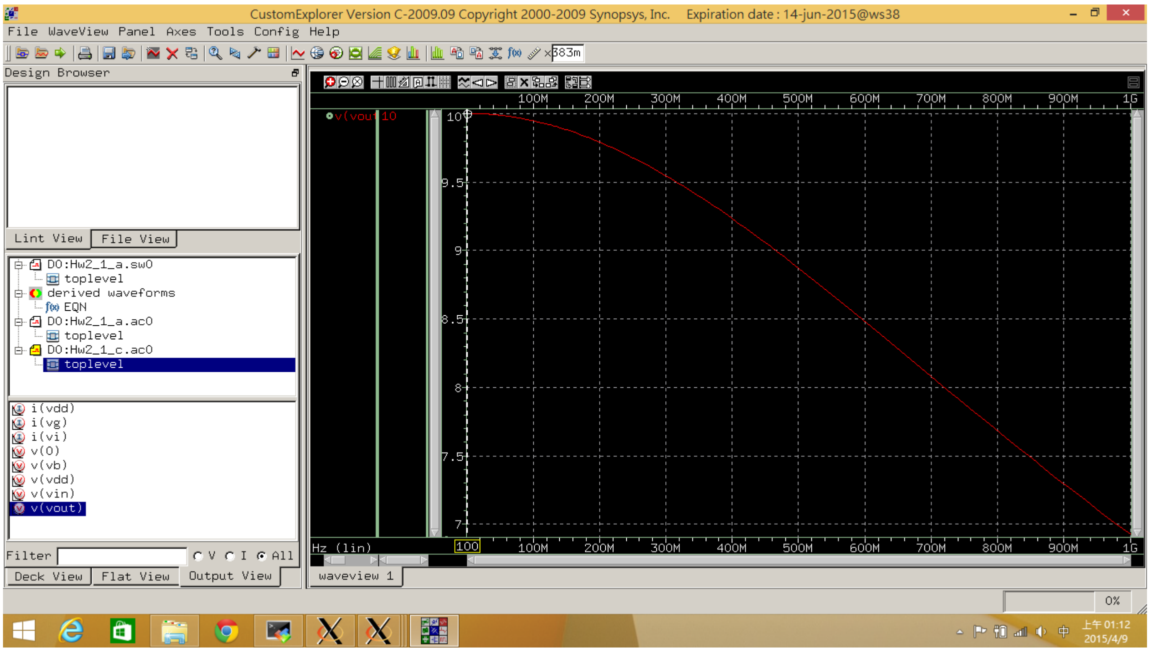
Therefore, based on the .lis file, the AC gain is about -149, and the output DC voltage is about 0.498 V with the input DC voltage designed with the value of about 0.387 V.

(b)Based on the .lis file and we know that the AC gain of the common source stage equals $g_m * r_o$, we can calculate the gain = g_m/g_{ds} indicated in the file, which equals 36.1793 u / 242.4679 n~ -149.2127. In order to make the gain higher, we can raise W/L first, particularly Lsince $r_o \propto L^2$. After L becomes higher, we should raise W as well to keep high gain. In addition, adjust Vin to keep the stage in saturation region andtry to raise g_m, but avoid lowering r_o.

(c) Composer：



Waveform：

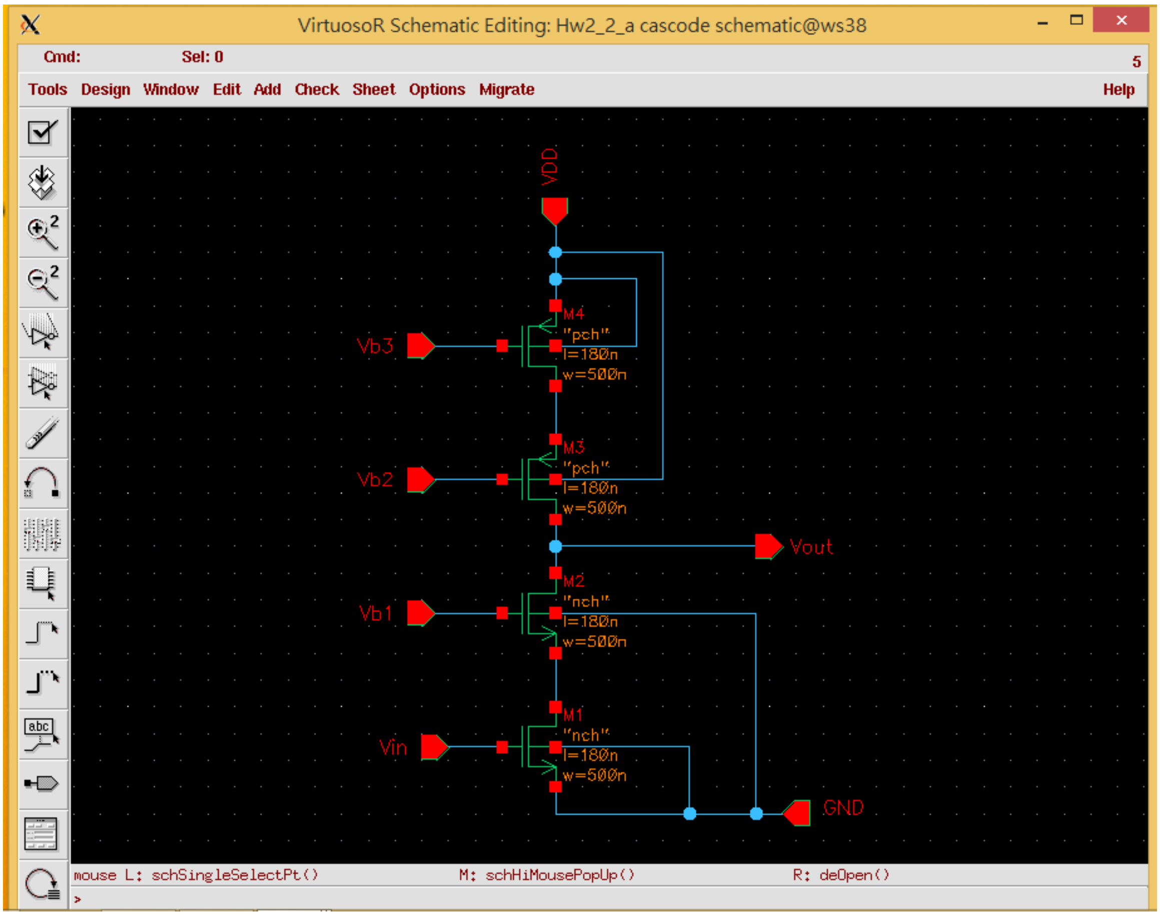


This common-gate stage is designed with the input DC voltage 0.5 V, bias current about 40.4 u, and bias voltage about 1.1346 V.

(d)The AC gain of the common-gate stage equals $g_m*(R_D//r_o)/(1+g_m*R_S)$, so, based on the .lis file, the AC gain is about 10.0032.

(e)A1*A2 is about -1490, but the gain of the connected stage is only about -56.0765. This phenomenon is due to the output impedance of the first stage, which is r_o of the common-source stage, causing the source degeneration of the second stage. In addition, r_o of the first stage is large enough to make the effect of source degeneration of the second stage very obvious. Therefore, the real gain of two connected stages is quite smaller than the multiplication of the first stage and the second one.

2. (a) Composer：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Sel: 0
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VDD
Vb3
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"pch"
l=180n
w=500n
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l=180n
w=500n
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Vb1
M2
"nch"
l=180n
w=500n
Vin
M1
"nch"
l=180n
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mouse L: schSingleSelectPt()
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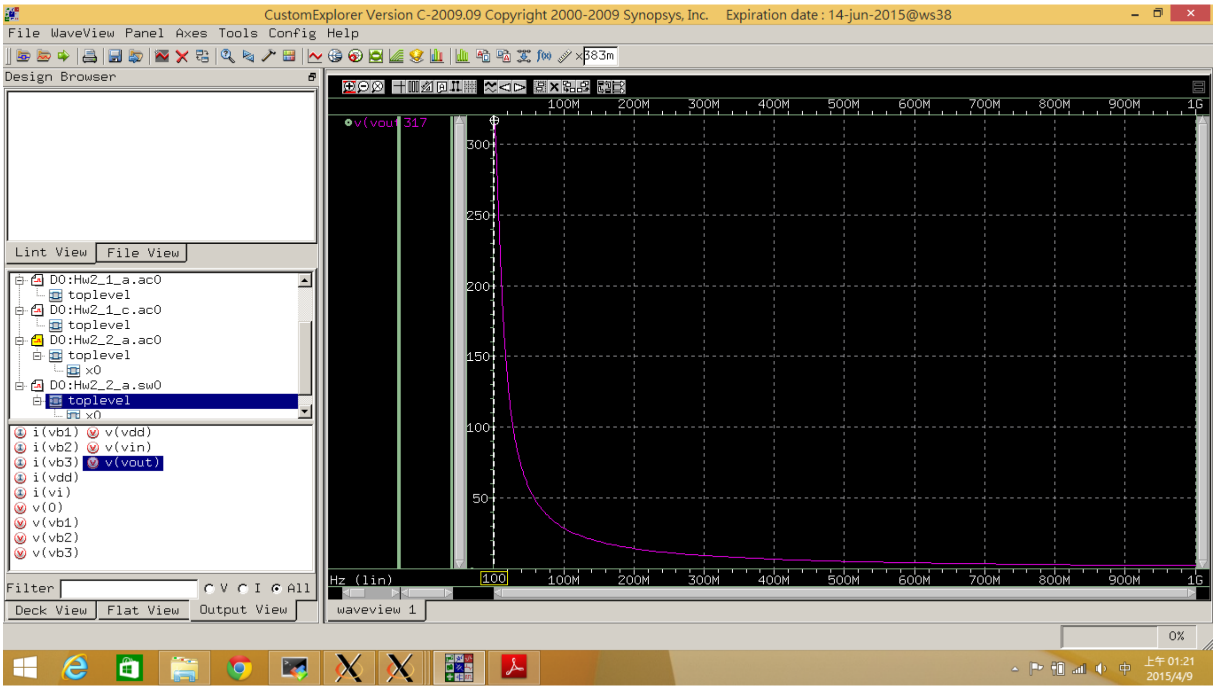
Waveform：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Hz (lin)
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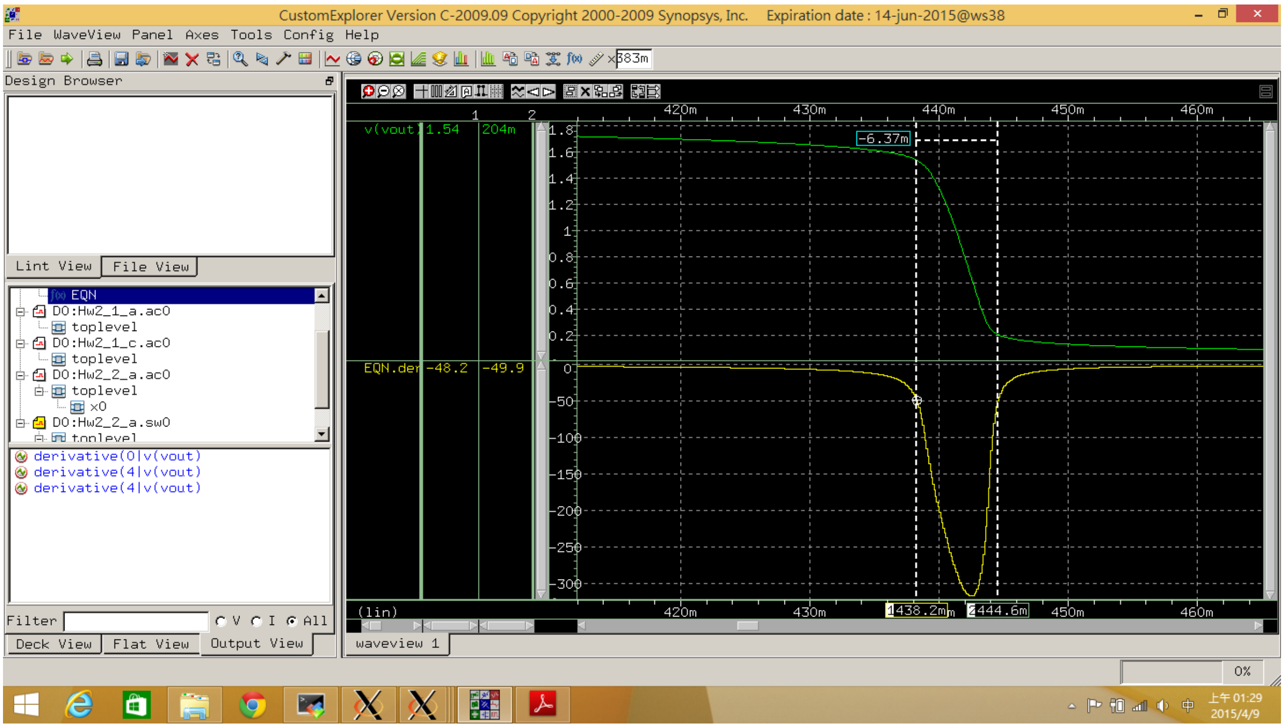
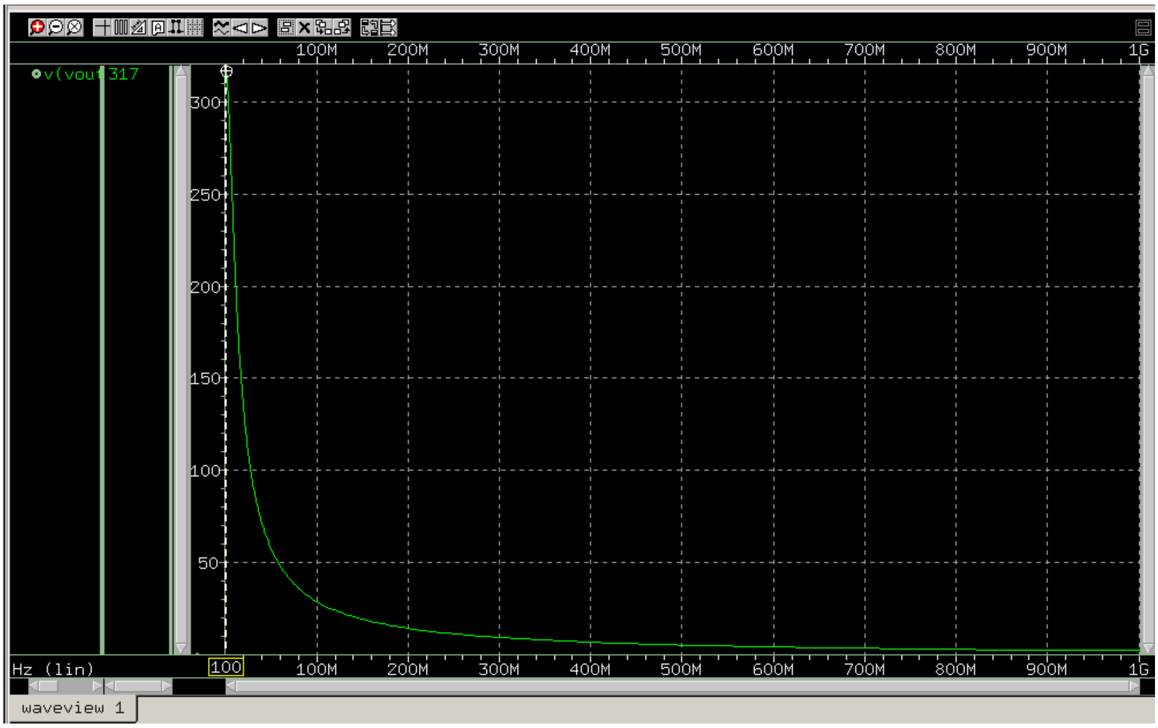
waveview 1

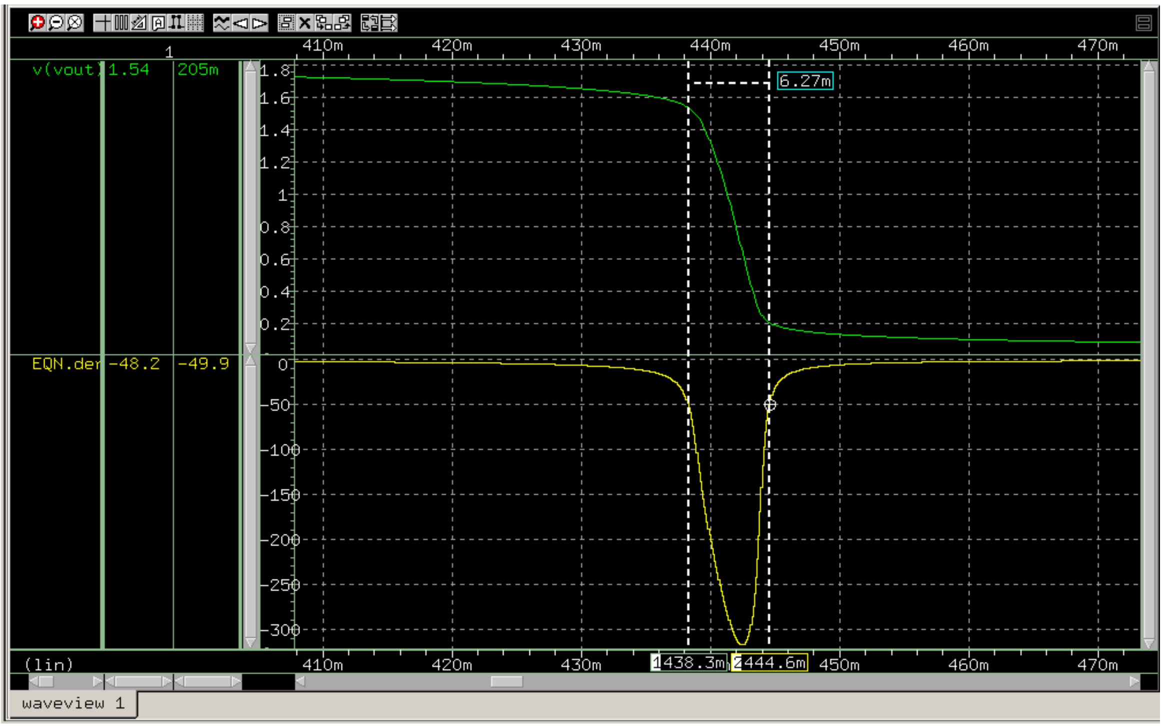


The four bias voltage from M1 to M4 are respectively 442.3 mV, 627.5 mV, 1.041 V, and 1.195 V, while the bias current is about 22.3733 u, causing the gain of about 50.03 dB.

(b)Composer：

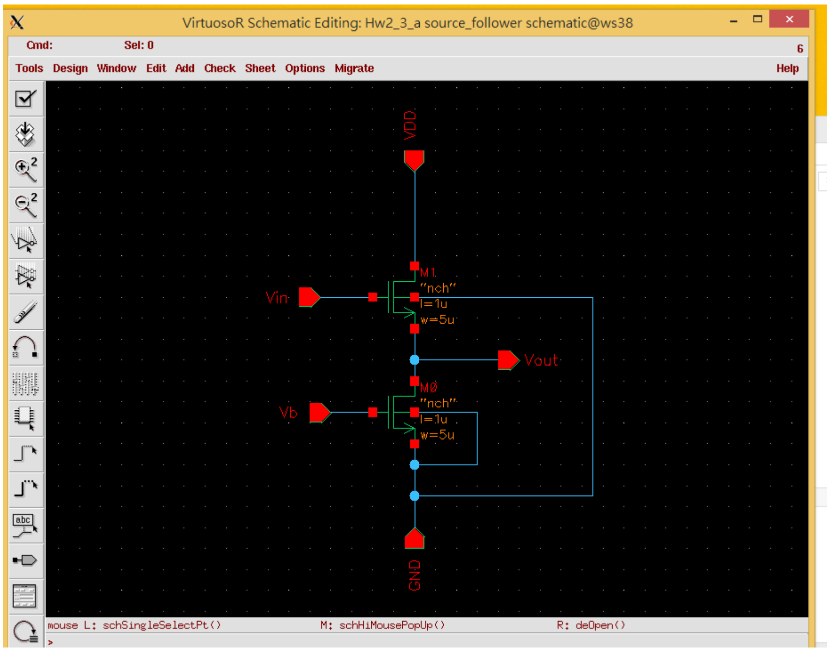


Waveform：

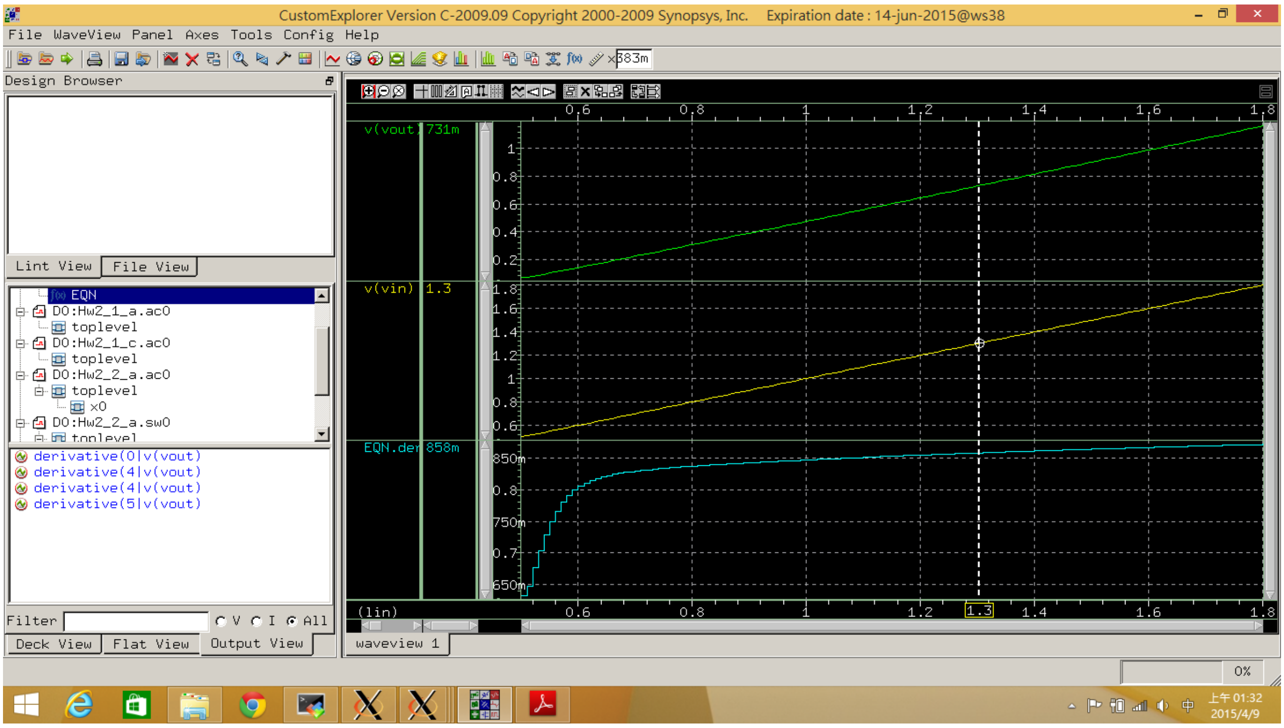


The bias current and the trans-conductance become two times larger than the origin, while r_o becomes half of the origin. When m = 2, W becomes twice longer, and therefore the bias current becomes twice larger. Since $r_o = \frac{1}{\lambda * I_D}$, r_o becomes half smaller, as mentioned above. Given that the gain is about $-g_{m1}[(g_{m2}r_{o2}r_{o1})//(g_{m3}r_{o3}r_{o4})]$, we can know that actually the gain keeps the same as (a). In addition, the output swing is almost the same as the origin.

3. (a) Composer：

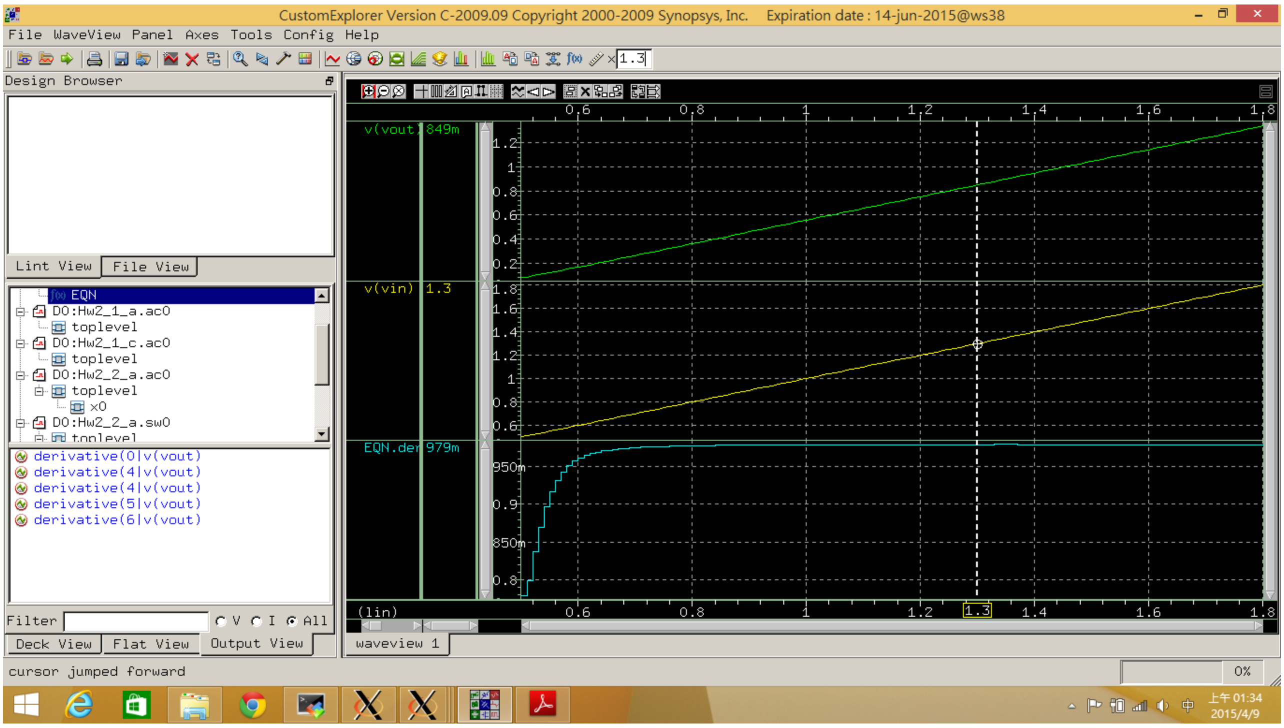


Waveform：



The source follower is designed with the bias voltage 0.45 V and the size W/ L = 5 u / 1.2 u and 5 u / 1 u for M1 and M2 respectively. At last, the gain becomesabout 0.858.

(b) Waveform：



All the bias conditions are the same as (a), as well as the size of the devices.

After adding deep n-well, the gain becomes about 0.979.

(c)Given that the gain of (a) equals $\frac{\frac{1}{g_{mb}}//r_{o1}//r_{o2}}{\frac{1}{g_{mb}}//r_{o1}//r_{o2}+\frac{1}{g_{m1}}}$ and the gain of (b) becomes $\frac{r_{o1}//r_{o2}}{r_{o1}//r_{o2}+\frac{1}{g_{m1}}}$ and we also know that $\frac{1}{g_m}$ is usually small, we can conclude that the stage with deep n-well devices will have larger gain since there is no body effect.