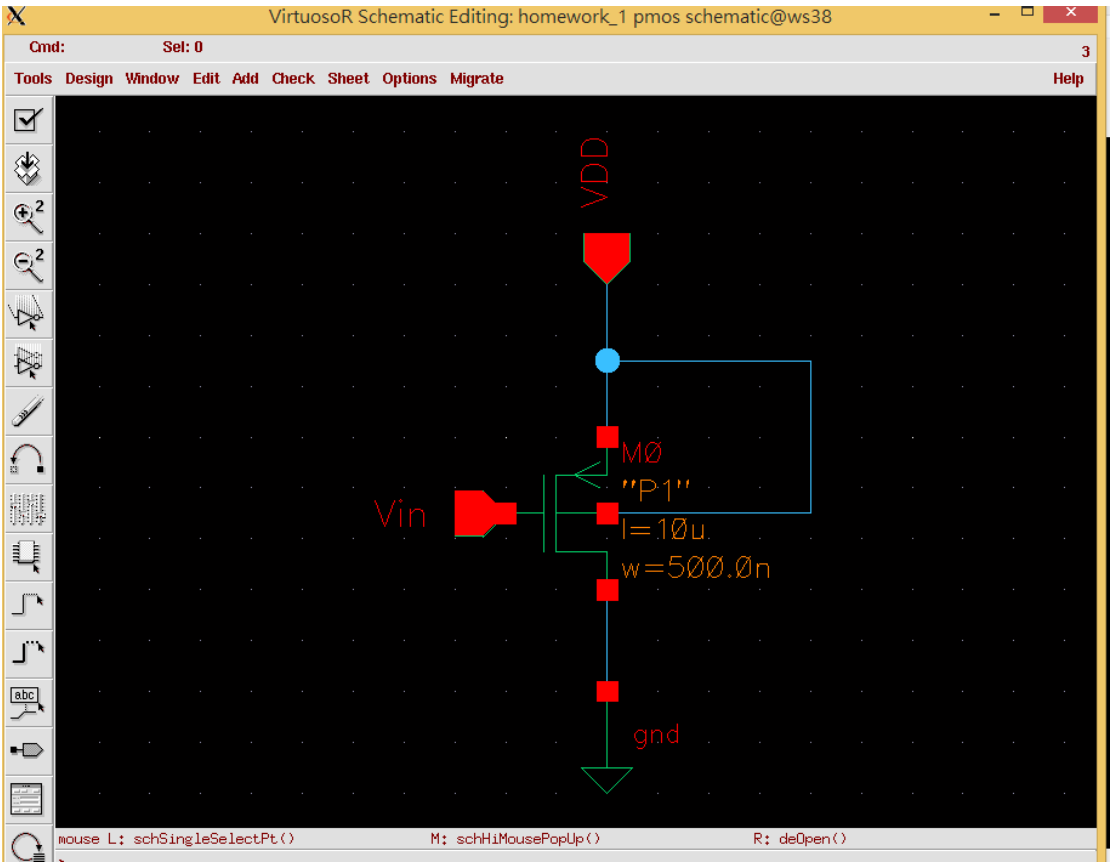
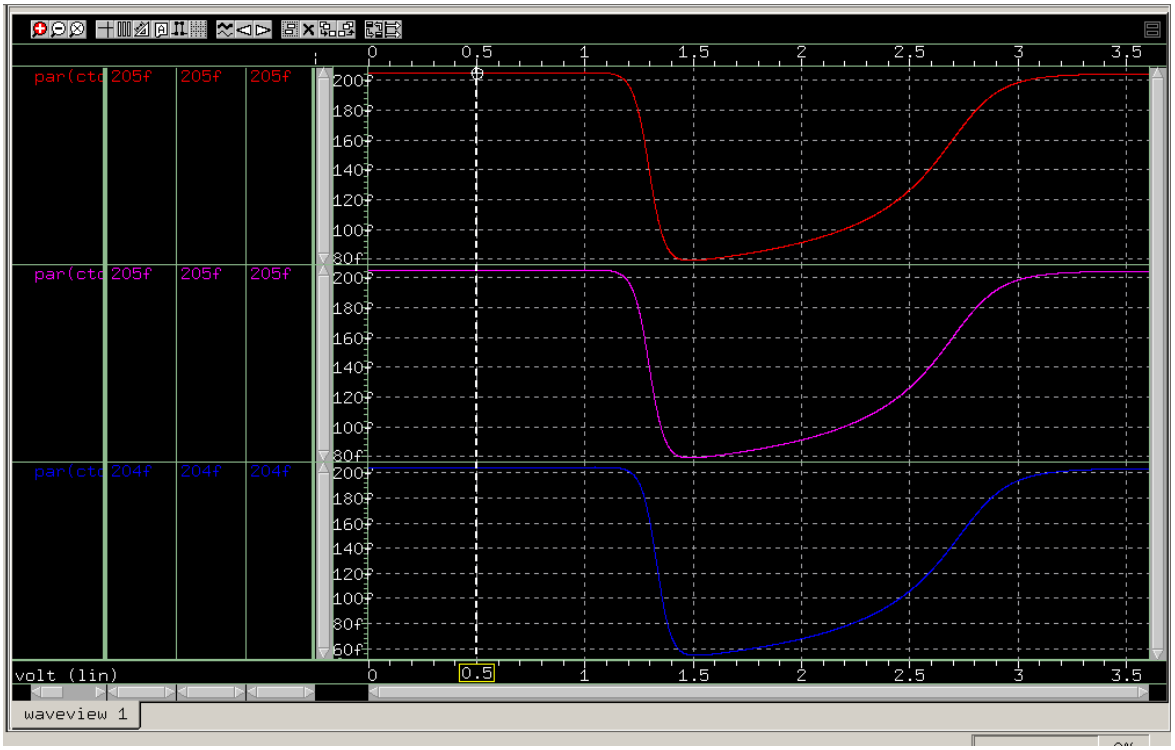
Analog IC Design & Analysis Homework 1 陳彥廷 102061146

1.Composer：



Waveform：



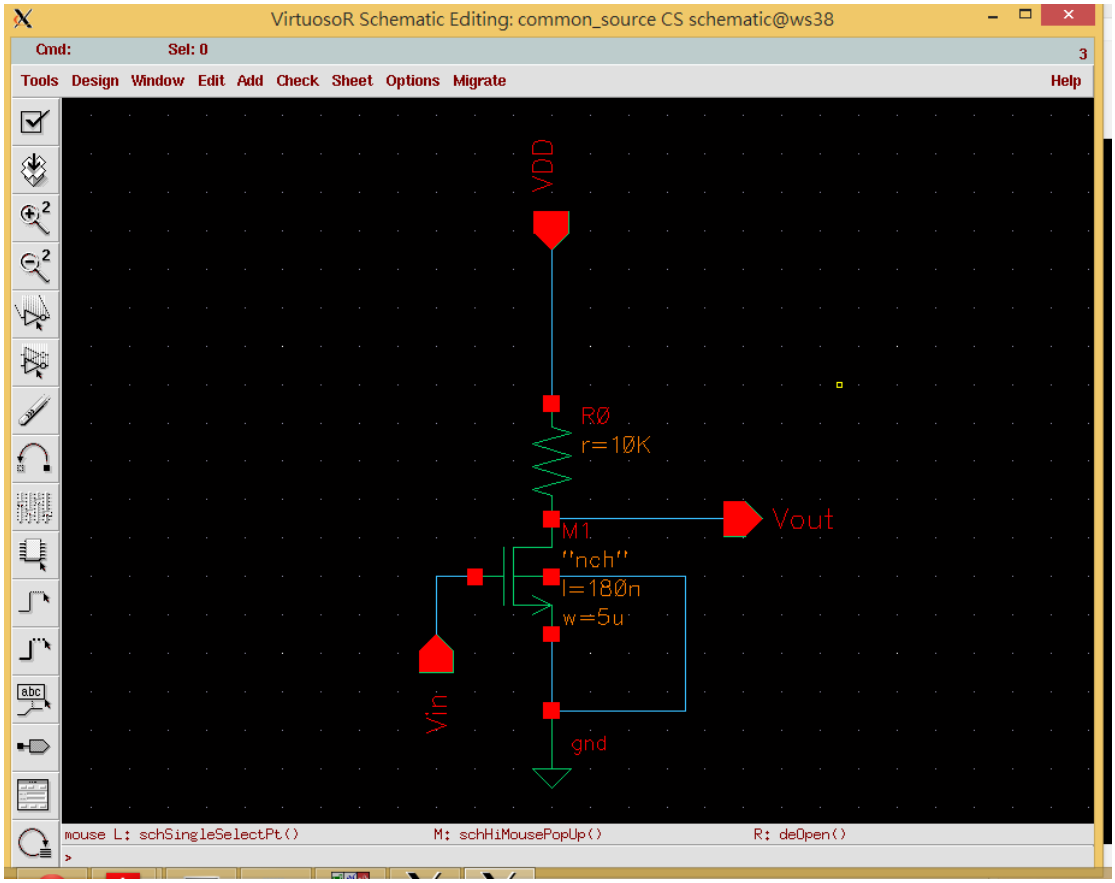
Comments：

(a) The capacitance is about 205 fF.

(b) The capacitance is still 205 fF since it's proportional to W*L, and the value of W*L is the same as (a); that is, 25 (um)^2.

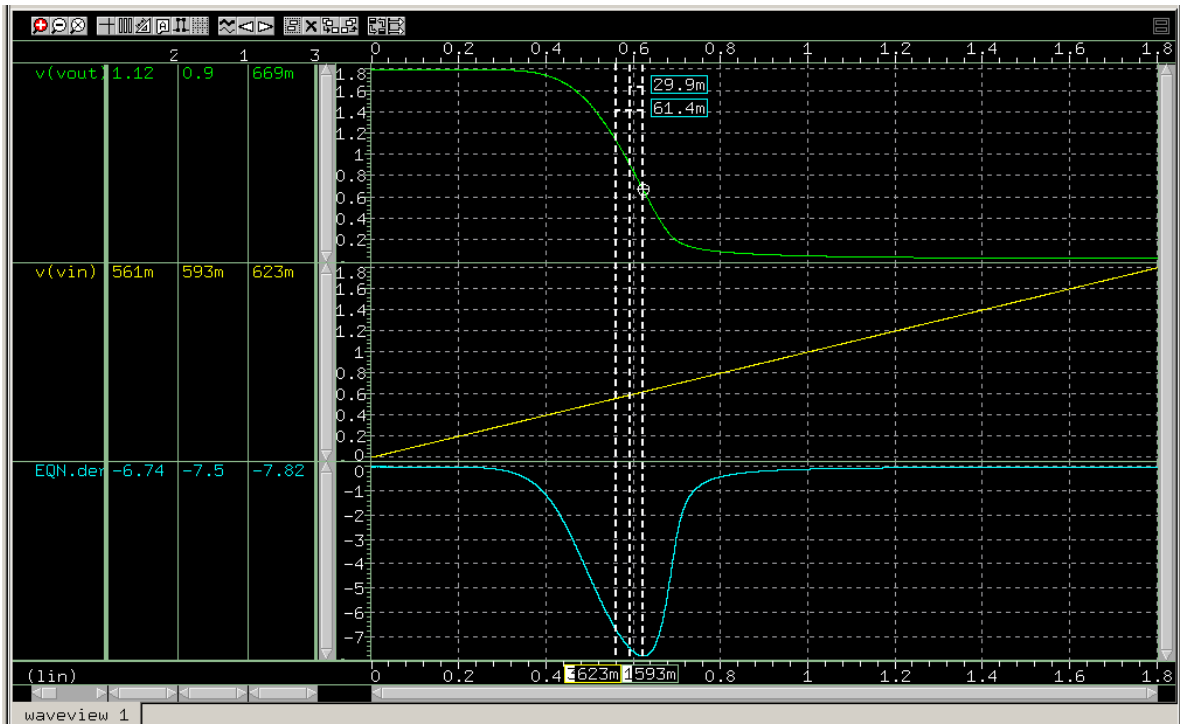
(c) With same W*L, the capacitance still approaches to 205fF, but with 1 fF difference due to the folded structure and the channel-stop implant.

2. Composer：

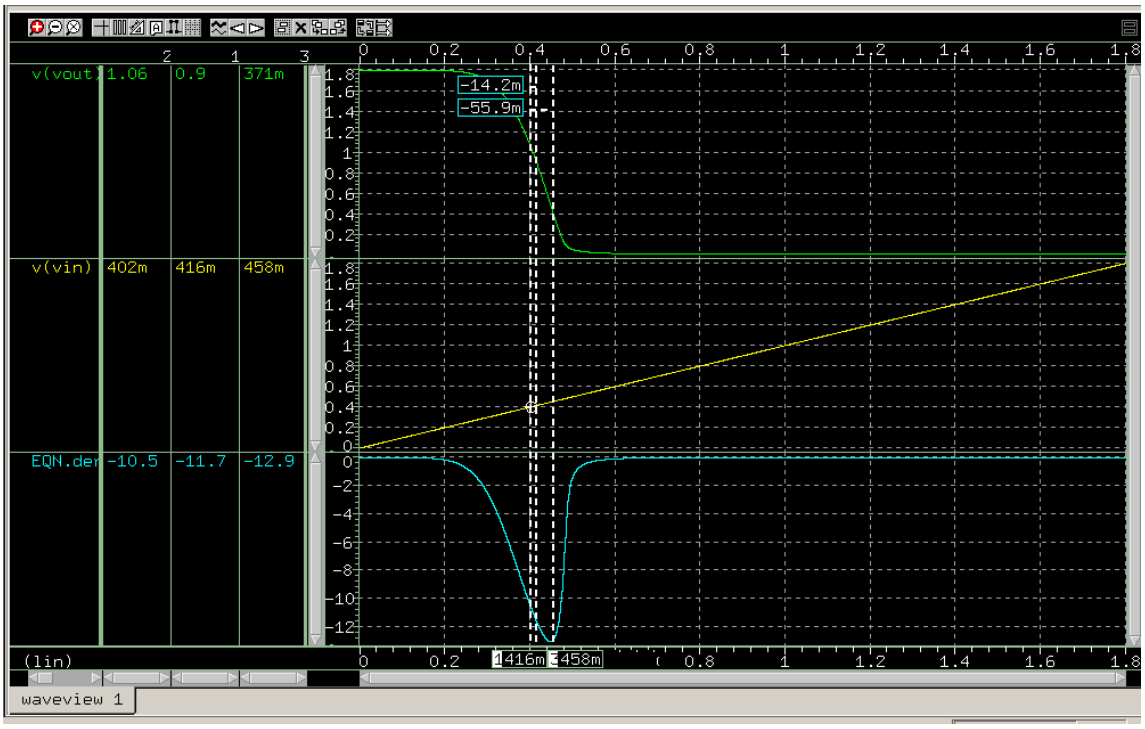


Waveform：

(a) &(b)



(c)



Comments：

(a) The DC input voltage is about 0.593V, and W=5 μ, L=0.18 μ, M=1.

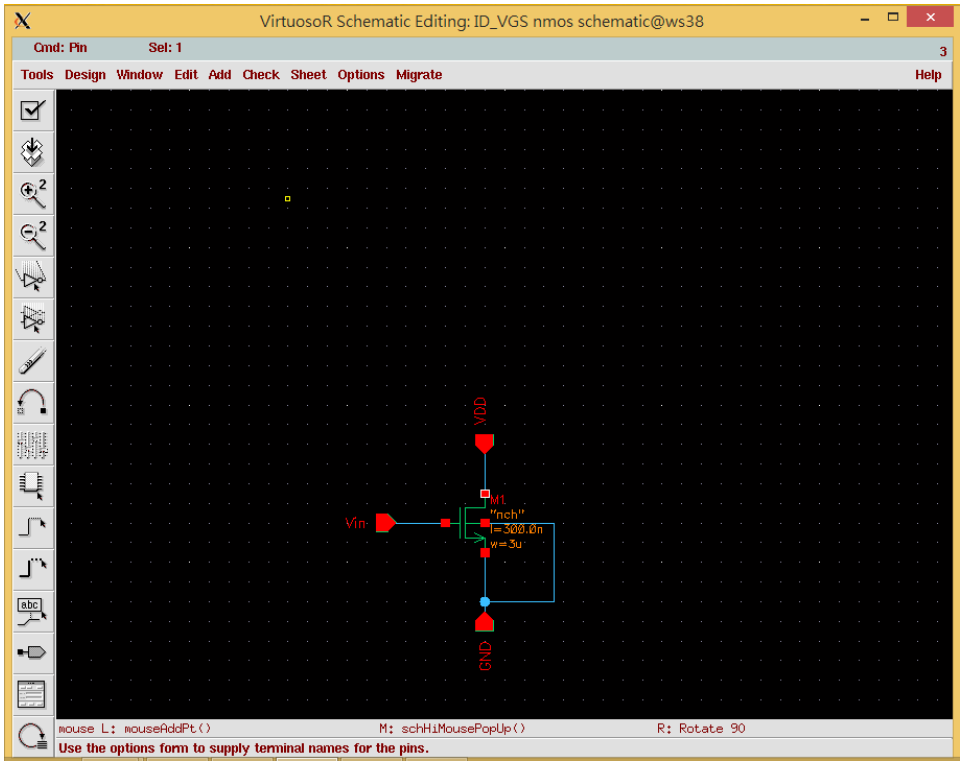
(b) Output range is from 1.12V to 0.669V with input range from 0.561V to

0.623V while the largest gain is only 7.82, whose difference from the gain derived in (a) is less than 10% of it.

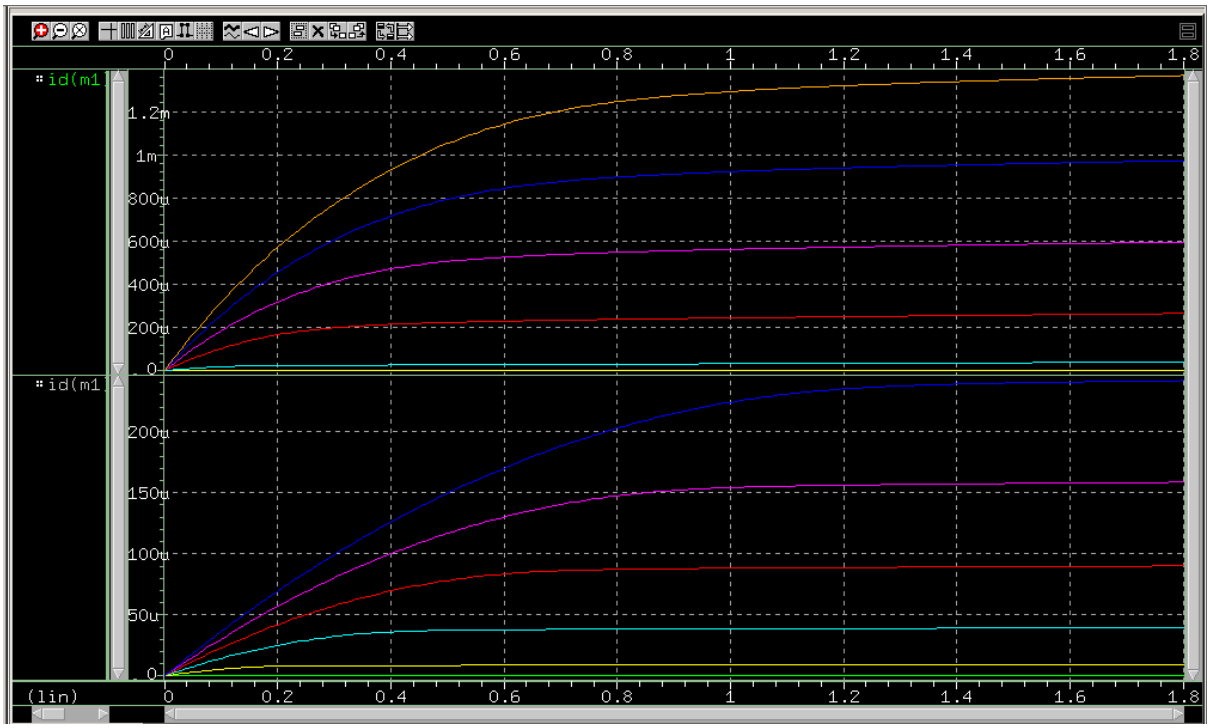
(c) In this situation, output range becomes from 1.06V to 0.371V with input range from 0.402V to 0.458V.

(d) If the amount of the nmos connected in parallel increases, then W becomes 20 times longer than the original one, so the gain will become larger. In addition, since the output voltage and VDD are fixed, the drain current is also fixed. Therefore, $(V_{GS} - V_{TH})^2$ must become smaller, causing the smaller gate voltage; that is, the input voltage.

3. Composer：



Waveform：



Comments：

1. For the same size of nmos, if VGS increases, then the actual length of the inverted channel decreases, causing the Channel-Length Modulation Effect. Therefore, VGS will actually depend on ID even though the nmos is in the saturation region.
2. Based on the formula, $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$, and $\lambda \alpha \frac{1}{L}$.

   Therefore, the device with shorter channel length will have higher drain current.
3. Since $I_D \alpha (V_{GS}-V_{TH})^2$, larger V_{GS} will lead to larger drain current with the fixed channel length.