

1. Use composer and hspice to simulate the capacitance characteristic of pMOS as shown in Fig. 1 with body connected to vdd=1.8V. (30%) (*hint*: .probe DC ctot=par("lx18(MN)"))
 - (a) Assume the $W/L = 5*10\mu\text{m}/0.5\mu\text{m}$, $V_G = 0\text{V} \sim 3.6\text{V}$. (use CIC 0.18um hspice model). (10%)
 - (b) Modify the $W/L = 50\mu\text{m}/0.5\mu\text{m}$, redo the simulation and plot, comments the capacitance difference compared to (a). (10%)
 - (c) Modify the $W/L = 5\mu\text{m}/5\mu\text{m}$, redo the simulation and plot, comments the capacitance difference compared to (a) and (b). (10%)

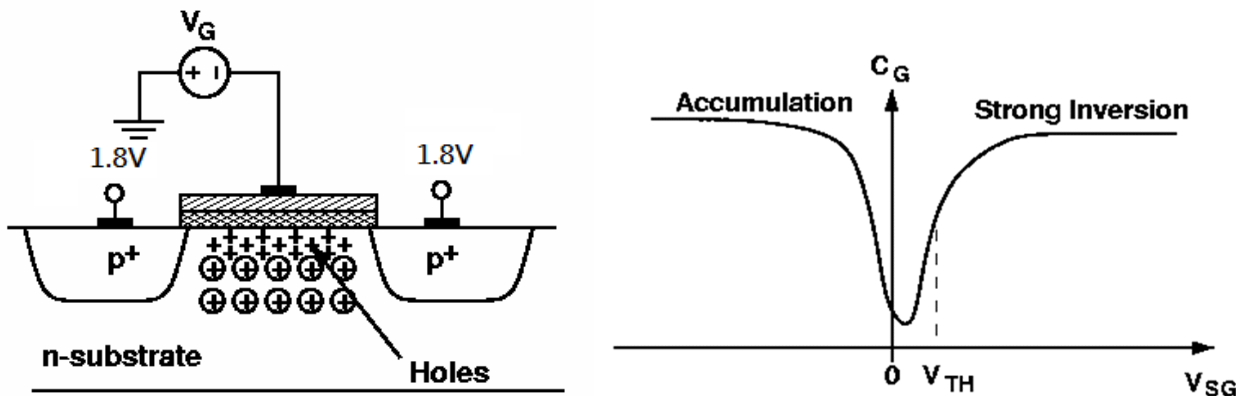


Fig. 1.

2. A common source as shown in Fig. 2 has $V_{DD} = 1.8\text{V}$, Output DC voltage= 0.9V , and $R=10\text{k}\Omega$. (50%)
 - (a) Choose the size ($m=1$) and the input DC voltage of M_1 . Use function “.tf v(out) vin” to find the AC gain >5 . (5%)
 - (b) Find the linear range (1. Definition: 10% gain deviation. 2. Range of both input and output) and gain of this common source with voltage transfer curve V_{in} vs. V_{out} only. (10%)
 - (c) Use the same width and length with $m=20$ to find input DC voltage again. And redo the (b). (15%)
 - (d) Comment on what makes the difference of gain and linear range between (b) and (c). (20%)

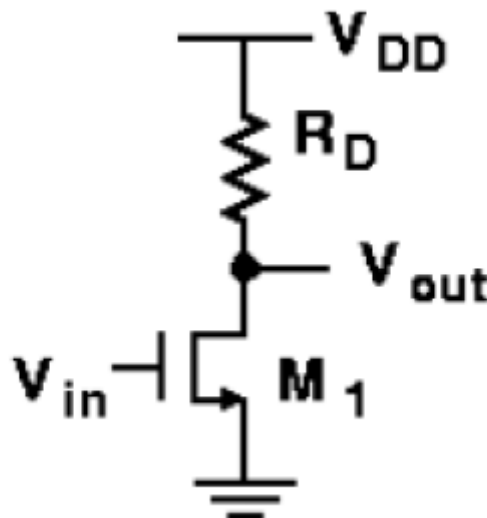


Fig. 2.

3. Choose two nMOSs (1.8V devices) with $W/L = 3\mu\text{m}/0.3\mu\text{m}$ and $W/L = 3\mu\text{m}/3\mu\text{m}$. Use HSPICE DC sweep analysis to show the I_D - V_{DS} characteristic waveforms with $V_{GS} = 0, 0.3, 0.6, 0.9, 1.2, 1.5$ and 1.8V as shown in Fig. 3. Comment the characteristics difference between long-channel and short-channel devices. (20%)

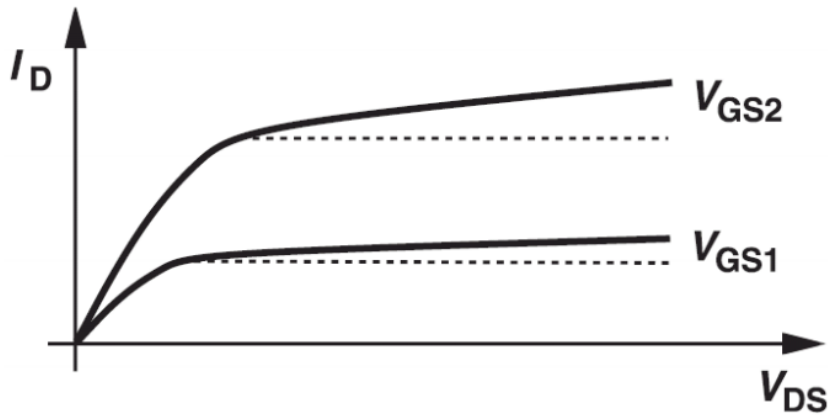


Fig. 3.

- ✧ *The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.*