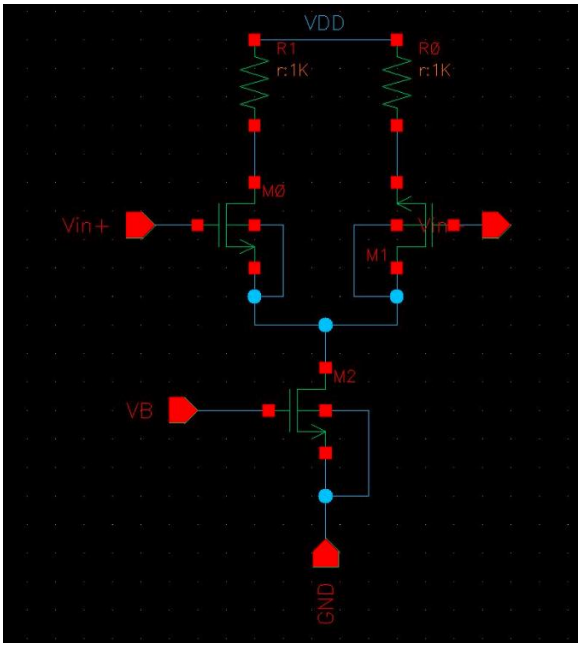
Analog IC Design Homework 3

學號: 102061112

姓名: 謝博楊

1.

Schematic:



(a) To find a proper V_b to let the drain current of M_3=20uA, I connect M_3 with a 20uA current source, and V_b=V_{GS}.

from .lis file:

```
element   0:m3
model     0:n_18.1
region      Saturati
 id         20.0000u
 ibs      -3.236e-21
 ibd      -380.8417a
 vgs       489.5179m
 vds       489.5179m
```

V_b=V_{GS} is about 489.5mV, I choose 0.49

$|A_v|$ = g_m*(r_o//R_D), so if we want to raise the gain, we expect

(1) g_m to be larger, which means larger W

(2) r_o to be larger, which means larger L, but r_o//R_D, so the impact of L is narrowed. Thus, W is my trial priority.

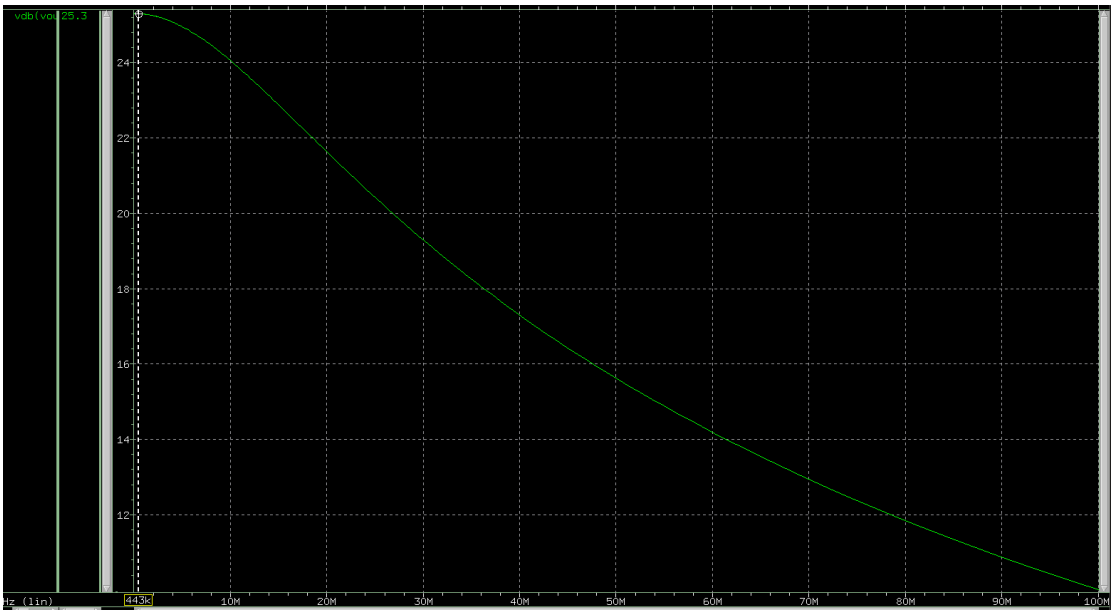
(3) R_D to be larger, which R_D = 100k.

And my design is $(W/L)_{M1}$ = $(W/L)_{M2}$ = 84u /2.8u.

from .lis file:

```
element   0:m3        0:m2        0:m1
model     0:n_18.1    0:n_18.1    0:n_18.1
region      Saturati    Saturati    Saturati
 id         20.0557u    10.0278u    10.0278u
```

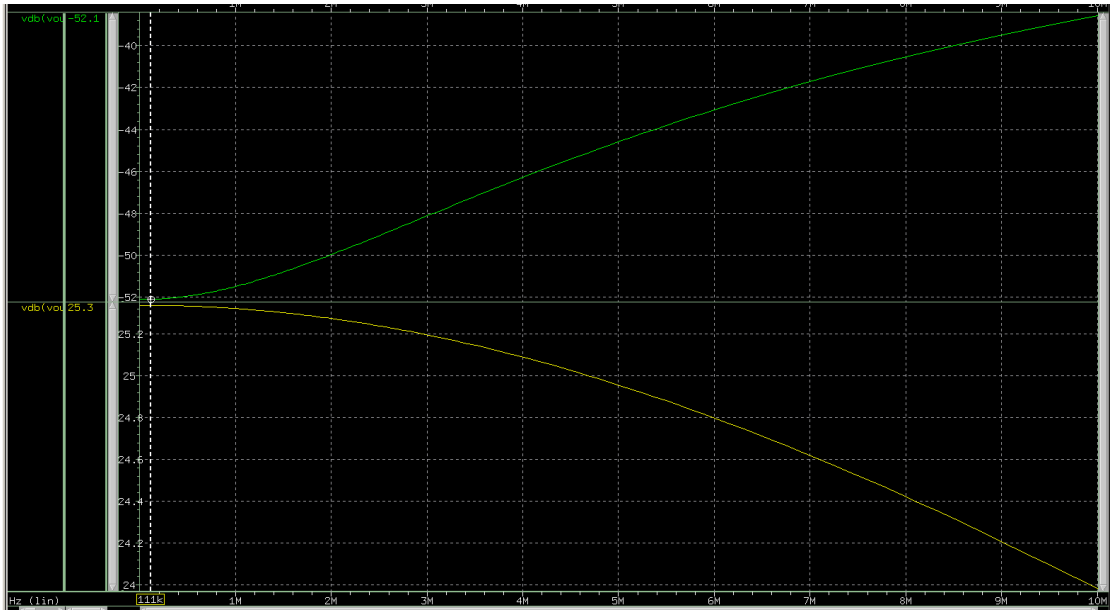
The voltage gain= 25.3dB > 20dB:



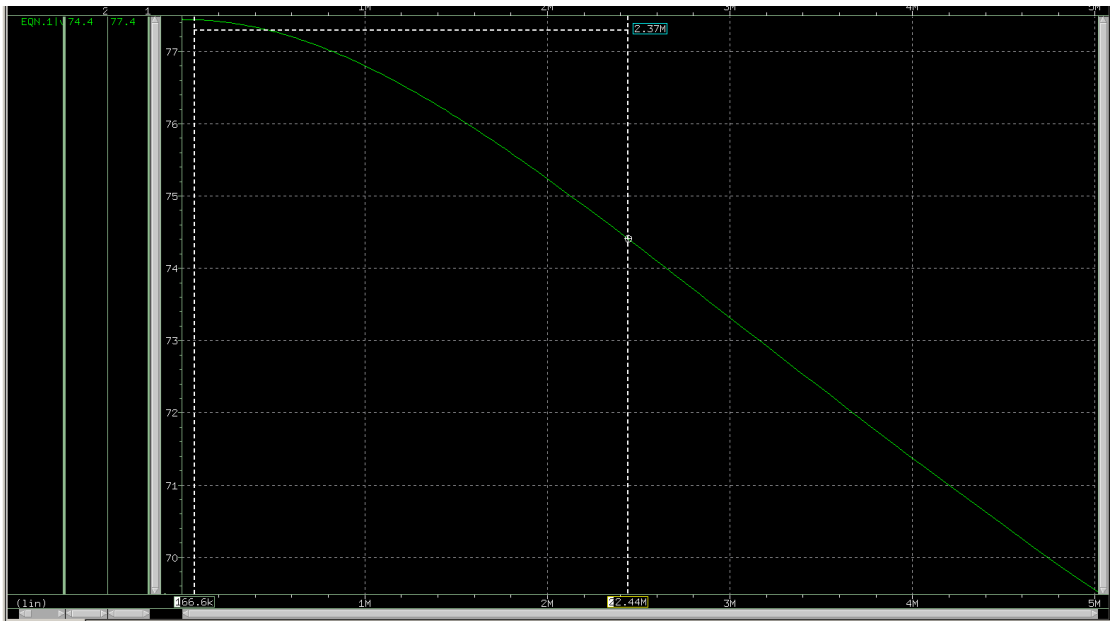
(b) $(W/L)_{M2}$ becomes 92.4u/2u.

(i) Without C_p:

$|A_v|$ = 25.3dB, $|A_{cm}|$ = 52.1dB



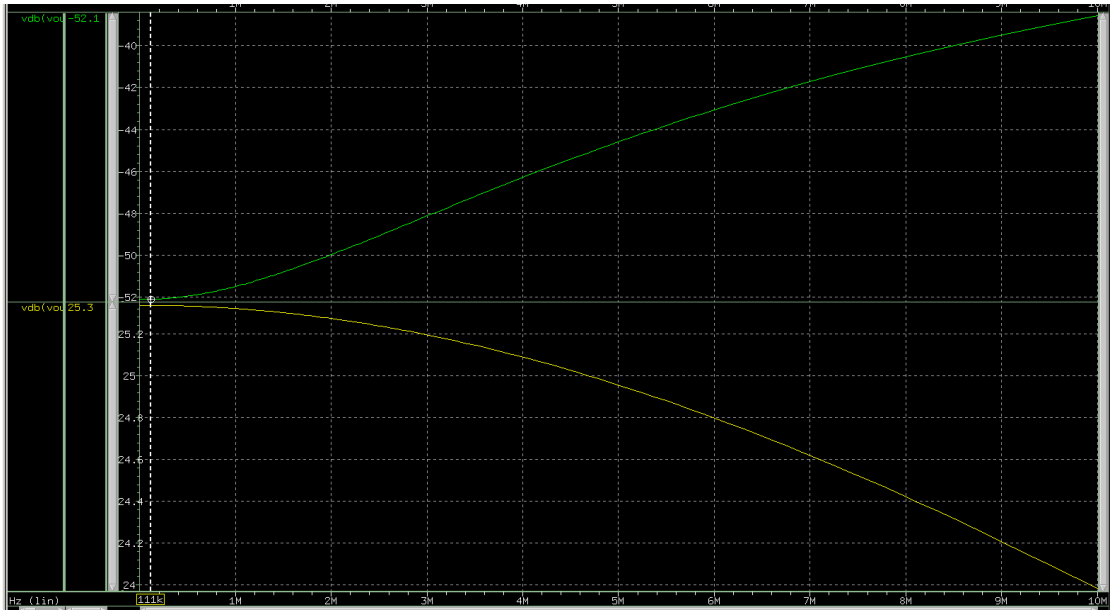
At low freq. CMRR = $|A_v \ / \ A_{cm}|$ = 25.3dB - (-52.1dB) = 77.4dB



from the figure, -3dB bandwidth without C_p = 2.44M.

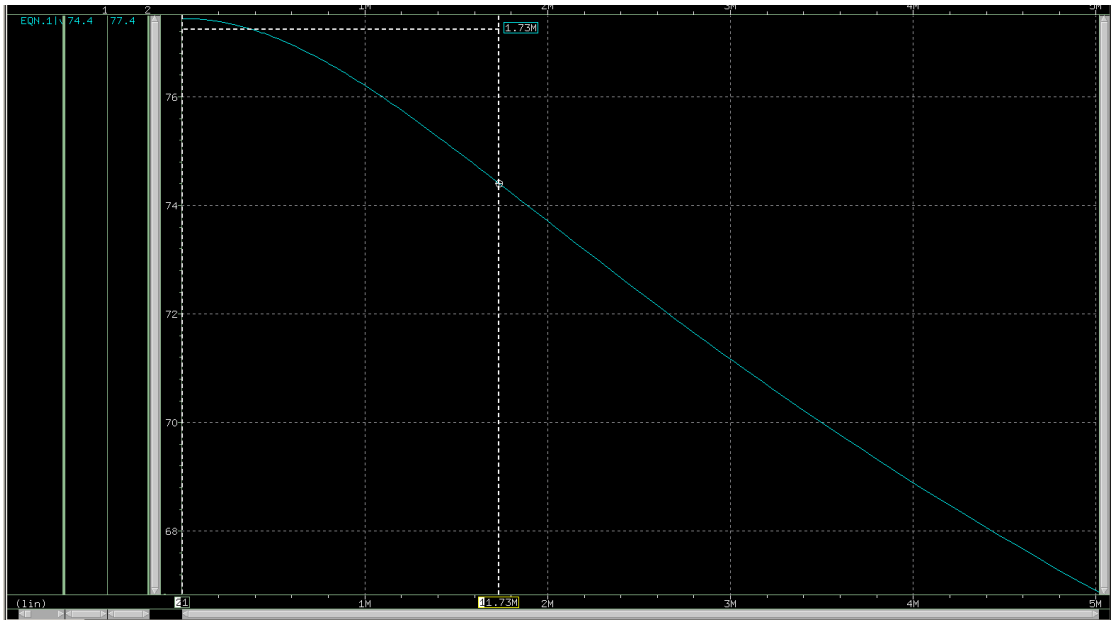
(ii) With C_p from P to ground:

$|A_v|$ = 25.3dB, $|A_{cm}|$ = 52.1dB

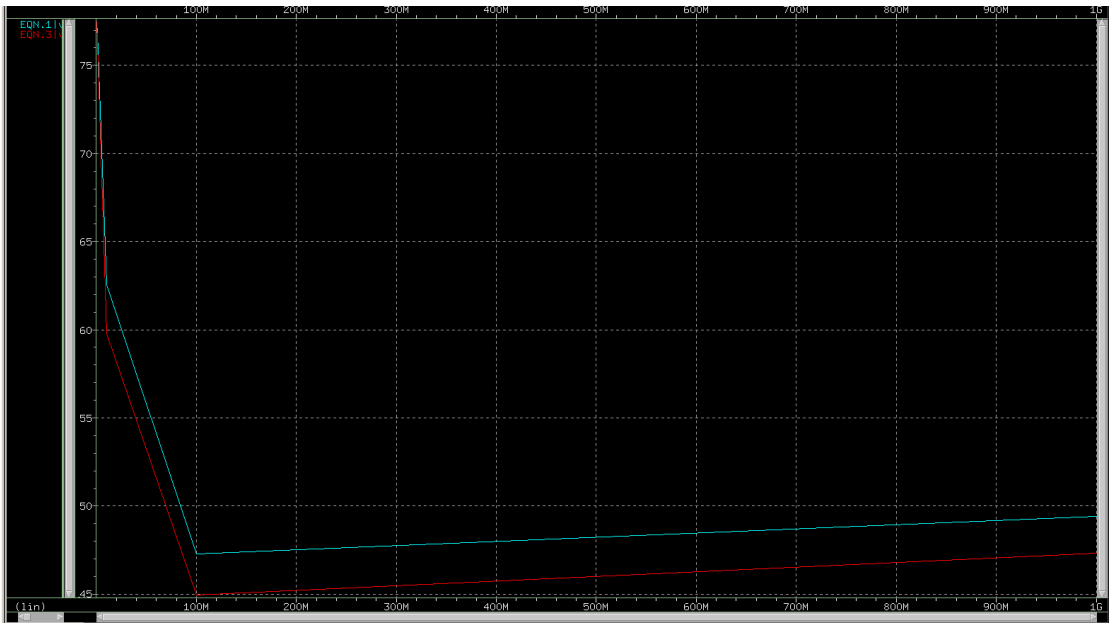


At low freq. CMRR = $|A_v \ / \ A_{cm}|$ = 25.3dB - (-52.1dB) = 77.4dB

is same as that without C_p.



from the figure, -3dB bandwidth with C_p = 1.73M.



Red curve: CMRR with C_p ; Blue curve: CMRR without C_p

(iii) Comment:

The common-mode to differential conversion becomes significant at high frequencies, since r_{o3} is shunted by C_p. $A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1}+g_{m2})(r_{o3}//C_p)+1}$ and at high frequencies, $Z(C_p) = 1/jwC_p$ becomes smaller, so $r_{o3}//C_p$ becomes smaller, and A_{CM-DM} becomes larger, resulting in smaller CMRR.

I compare the -3dB bandwidth , and the one without C_p is bigger than the one with C_p. It's reasonable since CMRR with C_p decrease faster, resulting in smaller bandwidth.

(c)

To calculate $V_{in,CM}$ for all MOS saturation:

element	0:m3	0:m2	0:m1
model	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati
id	20.0557u	10.0278u	10.0278u
ibs	-3.245e-21	-2.8168f	-2.8168f
ibd	-365.4617a	-4.7805f	-4.7805f
vgs	490.0000m	430.2507m	430.2507m
vds	469.7493m	327.4665m	327.4665m
vbs	0.	-469.7493m	-469.7493m
vth	443.4527m	426.6507m	426.6507m

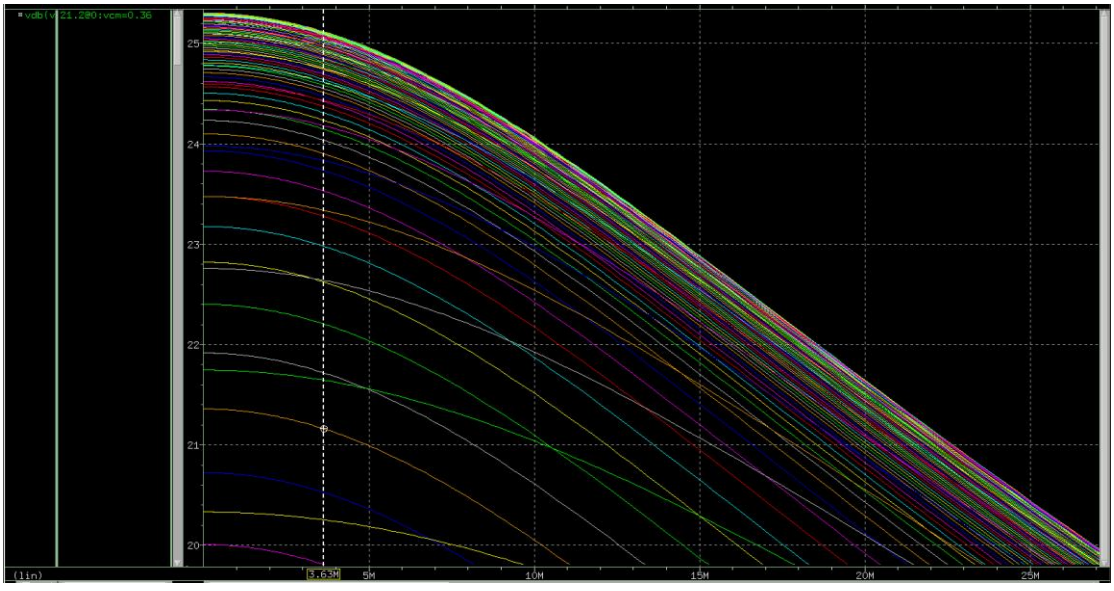
from .lis file

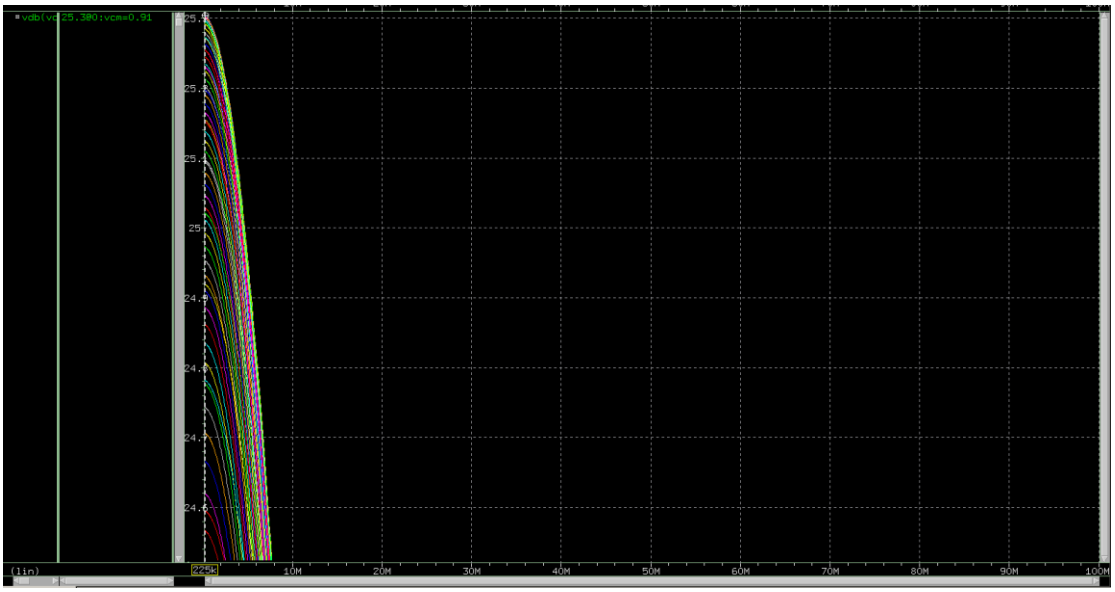
$$V_{GS1}+(V_{GS3}-V_{TH3}) \le V_{in,CM} \le \min[V_{DD}-R_D\frac{I_{SS}}{2}+V_{TH}, V_{DD}]$$

-> $0.43025+(0.49-0.44345) \le V_{in,CM} \le 1.8-100k*\frac{20u}{2}+0.42665$

-> $0.4768 \le V_{in,CM} \le 1.22665$

And from simulation, $0.36 \le V_{in,CM} \le 0.91$





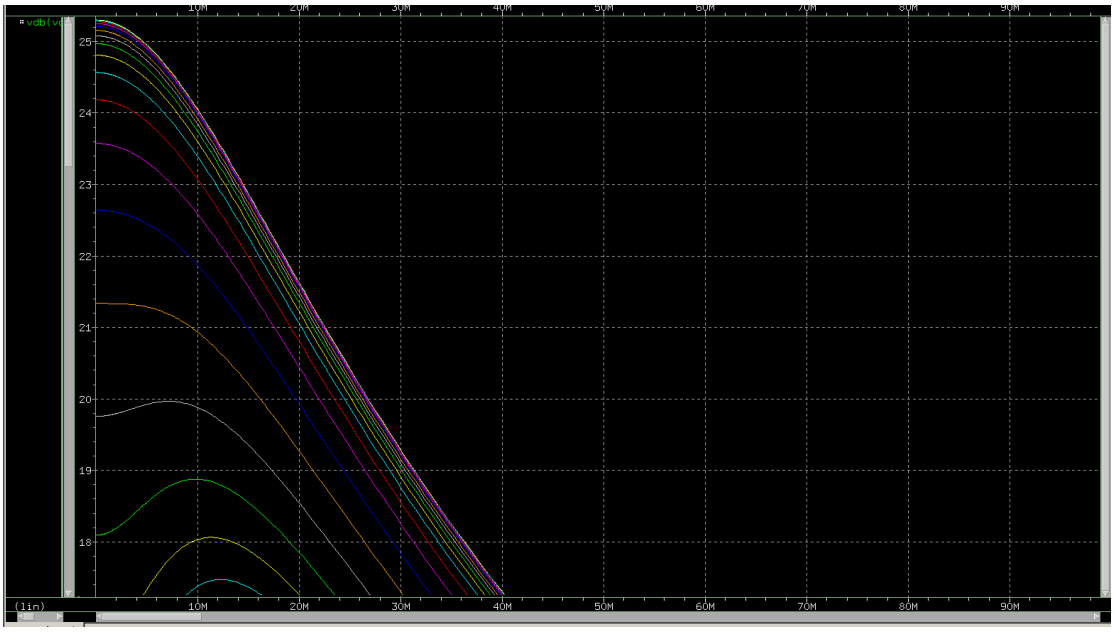
So combine above results, our desire IMCR is $0.4768 \leqq V_{in,CM} \leqq$ 0.91

(d)

The maximum differential input that the circuit can handle:

$$\Delta V_{in} = \sqrt{\frac{2I_{d3}}{\mu_n C_{ox} W/L}} = \sqrt{2}\,(V_{GS1} - V_{TH}) = \sqrt{2}\ (0.43\text{-}0.426)$$

=0.00565V



Above figure is the simulation, and find the one with all MOS in saturation from .lis file(shown below),

```
*** parameter d                  =    8.965E-01 ***

      subckt
      element  0:m3        0:m2        0:m1
      model    0:n_18.1    0:n_18.1    0:n_18.1
      region     Saturati    Saturati    Saturati
       id        20.0560u     9.3848u    10.6712u

 *** parameter d                  =    9.035E-01 ***

      subckt
      element  0:m3        0:m2        0:m1
      model    0:n_18.1    0:n_18.1    0:n_18.1
      region     Saturati    Saturati    Saturati
       id        20.0560u    10.6712u     9.3848u
```

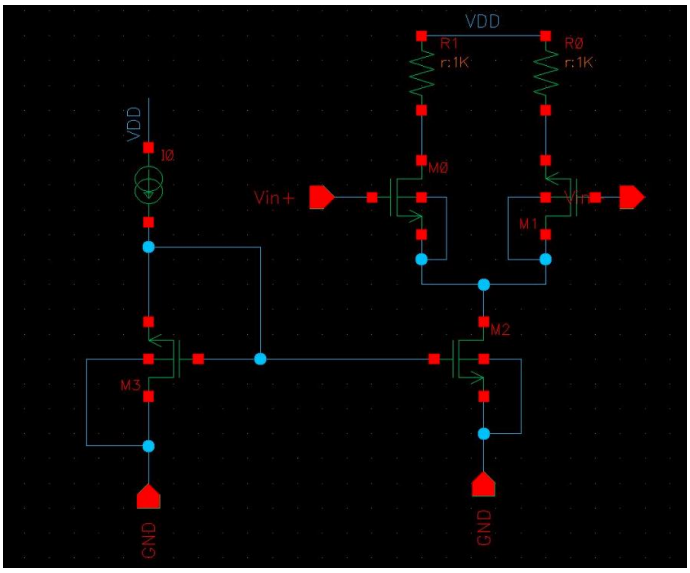
So the input differential maximum is 0.9035-0.8965=0.007V

and the input differential range ΔV_{in} is from 0 to 0.0035.

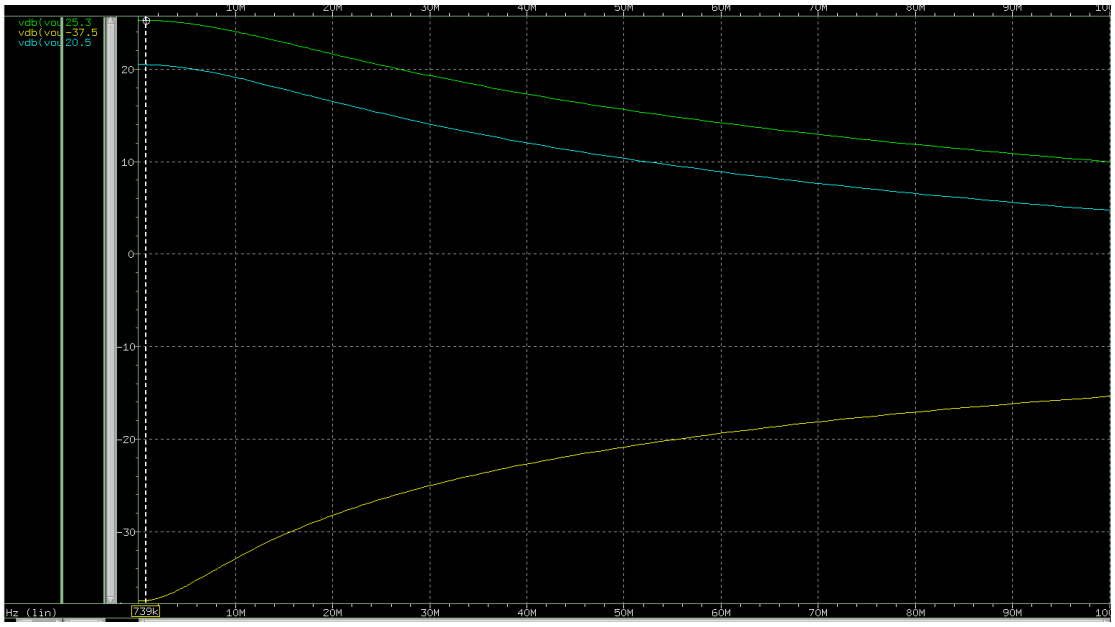
It's reasonable that it's smaller than calculation, since we want all MOS to be saturation.

(e)

Schematic:

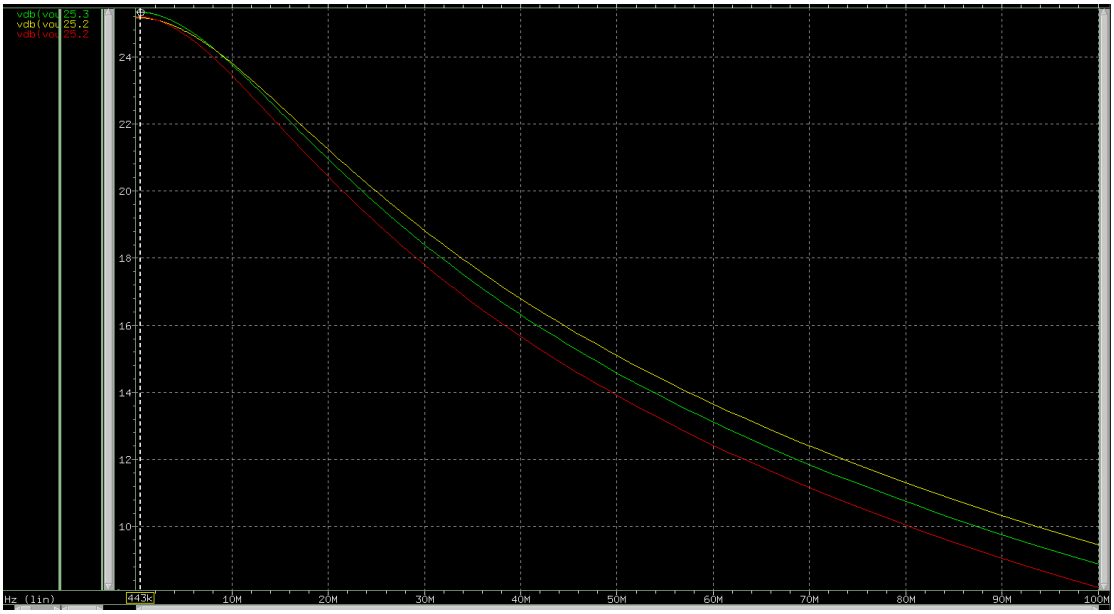


The gain of using ideal voltage source to generate V_b:



Green curve: TT Yellow curve: FF Blue curve: SS

The gain of using current mirror to generate V_b:



Green curve: TT Yellow curve: FF Red curve: SS

Comment:

(i) For TT corner, both methods generating bias voltage will have all MOS in saturation, and reach a voltage gain of 25.3.

(ii) For FF corner, when using current mirror, we can still get a voltage gain of 25.2 and all MOS in saturation at the same time. But when using ideal voltage source, the gain $|A_v|$ can reach 37.5, but not all MOS in saturation.

element	0:m3	0:m2	0:m1
model	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Linear	Linear
id	32.1835u	16.0918u	16.0918u

from .lis file

(iii) For SS corner, when using current mirror, we can still get a voltage gain of 25.2 and all MOS in saturation at the same time. But when using ideal voltage source, the gain will drop to 20.5

and not all MOS in saturation.

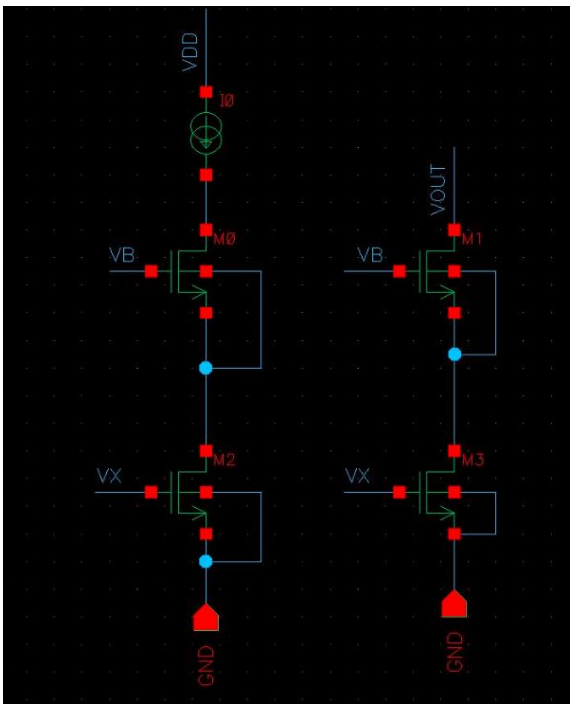
element	0:m3	0:m2	0:m1
model	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Cutoff	Cutoff
id	9.8075u	4.9037u	4.9037u

from .lis file

(iv) We can observe that using current mirror to generate bias voltage is better in all three TT, FF, SS corners, since when operating in different corners, the parameters changed, so if we use the same ideal voltage source, it might not operate in saturation.

2.

Schematic:

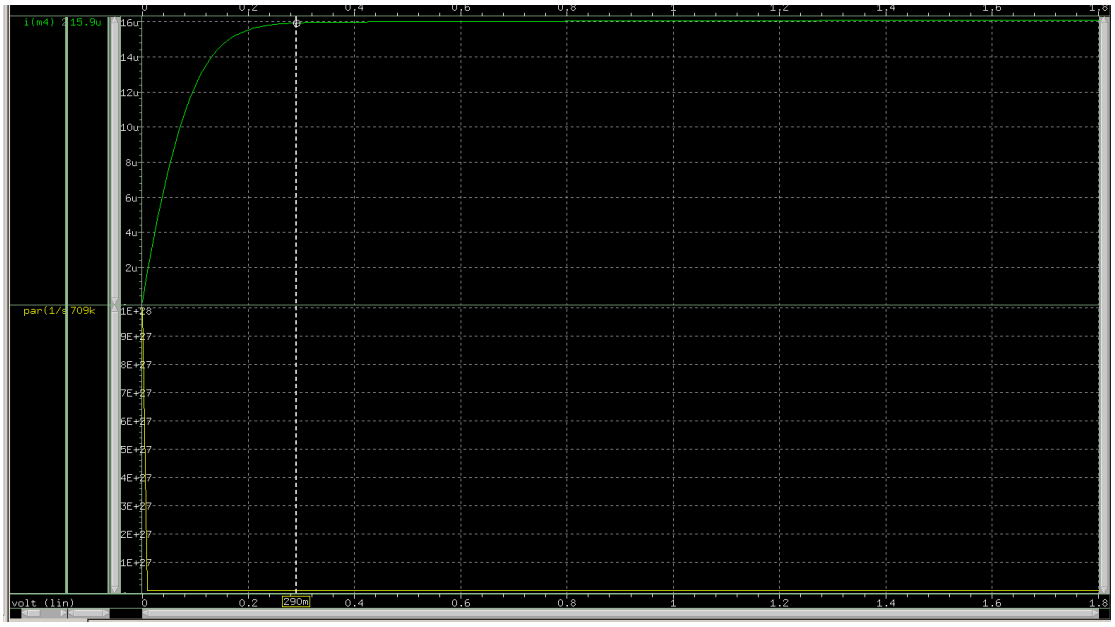


(a)

We want I_{out} to be 16uA and I_{ref} is 4uA, so we want

$4(W/L)_{1,2} = (W/L)_{3,4}$. I use the same length for all of the transistors so as to minimize errors due to the side diffusion of the source and drain areas, and make the multiple finger of 4.

For M1, M2 in saturation, $V_{GS2}+(V_{GS1} - V_{TH1}) \leqq V_b \leqq V_{GS1} + V_{TH2}$



(b)

M6 is guaranteed to be in saturation, since it's gate and drain are connected. But with all transistors in saturation region, M5 can only be in linear region, because $V_{in1} = V_{GS5} = V_{DS5} + V_{GS6}$, $V_{GS6} > V_{th}$ and thus $V_{GS5} - V_{DS5} > V_{th}$.

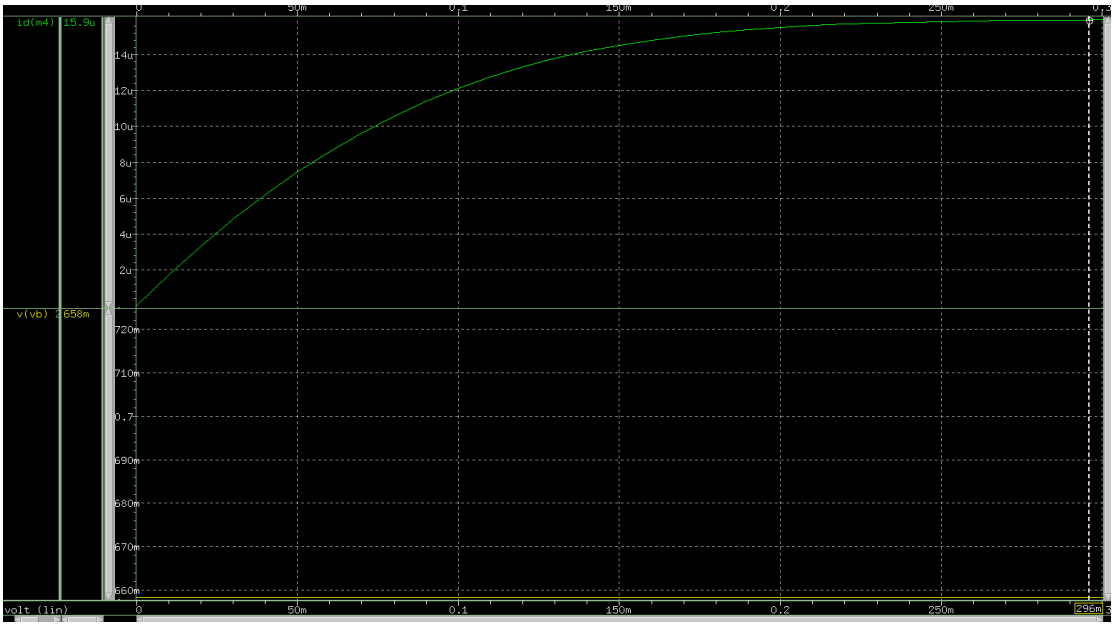
element	0:m4	0:m3	0:m2	0:m1	0:m5	0:m6
model	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Linear	Saturati
id	15.9293u	15.9293u	4.0000u	4.0000u	5.1174u	5.1174u

So we can calculate the current:

For M6: $I_D = \frac{1}{2}\mu_n C_{ox}(W/L)_6 V_{ov}^2$

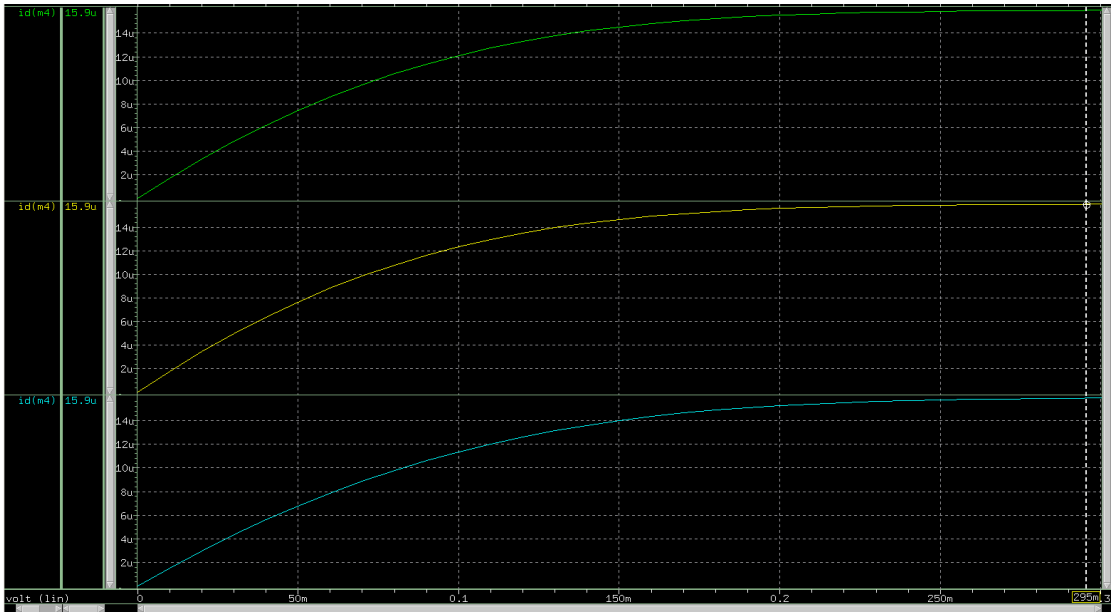
For M5: $I_D = \frac{1}{2}\mu_n C_{ox}(W/L)_5(2(V_{gs} - V_{th})V_{ov} - V_{ov}^2)$

After calculation, we found that $(W/L)_6$ is equal to $(W/L)_5$ times 3, so I design $(W/L)_5$ = 2u/4.5u and $(W/L)_6$ = 2u/1.5u. And I_{D4} can reach 16u, same as the result of giving bias voltage. And there is about 40mV difference from the original one, but I reckon that a roughly 5% difference is acceptable.



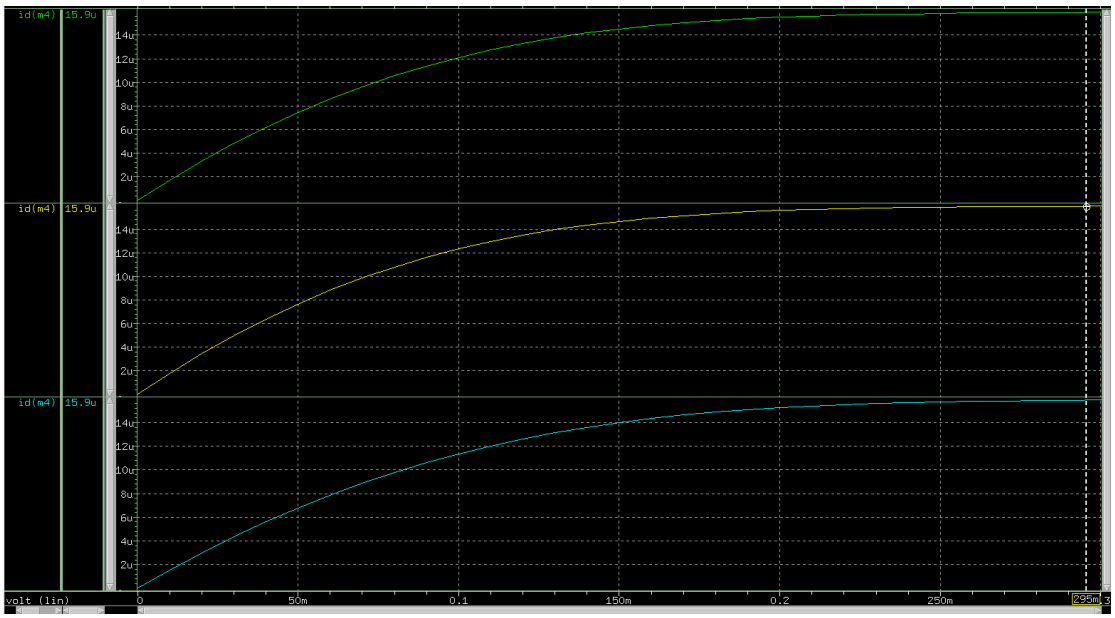
(c)

Figure of output current when using bias generation circuit:



Green curve: TT Yellow curve: FF Blue curve: SS

Figure of output current when using ideal voltage source:



Green curve: TT Yellow curve: FF Blue curve: SS

Comment:

(i) Using bias generation circuit, we have I_{out} close to 16uA, and from .lis file, we found only M5 in linear region as expected.

(ii) Using ideal voltage source, we have I_{out} close to 16uA as well, we concern that there might be transistor other than M5 not being in saturation. But in this case, from .lis file(shown below), we found it alright.

TT:

element	0:m4	0:m3	0:m2	0:m1	0:m5	0:m6
model	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Linear	Saturati
id	15.9195u	15.9195u	4.0000u	4.0000u	4.0000u	4.0000u

FF:

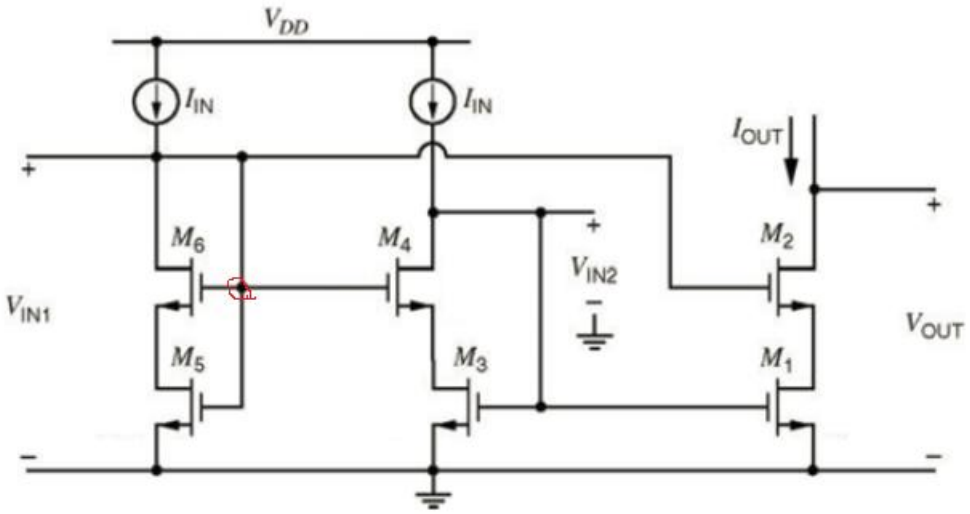
element	0:m4	0:m3	0:m2	0:m1	0:m5	0:m6
model	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Linear	Saturati
id	15.8676u	15.8676u	4.0000u	4.0000u	4.0000u	4.0000u

SS:

element	0:m4	0:m3	0:m2	0:m1	0:m5	0:m6
model	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Linear	Saturati
id	15.9063u	15.9063u	4.0000u	4.0000u	4.0000u	4.0000u

(d) M6 is guaranteed to be in saturation, since it's gate and drain are connected. But with all transistors in saturation region, M5 can only be in linear region, because $V_{in1} = V_{GS5} = V_{DS5} + V_{GS6}$, $V_{GS6} > V_{th}$ and thus $V_{GS5} - V_{DS5} > V_{th}$.

(e)



$V_{in\,1}$ = the voltage with red circle in the figure above =

V_{ov}(M3)+(V_{ov} + V_{th})(M4) = 2V_{ov} +V_{th}