2016 Analog IC Design Homework 2 ***due date: 04/14/2016***

1. Design a PMOS source follower with VDD=1.8V as shown in Fig. 1. (20%)
   (a) Design the W/L sizes of M_1~M_2, dc bias V_b and bias current. To get a voltage gain $V_{out}/V_{in} > 0.95$ for Vin DC voltage from 0V to 1.2V. Plot the V_{in}-V_{out} transfer curve and comments the level shift and the relationship between bias current and sizes. (10%)
   (b) In reality, the body effect exists. Please connect the body of M1 to VDD and redesign the W/L sizes and Vb to get voltage gain $V_{out}/V_{in} > 0.75$ for Vin DC voltage from 0V to 1.2V. Plot the V_{in}-V_{out} transfer curve. (5%)
   (c) Comment on the differences between (a) and (b). (5%)

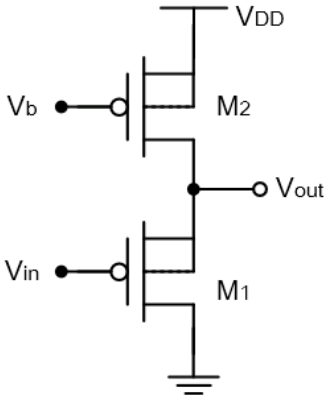

Fig. 1.

2. Design a common-source amplifier with a load R_D = 180KΩ as shown in Fig. 2. (20%)
   (a) With V_{DD} = 1.8V, design the W/L sizes of M_1 and input dc bias V_{in} to get voltage ac gain A_V = $V_{out}/V_{in} > 15$ and V_{out} dc voltage = 0.9V. (10%)
   (b) Add a source degeneration resistor Rs = 20KΩ as shown in Fig. 3. Redesign the dc bias Vin under the same output voltage and M1 W/L sizes. Check the voltage gain AV = Vout/Vin and make a comment between (a) and (b). (10%)

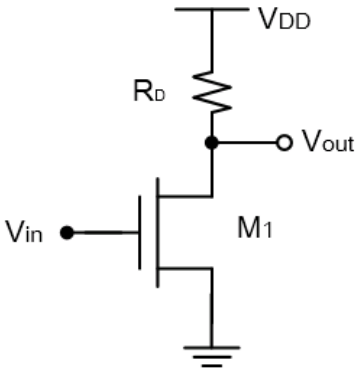

Fig. 2.

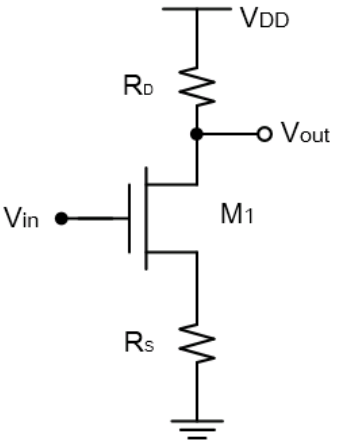

Fig. 3.

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3. Design a common-source amplifier with folded cascoded loading as shown in Fig. 4. (25%)
   (a) With V_{DD} = 1.8 V and I_{bias} = 40uA (bias current of M_2), design the W/L sizes of M_1~M_5, the dc bias V_1 ~ V_4, and input dc bias V_{in} to get voltage ac gain $A_V = V_{out}/V_{in}$ > 45 dB and $V_{out\text{-}swing}$ > 1V. Please explain your design methodology and results. (15%)
   (b) Keep W/L as the same but modify all the m(finger) in (a) to be double, compare the differences of the bias current, voltage gain and output swing and comments. (10%)

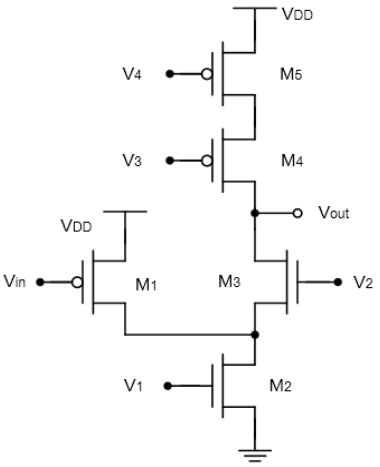
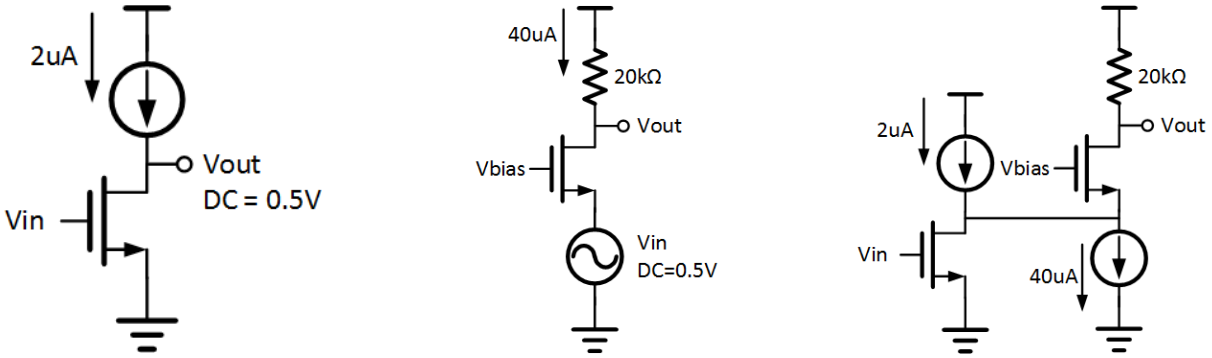


Fig. 4.

4. Use HSPICE to simulate the circuits in Fig. 5 with Vdd=1.8V and do the calculation. (35%)
   (a) Design a common source stage with ac gain A1 >150 and **output DC voltage=0.5 (static current=2uA)** as shown at Fig. 5. (a). (10%)
   (b) Base on the simulation parameter in .lis file, calculate the gain of common source and comment. (5%)
   (c) Design a common gate stage with gain A2>10 and **input DC voltage=0.5 (static current=40uA)** as shown at Fig. 5. (b). (10%)
   (d) Base on the simulation parameter in .lis file, calculate the gain of common gate and comment. (5%)
   (e) Connect two stage as shown at Fig. 5. (c). Whether the DC bias stays the same? The overall gain equals to A1×A2 or not? If not, please explain. (5%)



(a) (b) (c)

Fig. 5

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***

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