Analog IC Design Homework 2

EE17
Student ID: 102061112
Name: Po-Yang Hsieh

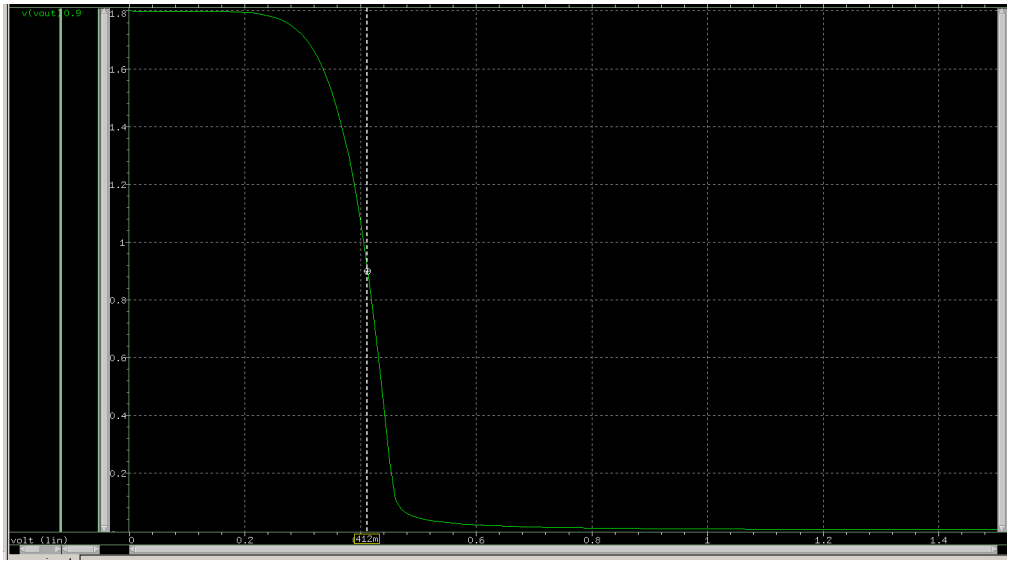
April 8, 2016

1.

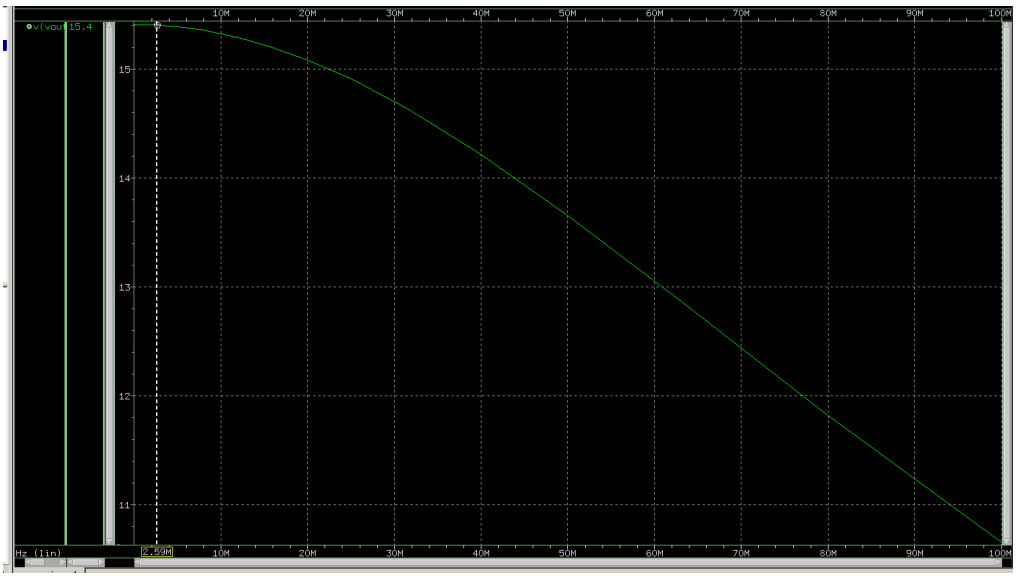
2. (a) Design:

   M1 size$(W/L) = 8.5u/1u$

   When Vin = 412mV, Vout = 0.9V



   The ac gain


v(vout) 15.4
10M
20M
30M
40M
50M
60M
70M
80M
90M
100M
15
14
13
12
11
Hz (lin)
2.59M

(b)