Analog IC Design Homework 2

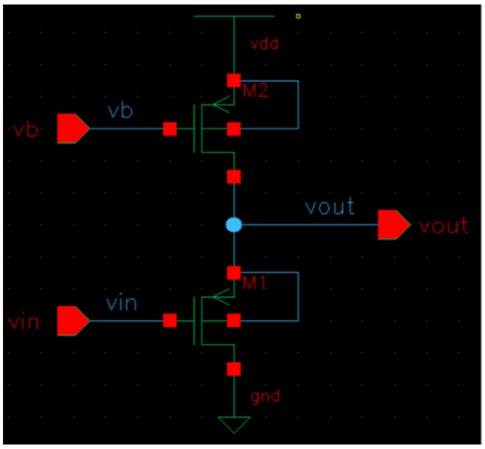
學號: 102061112

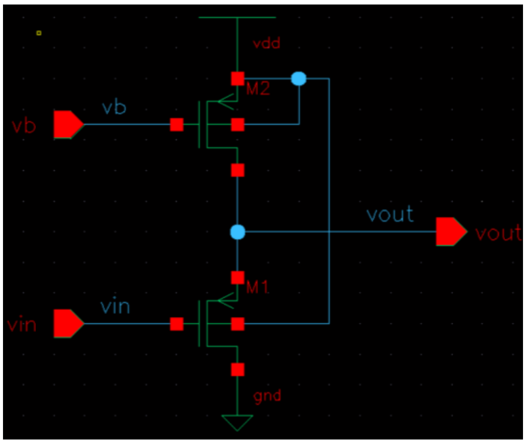
姓名: 謝博楊

1.

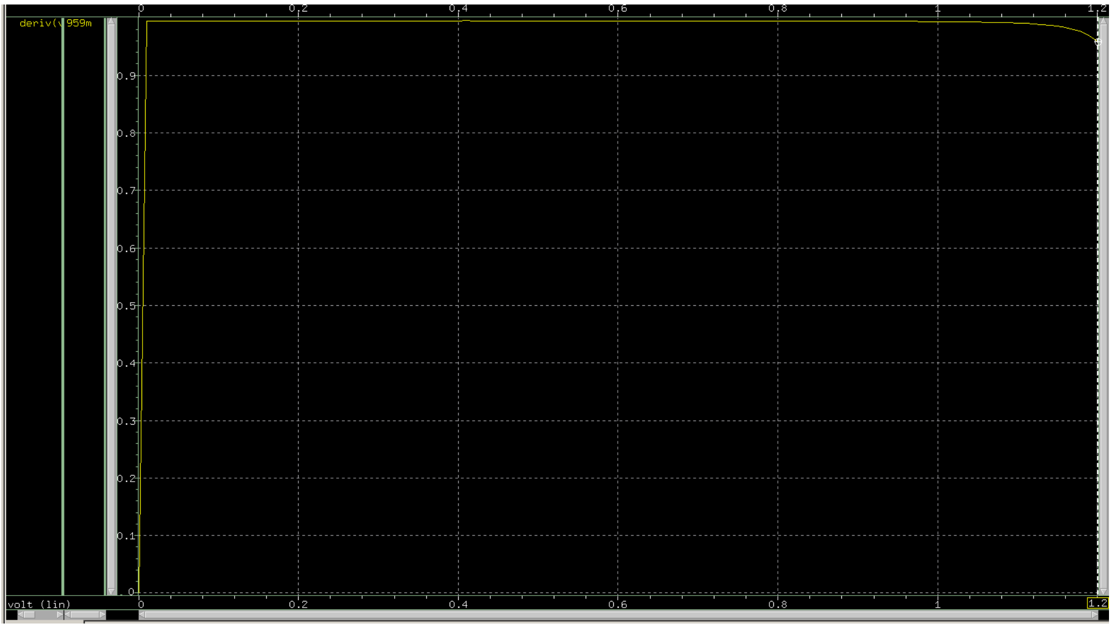
Schematic:

(a) (b)



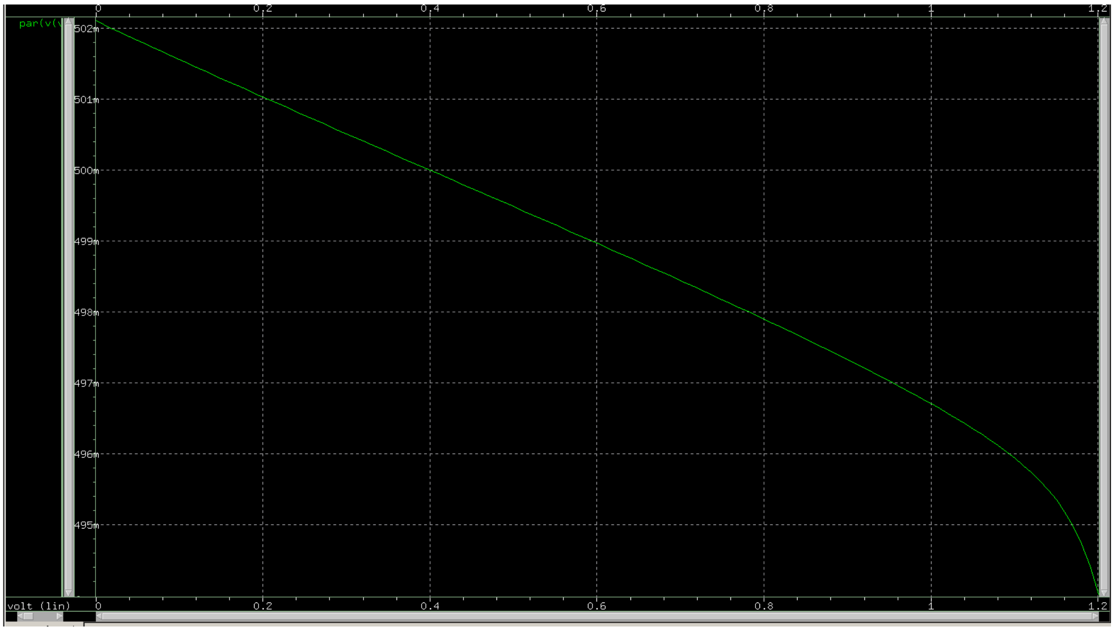


(a) The voltage gain > 0.95:



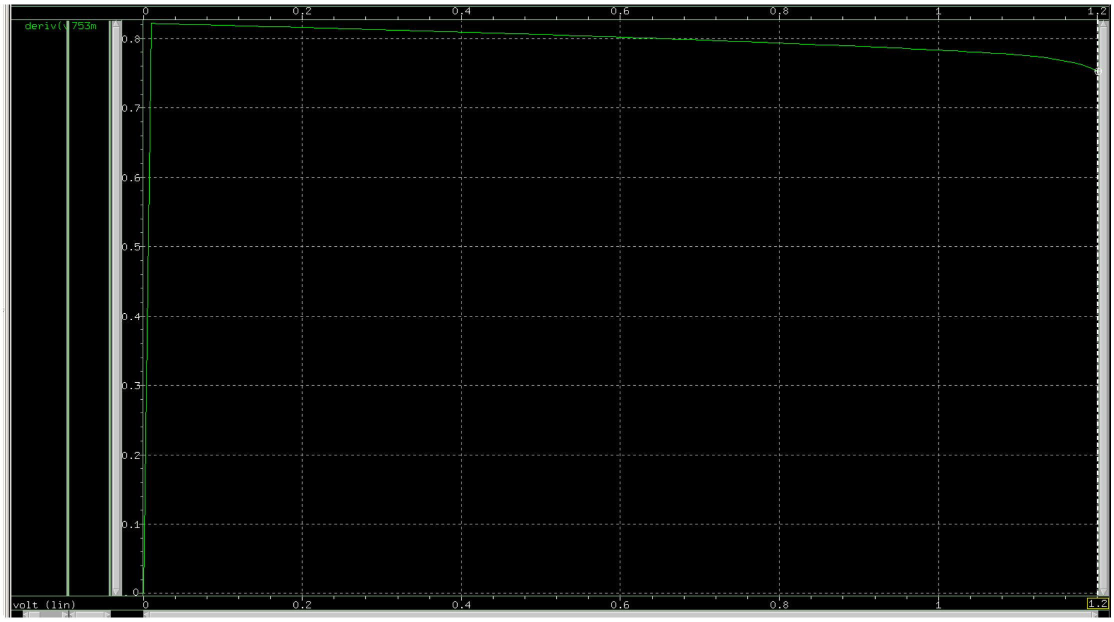
The Vout-Vin transfer curve is almost the same for Vin from

0~1.2V:

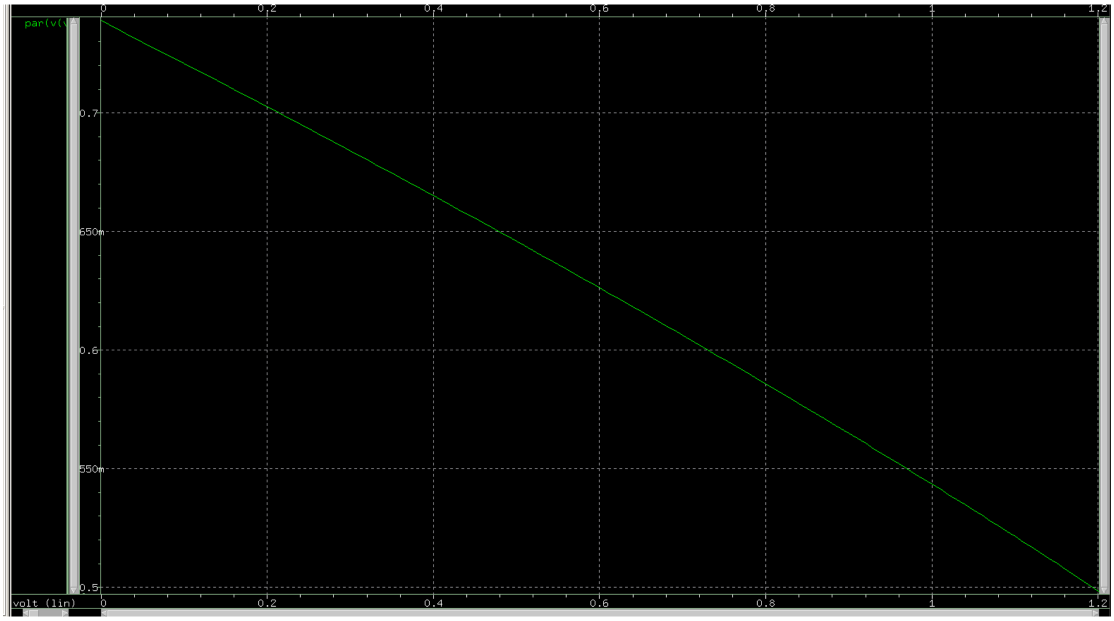


Level shift is almost the same, because our gain is close to 1.

(b) The voltage gain > 0.75:



The Vout-Vin transfer curve:



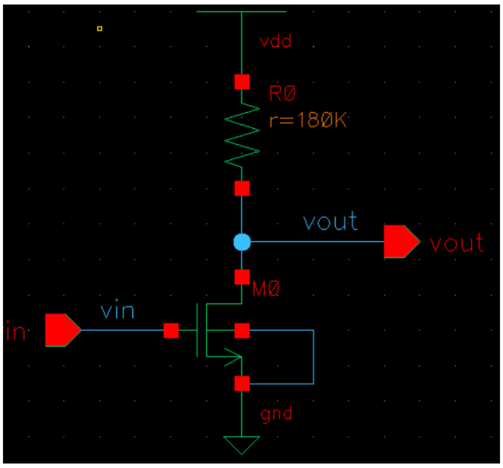
(c)

case (b) has body effect, so the gain is (1/(gm+gnb)), so th gain is smaller than (a)

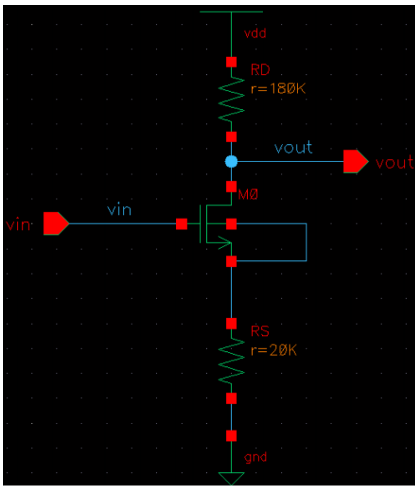
2.

Schematic:

(a)



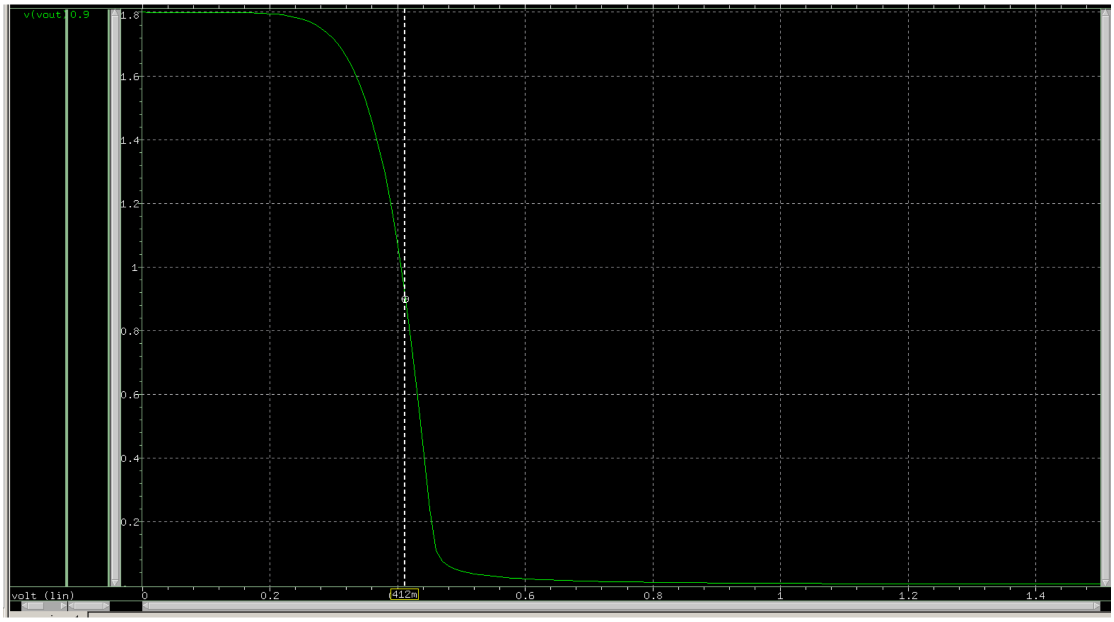
(b)



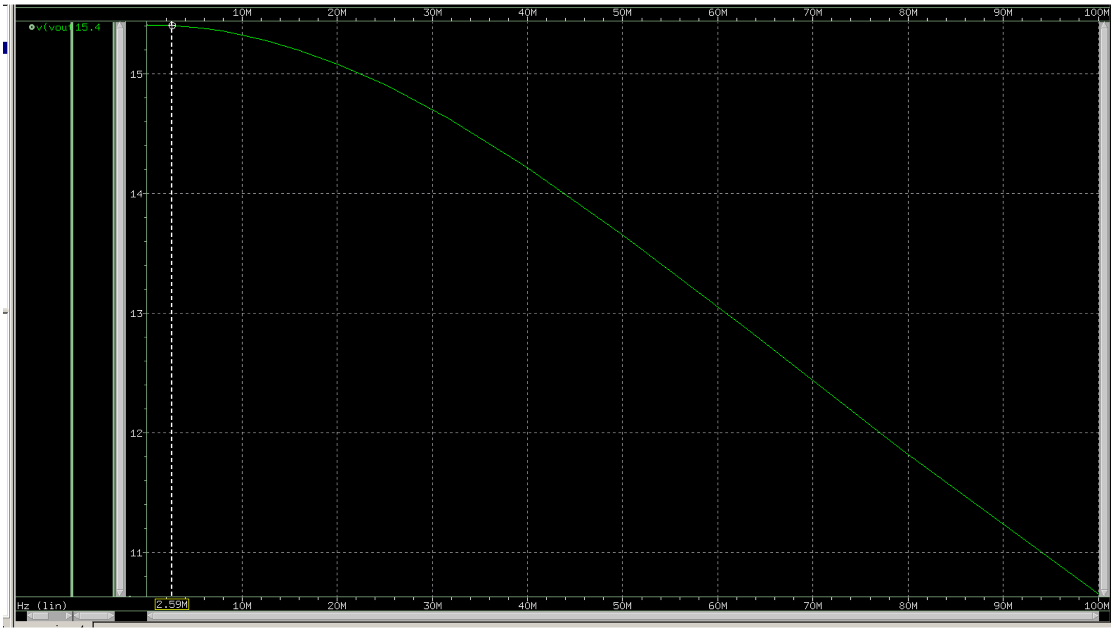
(a) Design:

The size of M1(W/L) = 8.5u/1u,

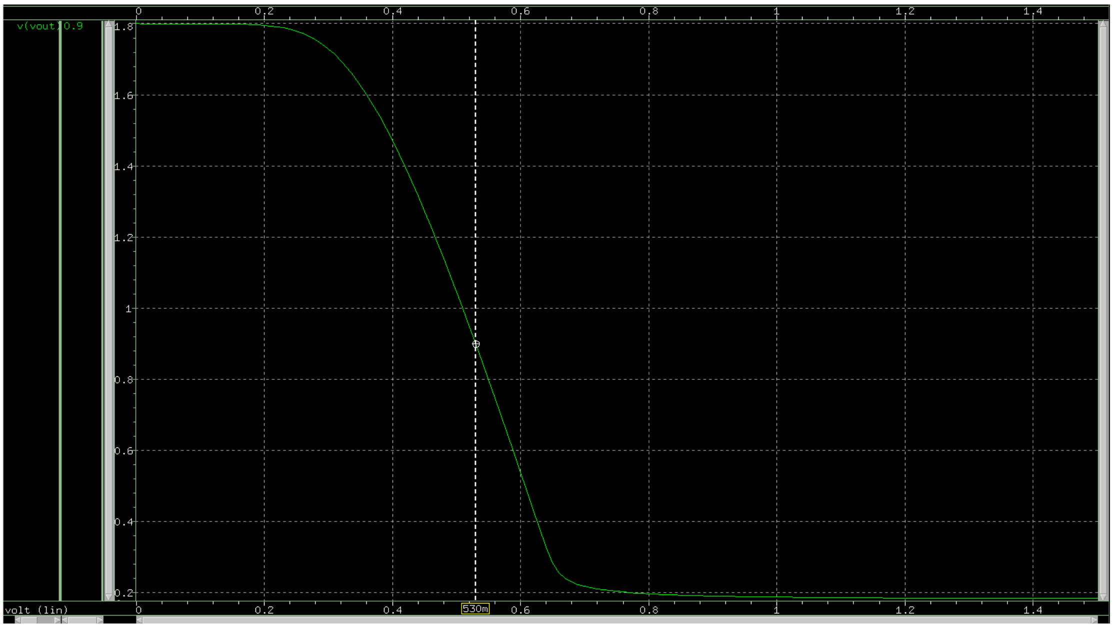
and when Vin = 412mV, Vout = 0.9V.



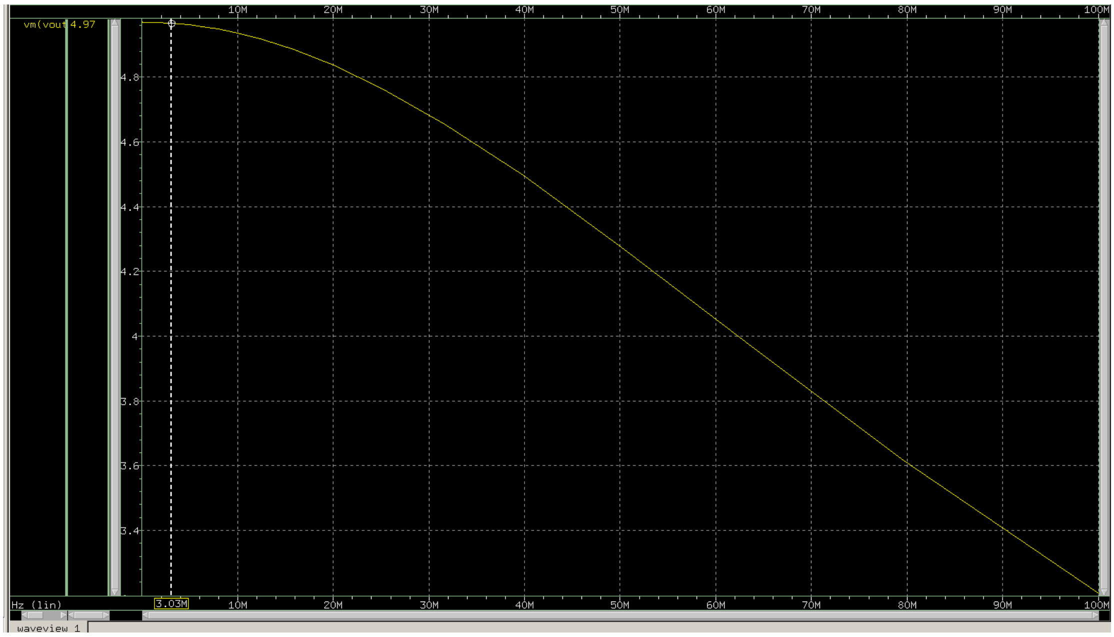
The ac gain is 15.4 > 15 at low frequency:



(b) Same M1 W/L size of (a), and to have the same output voltage Vout = 0.9, I set dc bias voltage Vin = 530mV.



The ac gain is 4.97 at low frequency:

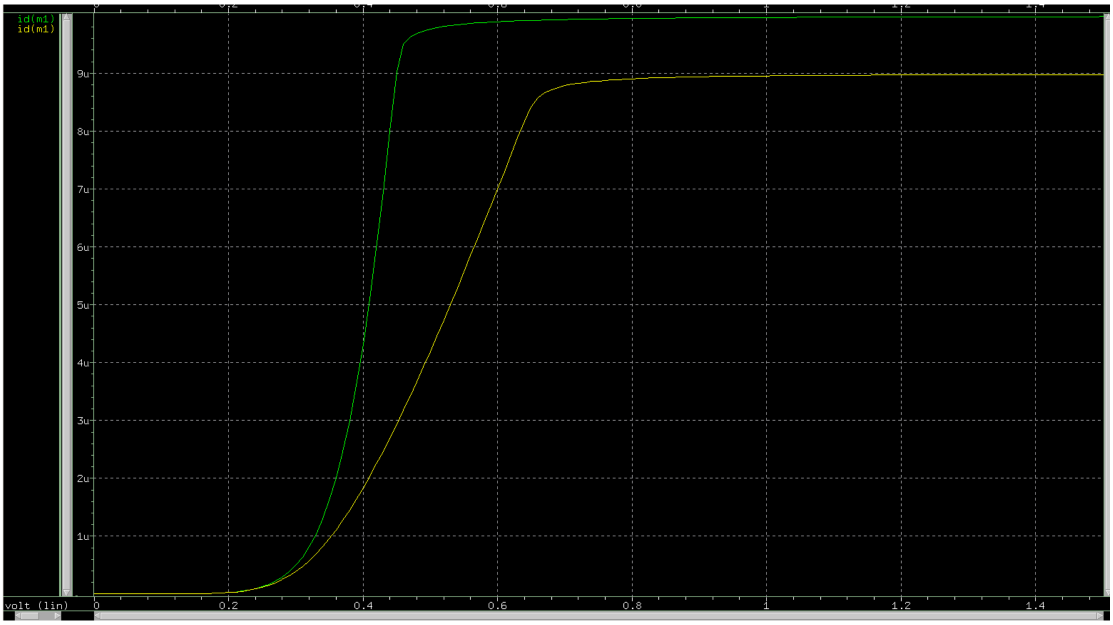


Comments:

(i) When V_{in} increases, I_D increases too, and so does the voltage across R_S, which means some of the voltage between gate and source now drop on R_S, and thus the linearity of case (b) improves in comparison with cases without source degeneration like (a).

(ii) Although the linearity of (b) increases, we actually sacrifice the gain. (Gain from $A_v = -g_m R_D$ to $A_v = -\frac{g_m R_D}{1+g_m R_S}$)

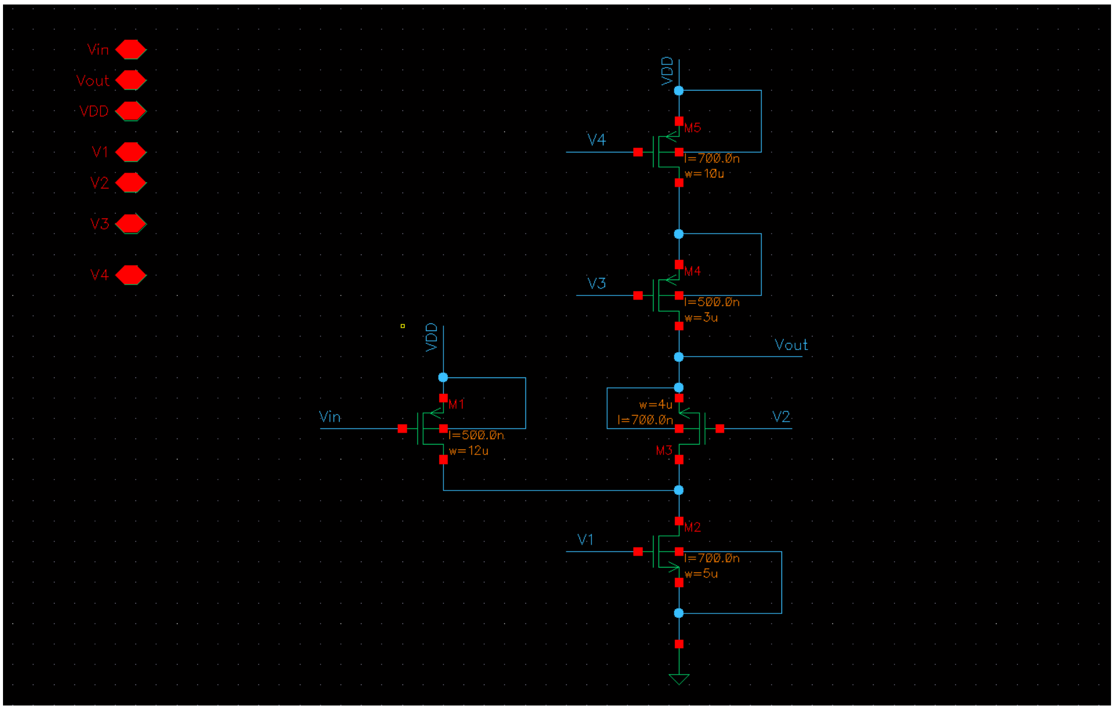
(iii) I_D of (b) is smaller than (a), because the voltage drop across R_S makes V_S higher, resulting in a smaller V_{GS}.



(green curve:(a), yellow curve:(b))

3.

Schematic:



(a) My idea is: The ac gain is proportional to g_{m1}, so if we want a bigger gain, I design g_{m1} to be bigger. And design to make $I_{d3} = I_{d4} = I_{d5} + I_{d1}$ as close as possible to 40uA, and meanwhile, keep all mos in saturation.

(W/L)M1:12u/0.5u, M2: 5u/0.7u, M3:4u/0.7u, M4:3u/0.5u, M5:10u/0.7u. I_{bias} = 41.2uA.

$V_{out-swing} = V_{outmax} - V_{outmin} =$

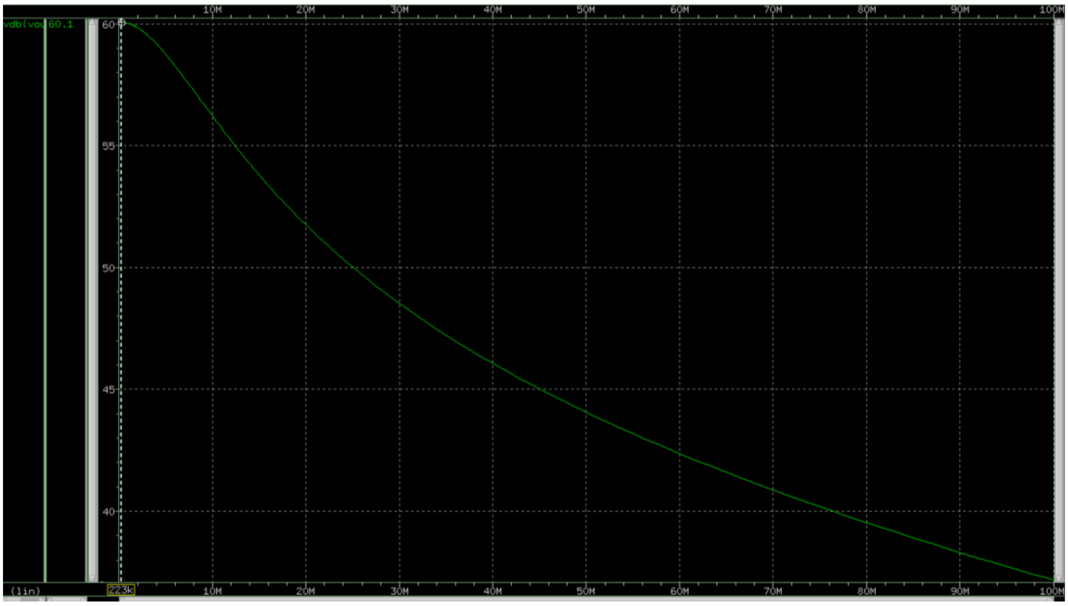
$(V_{DD} - V_{dsat\,4} - V_{dsat\,5}) - (V_{dsat\,2} + V_{dsat\,3}) =$

(1.8-117.87m-94.295m)-(185.565m+68.07m) = 1.3342V >1V.

subckt					
element	0:m1	0:m2	0:m3	0:m4	0:m5
model	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-38.8527u	41.2284u	2.3756u	-2.3756u	-2.3757u
ibs	3.832e-21	-7.296e-21	-4.384e-22	2.885e-22	2.379e-22
ibd	863.5191a	-120.1284a	-305.3220a	105.3855a	26.7767a
vgs	-700.0000m	610.0000m	417.5937m	-594.3872m	-550.0000m
vds	-1.5176	282.4063m	860.3541m	-601.6268m	-55.6128m
vbs	0.	0.	0.	0.	0.
vth	-503.2950m	417.2219m	412.4830m	-514.6767m	-499.0154m
vdsat	-204.4876m	185.5654m	68.0703m	-117.8739m	-94.2951m

from .lis file

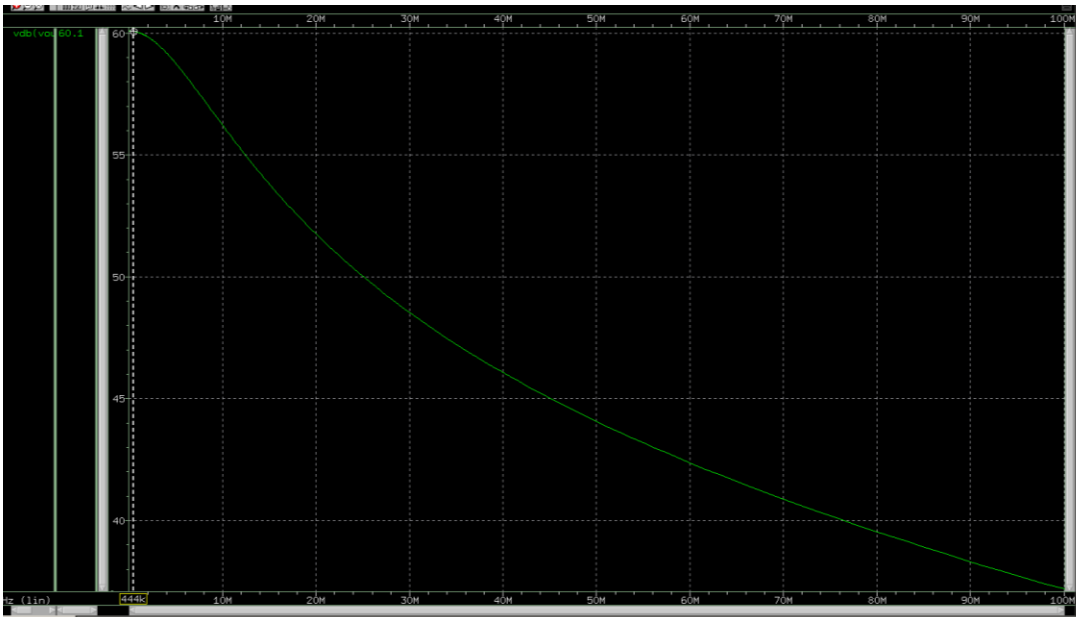
The ac gain is 60.1dB > 45dB at low frequency:



(b) Modify all the m(finger) in (a) to be double means to double the all the W in (a). And from the .lis file, we found it reasonable to have all the currents becomes two times of that of (a) since I_D is proportional to W, and all V_{dsat} remain the same, so $V_{out-swing}$ is the same as (a).

subckt					
element	0:m1	0:m2	0:m3	0:m4	0:m5
model	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-77.7054u	82.4567u	4.7513u	-4.7513u	-4.7513u
ibs	7.664e-21	-1.459e-20	-8.768e-22	5.770e-22	4.758e-22
ibd	1.7270f	-240.2567a	-610.6440a	210.7709a	53.5533a
vgs	-700.0000m	610.0000m	417.5937m	-594.3872m	-550.0000m
vds	-1.5176	282.4063m	860.3541m	-601.6268m	-55.6128m
vbs	0.	0.	0.	0.	0.
vth	-503.2950m	417.2219m	412.4830m	-514.6767m	-499.0154m
vdsat	-204.4876m	185.5654m	68.0703m	-117.8739m	-94.2951m

As for ac gain, it's the same as that of (a):



Since g_m is proportional to W, g_m becomes double, but on the other hand, r_o is proportional to 1/I_D, so r_o becomes 1/2.

And so the gain A_v = $-g_{m1}(g_{m4}(r_{o4} * r_{o5})//g_{m3}(r_{o3}(r_{o2}//r_{o1}))$

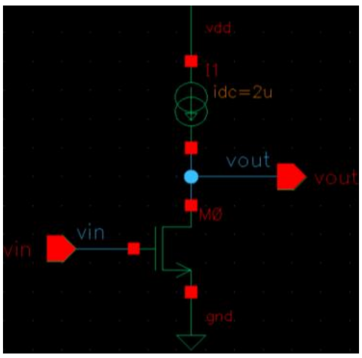
=> 2((2*1/4)//2(1/2(1/2))=>2(1/2)=1(number represents times)

remains the same.

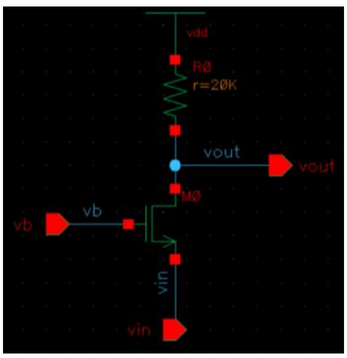
4.

Schematic:

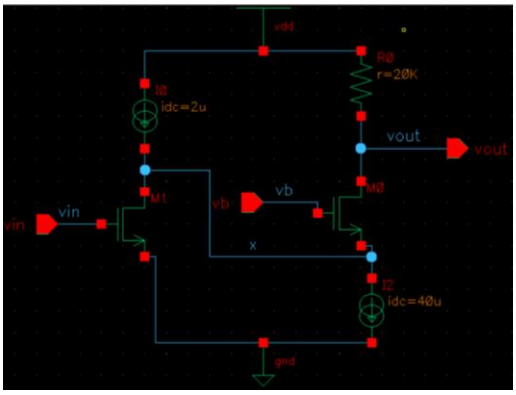
(a)



(c)

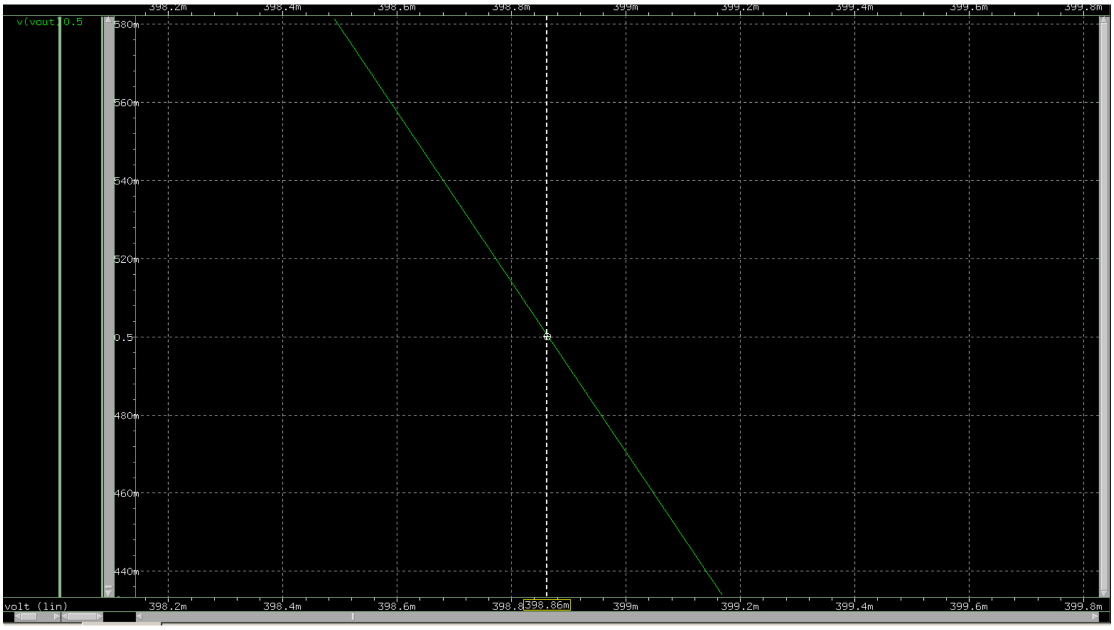


(e)

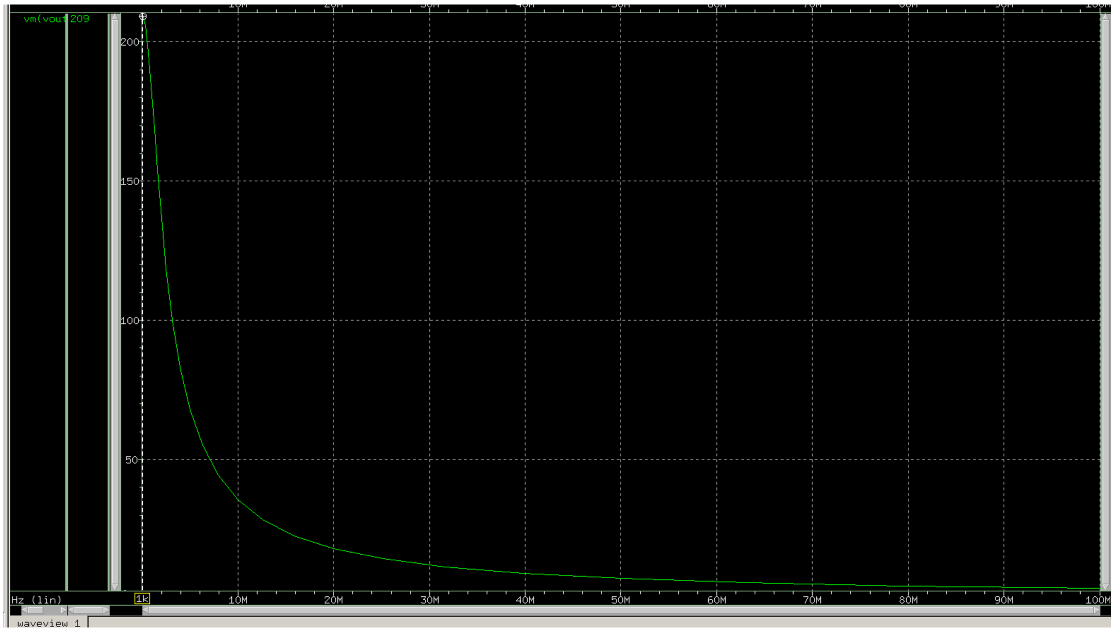


(a) I design the size of nmos to be W/L = 10u/6u,

and when Vin = 398.86mV, Vout = 0.5V.



The ac gain A1 is 209 > 150:



(b) Gain A1 = $-g_m * r_o$ = $-g_m / g_{ds}$ = 32.2064u/154.0038n = -209.127.

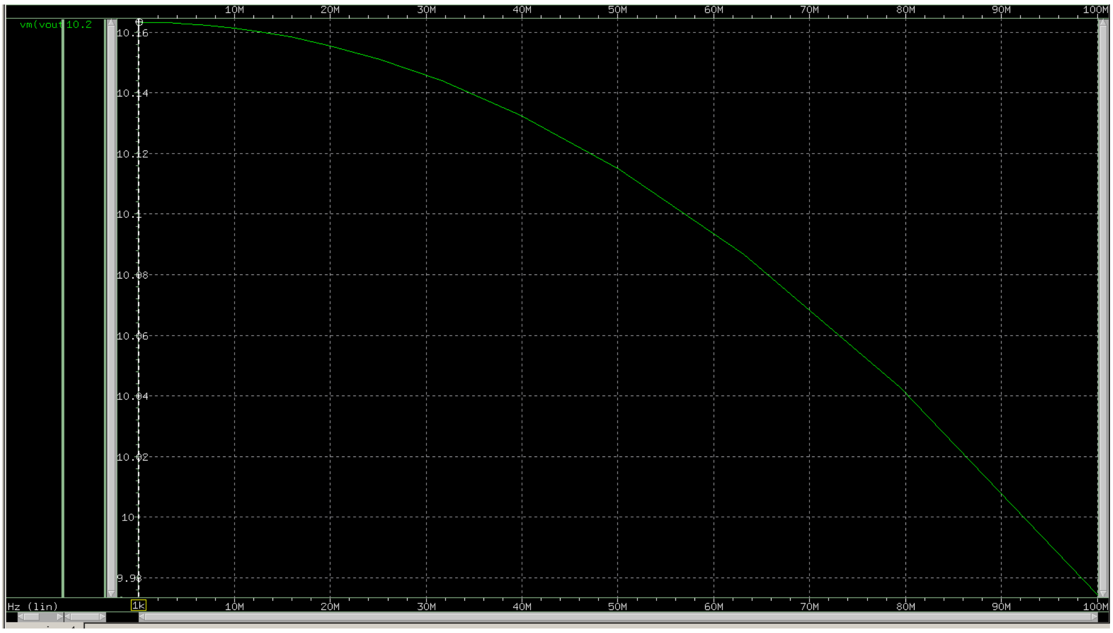
```
gm          32.2064u
gds        154.0038n
```
from .lis file

Since g_m is proportional to 1/L and r_o is proportional to L/I_D and thus L^2, Gain A1 = $-g_m * r_o$ is proportional to L, so to have a higher gain, we raise L bigger, but with constant I, we raise W bigger as well.

(c) I design the size of nmos to be W/L = 14u/1u and the bias voltage 1.1005642V to have a static current 40uA,

```
region      Saturati
 id         40.0000u
```
from .lis file

and gain A2 = 10.2 > 10.



(d) Gain A2 = $(g_m + g_{mb})$*$(r_o//R_D)$ = $(g_m + g_{mb})$*$(\frac{1}{g_{ds}} //R_D)$ =

(497.6027u + 77.2249u)*(17461.20992) ≒ 10.03

gm	497.6027u
gds	7.2698u
gmb	77.2249u

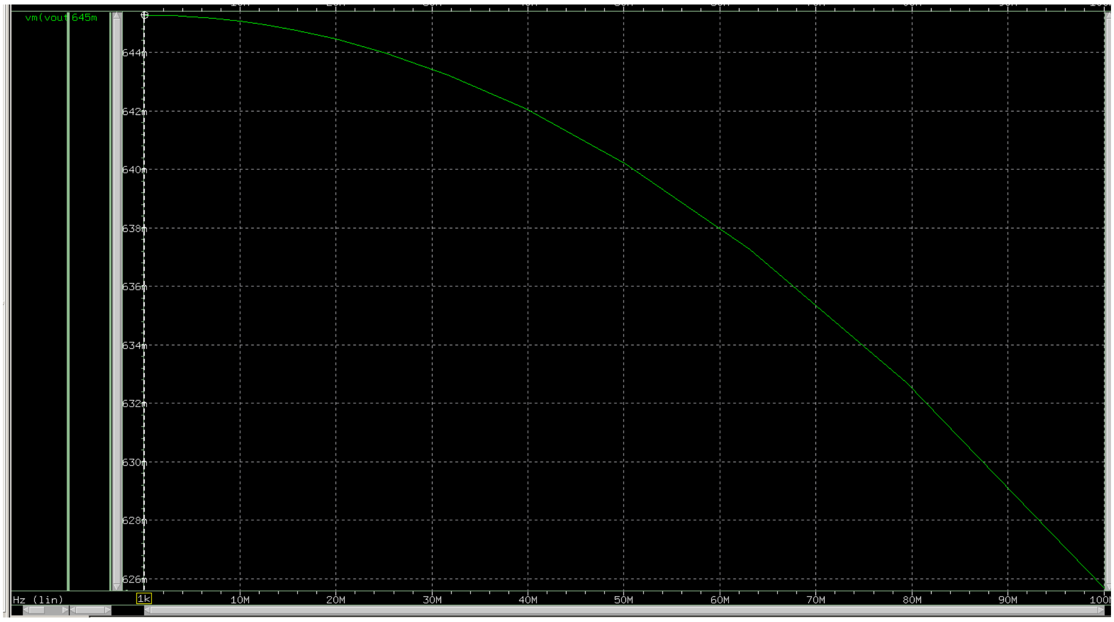
from .lis file

(e)

(i) The DC bias stays the same.

(ii) A1*A2 is about -209*10 = -2090.

And the overall gain is 645m.



The overall gain is not equal to the originally A1*A2, because the R_{out} of the CS stage changes from r_{o1} to $r_{o1}//1/(g_{m2}+g_{mb2})//r_{o2}$ = 6493346.268//1739.652//137555.366 = 1717.47

So A1 should adjust to $-g_{m1}*R_{out}$ = -32.2064u*1717.47 = 0.0553. And the R_{out} of the CG stage changes from $(r_{o2}//R_D)$ to $(r_{o2}*r_{o1}//R_D)$ ≒ R_D, so A2 should adjust to $(g_{m2}+g_{mb2})*R_D$ = 574.8276u*20k ≒ 11.49, which is only a small amount of change. So the major difference is from the CS stage. Here we get the overall gain A1*A2 = 0.053*11.49 ≒ 635m.