Analog IC Design Homework 1

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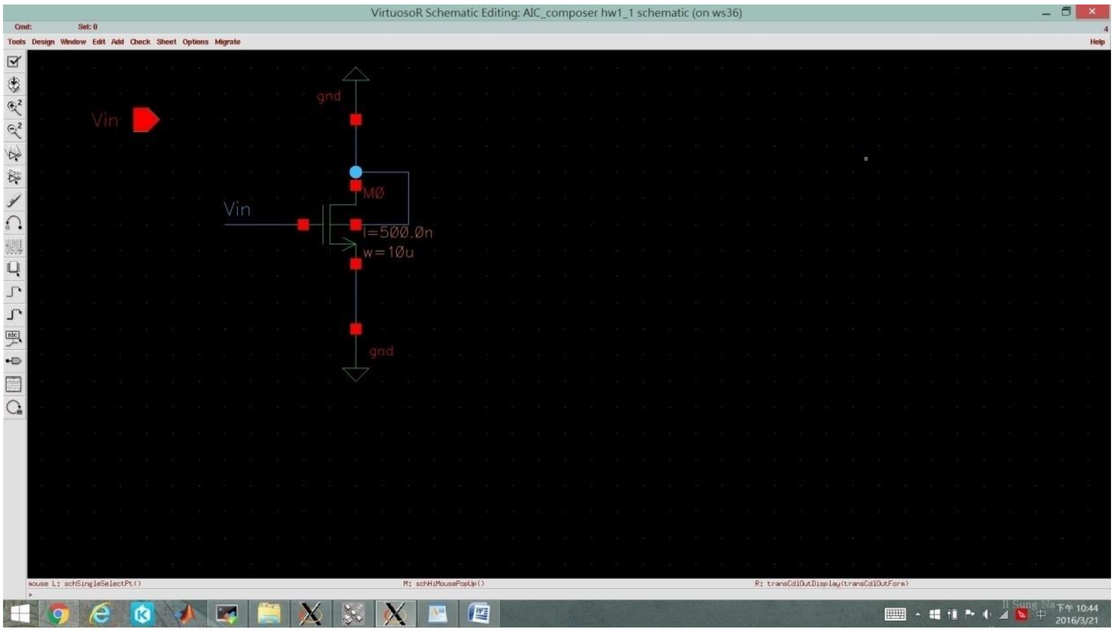
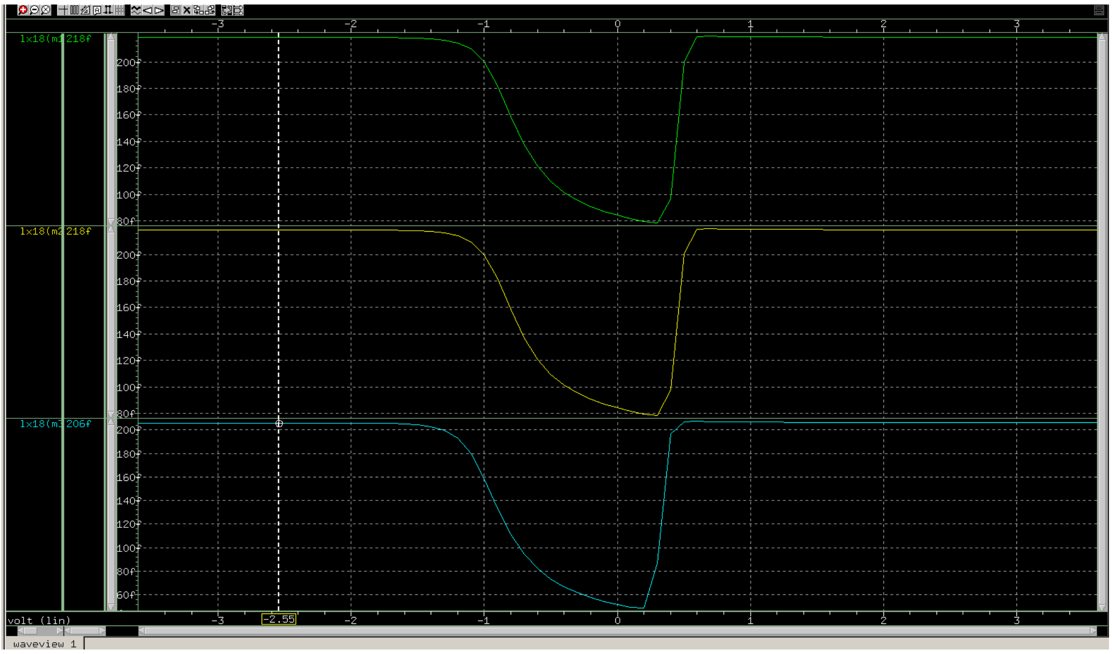
1.

Schematic:



Waveform:



Comments:

(a) The capacitance is 218fF.

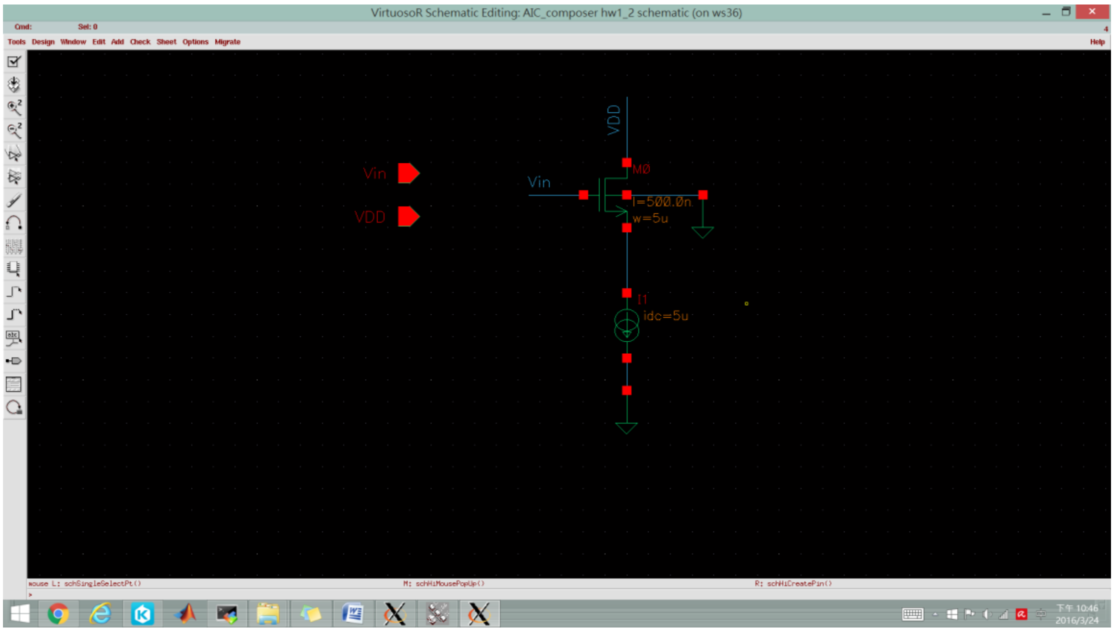
(b) The capacitance is same as (a), 218fF. Since Cgs = Cox*W*L proportional to W*L, with W*L=25um^2. Besides, five capacitors with the same value C parallel with each other is the same as a single capacitor with value 5C.

(c) The capacitance is slightly smaller, 206fF. Though having the same W*L with that of (a) and (b), from the formula $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$, the current proportional to W/L is smaller in case (c), so the depletion region is a little smaller, result in less electrons in inversion layer, so the capacitance is slightly smaller.

(i) When V_{GS} < 0, the device is off, and will attract holes to accumulate under the oxide, and can be seen as a capacitor with value C_{ox} per unit area, so $C_{g,total}$ = $C_{ox}\mathrm{WL}$. When V_{GS} < V_{th}, a depletion region begins to form, so $C_{g,total}$ = $C_{ox}\mathrm{WL}$ in series with C_{dep}. When V_{GS} > V_{th}, the oxide-silicon interface sustains a channel, so $C_{g,total}$ =$C_{gb} + C_{gd} + C_{gs}$ = 0 + 1/2$C_{ox}\mathrm{WL}$ + 1/2$C_{ox}\mathrm{WL}$ = $C_{ox}\mathrm{WL}$.

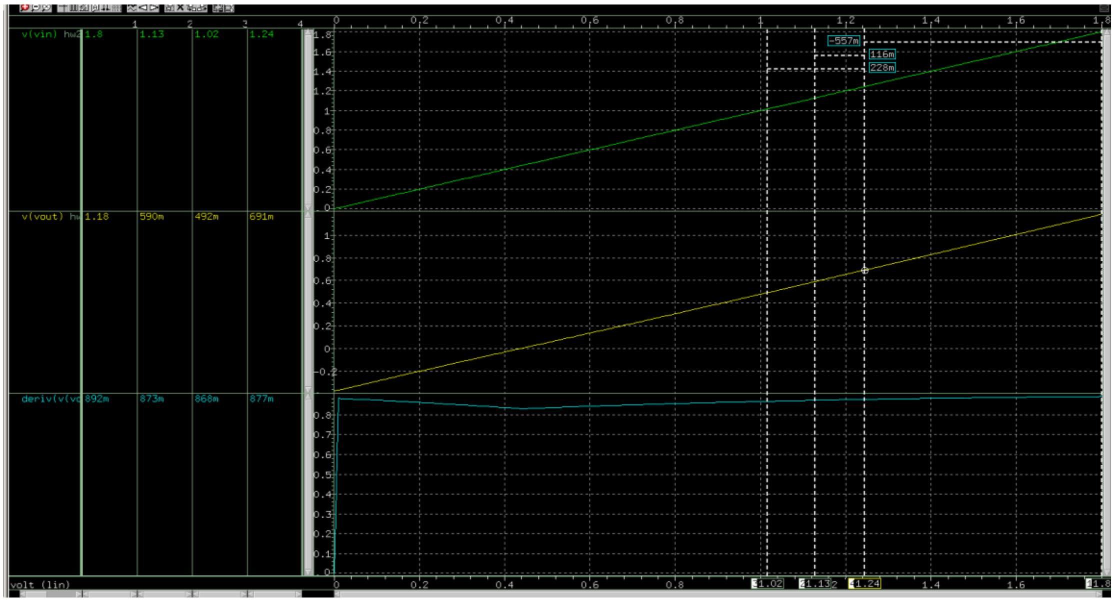
2.

Schematic:



(a)

Waveform:



Comments:

(i) From the figure above:

Vout=1.18V at Vin=1.8V.

The slope is 0.873 at Vout/2=590mV.

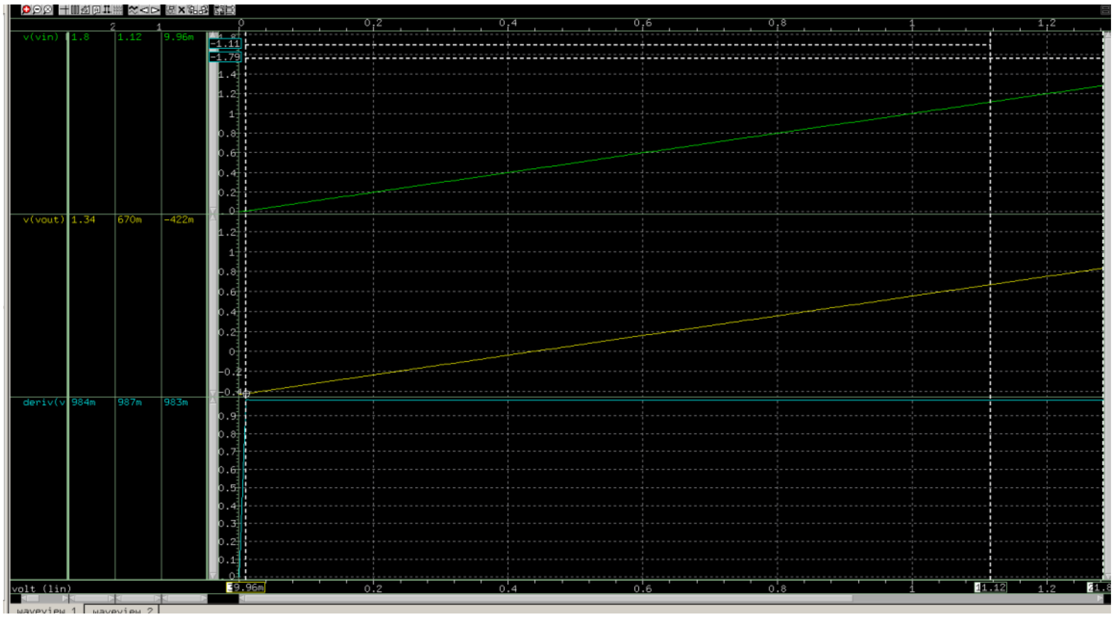
The slope within 0.5% variation is about from 0.868 to 0.877.

The linear range: Vin is from 1.02V to 1.24V, with the corresponding Vout from 492mV to 691mV.

The DC offset is 1.02-0.492=528mV, and 1.24-0.691=549mV.

(b)

Waveform:



Comments:

(i) From the figure above:

Vout=1.34V at Vin=1.8V.

The slope is 984m at Vout/2=670mV.

The slope within 0.5% variation is about from 979m to 988m.

The linear range: Vin is from 9.96mV to 1.8V, with the corresponding Vout from -422mV to 1.34V.

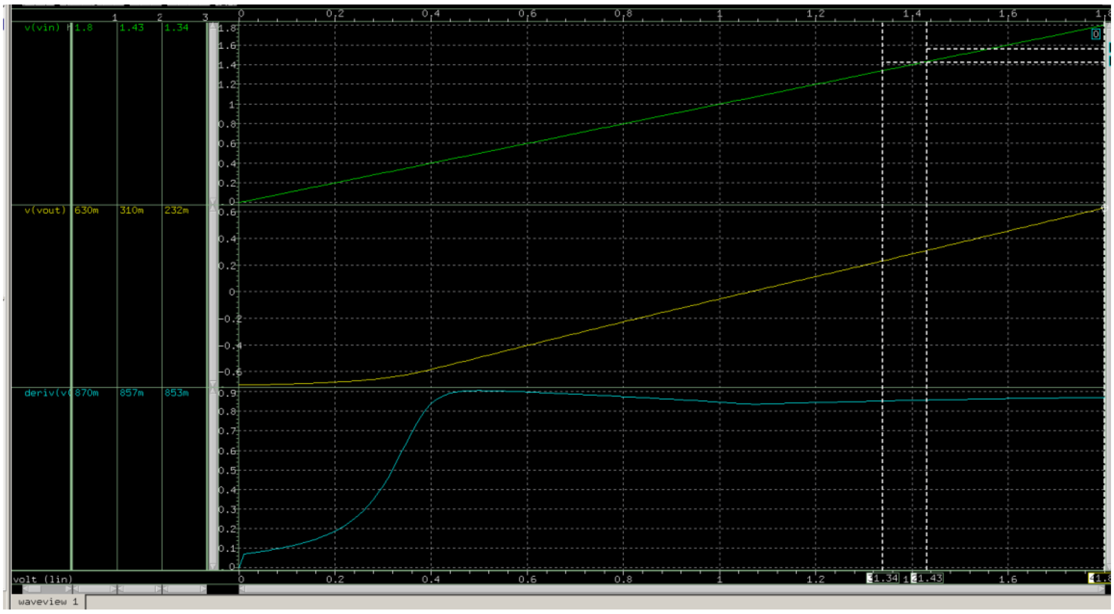
DC offset is 9.96m+422m=431.96mV, and 1.8-1.34m=460mV.

(ii) The DC offset is smaller than that of (a), because with body connected to source node, the body effect is reduced, V_{TH} becomes a little smaller than that of (a), and with I_1 remain the same, $V_{in} - V_{out}$ needs to be a little smaller.

$(I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{out} - V_{TH})^2)$

(c)

Waveform:



Comments:

(i) From the figure above:

Vout=630mV at Vin=1.8V.

The slope is 857m at Vout/2=310mV.

The slope within 0.5% variation is about from 853m to 900m.

The linear range: (we consider Vout>0)

Vin is from 1.34V to 1.8V, with the corresponding

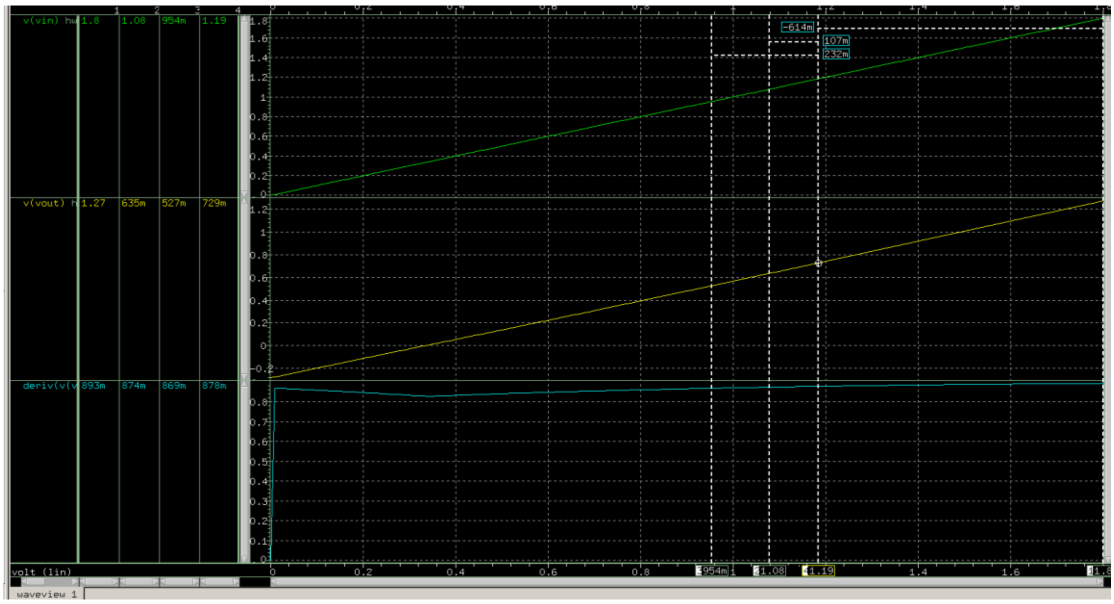
Vout from 232mV to 630mV.

DC offset is 1.34-232m=1.108V, and 1.8-0.63=1.17V.

(ii) The DC offset is much bigger than that of (a), because we need to provide a larger $V_{in} - V_{out}$, in order to provide a much larger current I_1. ($I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{out} - V_{TH})^2$)

(d)

Waveform:



Comments:

(i) From the figure above:

Vout=1.27V at Vin=1.8V.

The slope is 874m at Vout/2=635mV.

The slope within 0.5% variation is about from 869m to 878m.

The linear range:

Vin is from 954mV to 1.19V, with the corresponding

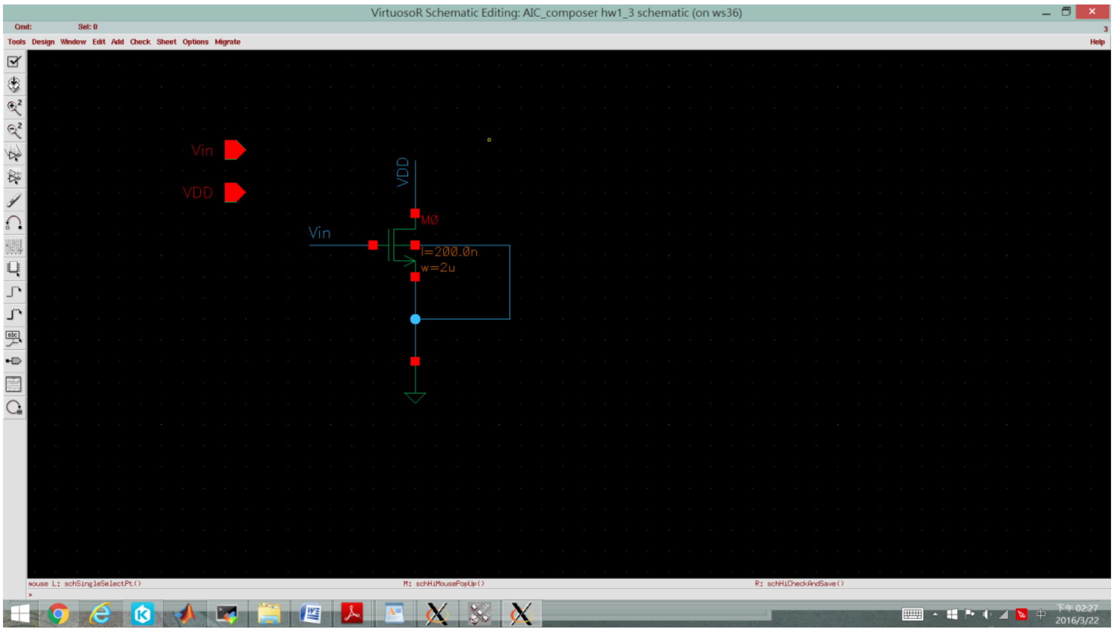
Vout from 527mV to 729mV.

DC offset is 954m-527m=427mV, and 1.19-729m=461mV.

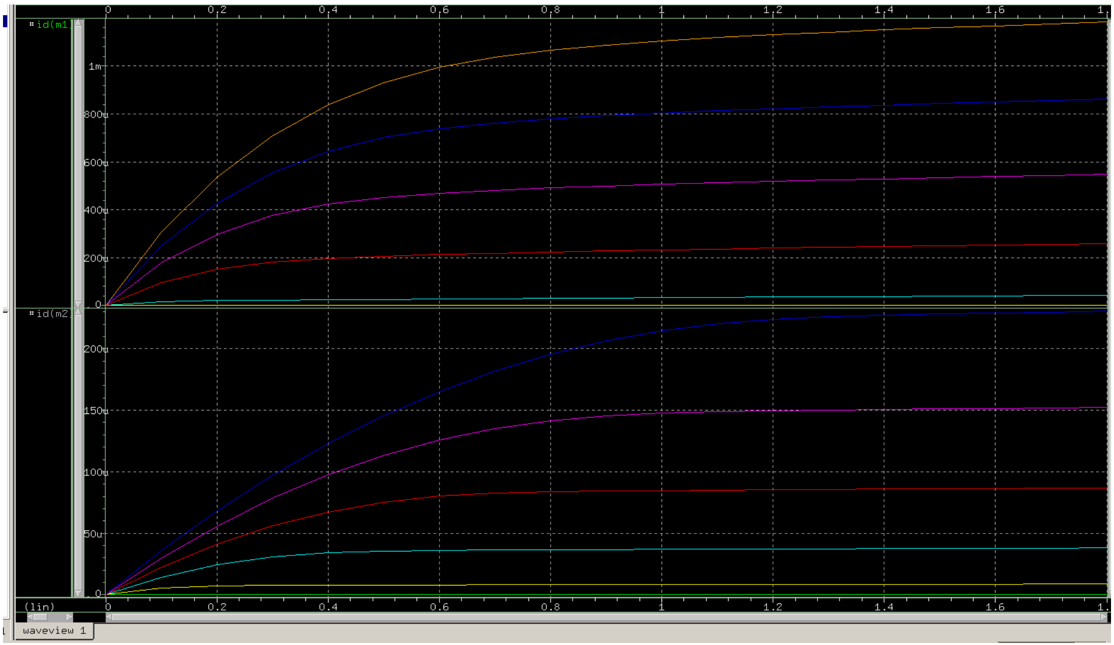
(ii) The DC offset is smaller than that of (a), because with I_1 remaining the same, W/L becomes bigger, $V_{in} - V_{out}$ must become smaller.

3.

Schematic:



Waveform:



Comments: (Channel Modulation Effect)

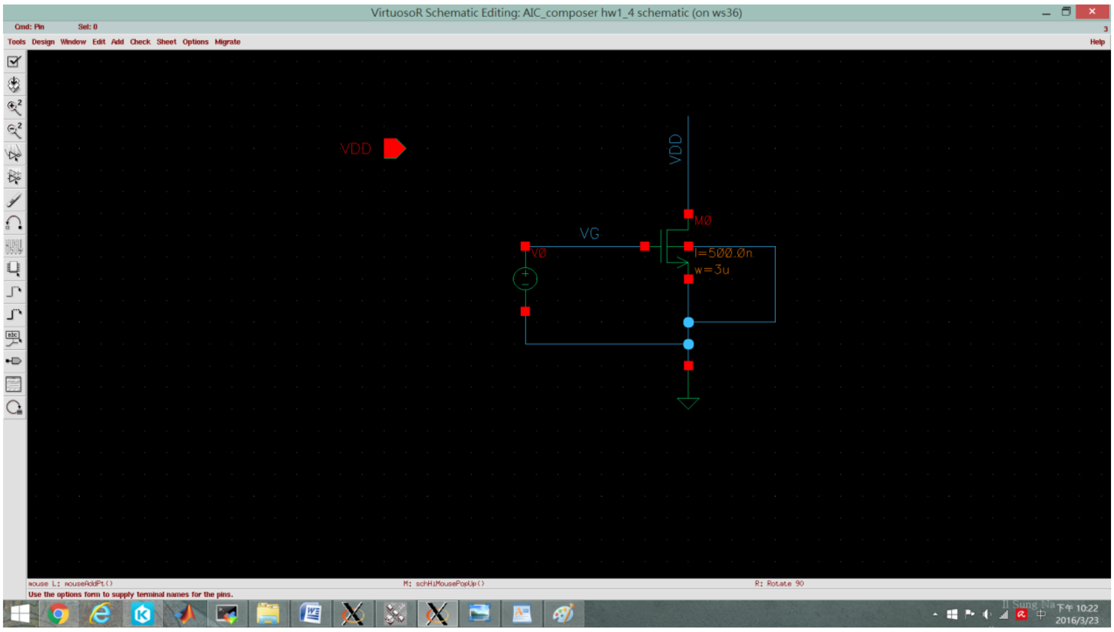
(i) The actual length of the inverted channel gradually decreases as the potential difference between gate and drain increases. So to the same device, as V_{GS} increases, the slope in the saturation region will have bigger change.

(ii) $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS})$, and λ is proportional to $\frac{1}{L}$, so with the same V_{GS}, the device with shorter channel length will have higher drain current. As shown in the figure above, the waveform on the top is the device with W/L = 2um/0.2um, and the one at bottom is the device with W/L = 2um/2um.

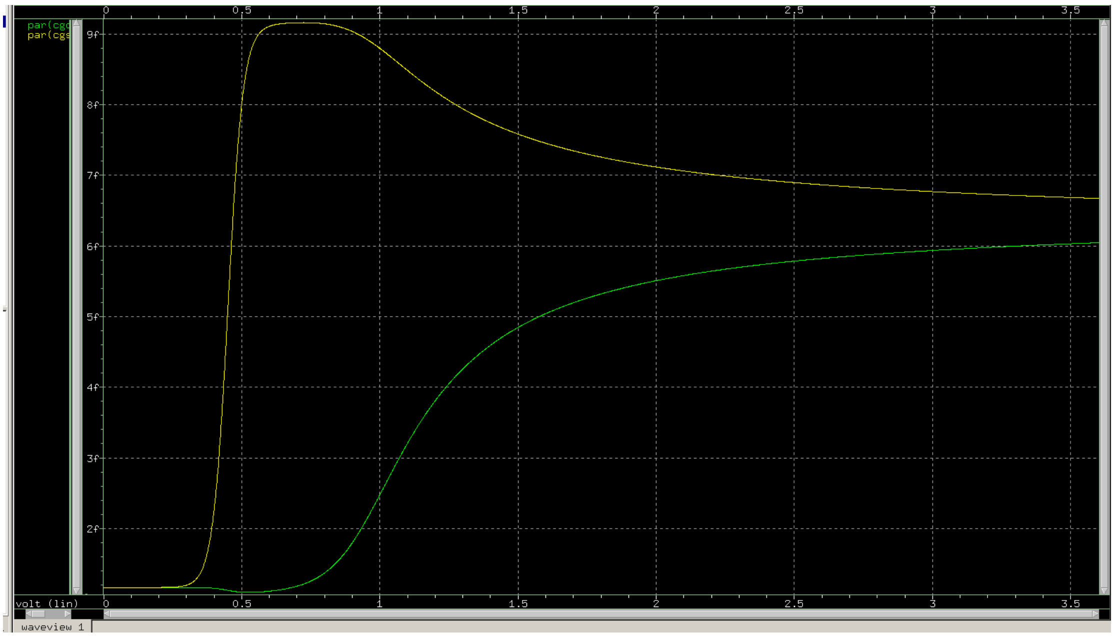
(iii) I_D is proportional to $(V_{GS} - V_{TH})^2$, so with the same channel length, larger V_{GS} means larger I_D.

4.

Schematic:



Waveform:



Comments:

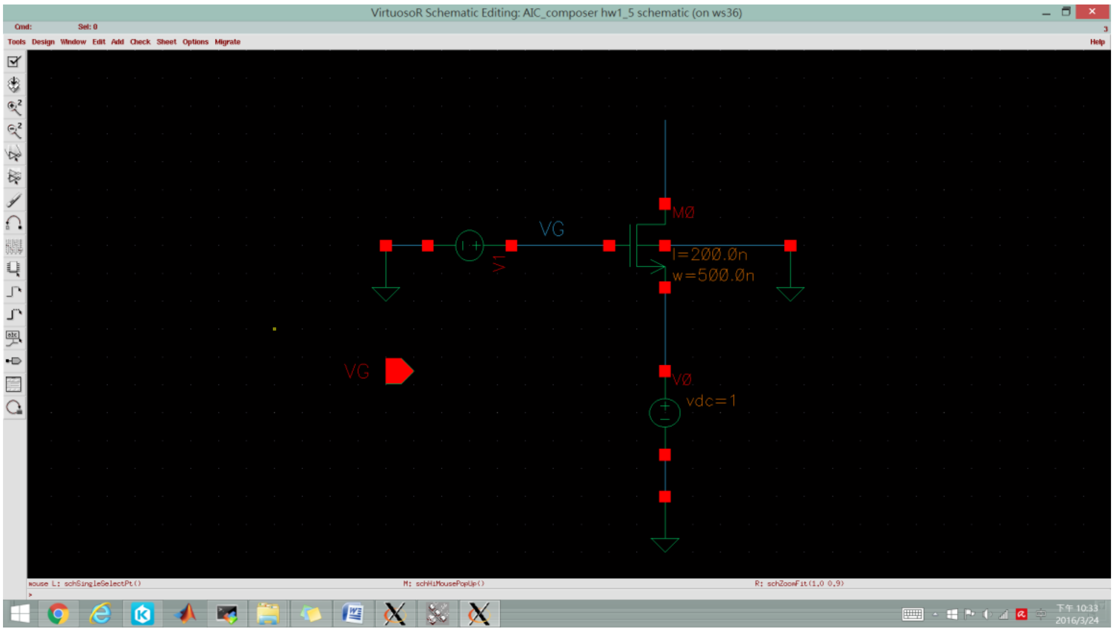
(i) When the device is off, $C_{GD} = C_{GS} = C_{ov}W$.

(ii) When the device is in saturation region, C_{GD} = $C_{ov}\mathrm{W}$. And the potential difference varies from $\mathrm{V_{GS}}$ at the source to $\mathrm{V_{GS}} - \mathrm{V_{TH}}$ at the pinch-off point, resulting in an inhomogeneous electric field, C_{GS} = $C_{ov}\mathrm{W}$ + $\frac{2C_{ox}\mathrm{WL}}{3}$.

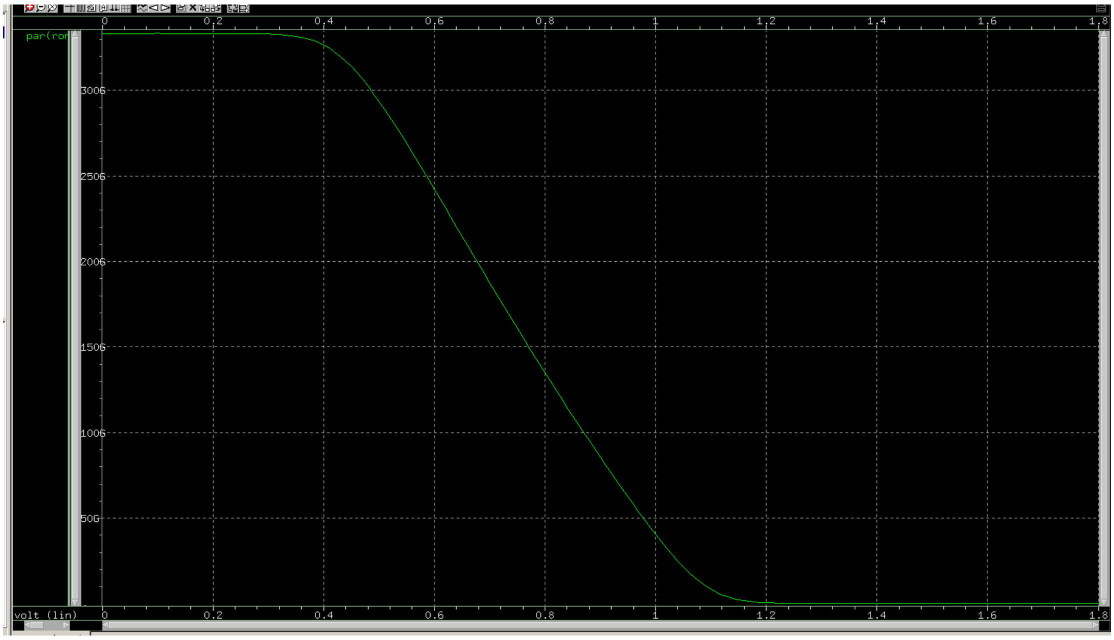
(iii) When the device is in deep triode region, the source and drain voltage are almost the same, and the capacitance between the gate and the channel $C_{ox}\mathrm{WL}$ can be separate evenly by source and drain, so $C_{GD} = C_{GS}$ = $C_{ov}\mathrm{W}$ + $\frac{C_{ox}\mathrm{WL}}{2}$.

5.

Schematic:



Waveform:



Comment:

(i) When $V_{GS} < V_{Th}$, the device is in cutoff region, $I_D = 0$, so

$R_{on} = \infty$

(ii) When $V_{GS} > V_{Th}$, if $V_{DS} << 2(V_{GS} - V_{Th})$, $R_{on} = (\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}))^{-1}$, so when V_{GS} becomes bigger, R_{on} will become smaller, as shown in the figure.