2015 Analog IC Design Final (100%) *due date: 06/25/2015*

1. **Design a Fully-differential (differential-input, differential output) OP. You can select your structure to meet the specifications but have to include the common-mode feedback (CMFB) circuit.**
   A. The OP has to design in sub-circuit, and the sub-circuit nodes neet to be ".subckt opamp iref vdd vinn vinp vocm von vop vss". The netlist has to be named as "My_op.spi".
   B. The output has to drive a loading 20kΩ and 100pF.
   C. The simulation should contain all the corners.
   D. If the supply voltage is decreased, you will get additional bonus. (1% for 0.1V lower)
   E. The Demo will use the test-bench offered by TAs, only the current of iref can be adjusted by your design consideration.
   F. Specification(50%). (ps. Please fill the provided Table)

Design Items	Specifications	My_op (TT)	My_op (SS)	My_op (SF)	My_op (FS)	My_op (FF)
Technology	CIC pseudo technology					
Supply voltage	<1.8V,low as possible					
power	Small as possible					
Loading	100pF / 20KΩ					
DC gain	>85dB,large as possible(8%)					
GBW	>15MHz,large as possible(8%)					
P.M.	>60° (8%)					
C.M.R.R.@10KHz	>100db(3%)					
P.S.R.R.+@10KHz	>100db(3%)					
P.S.R.R.-@10KHz	>100db(3%)					
Unity-gain configuration						
S.R.+(10% ~ 90%)	>5V/us(2%)					
S.R.- (10% ~ 90%)	>5V/us(2%)					
Settling+(1Vpp,0.01)	<0.5ms(2%)					
Settling-(1Vpp,0.01)	<0.5ms(2%)					
Figure of Merit (FoM)						
Small signal	GBW(MHz)/ Power(mW)(5%)					
Large signal	SR(V/us)/ Power(mW)(5%)					

by CCHsieh

2. **Report Must Contain : (50%)**
   A. **Schematic (including core amplifier circuits, common mode feedback, biasing circuits, etc.).(10%)**
   B. **Simulation results of each specification (AC/DC/transient/..) and contains all corners.(15%)**
      Please explain how to find the spec for your own OP and make the comparison.
   C. **Design procedure and consideration (15%)**
      Briefly express your design consideration and optimization on selected circuit structure, device value, voltage, compensation, and common mode feedback issues.
   D. **Discussion and conclusion (10%)**
      Discuss your experience on this project, problem during design, and conclude what you get and suggest for this course

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***