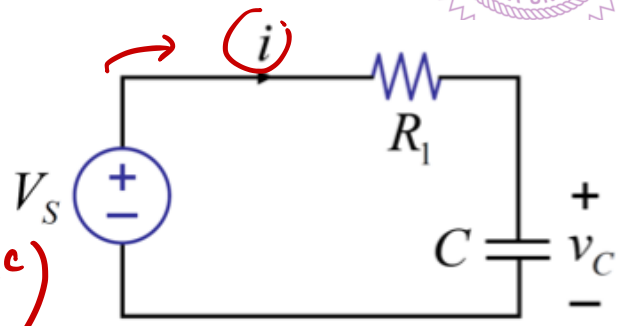
Total Energy Provided by Source During T_1

$$E = \int_0^{T_1} v \cdot i \, dt = \int_0^{T_1} V_S \cdot i \, dt$$

$$= \int_0^{T_1} V_S \cdot \frac{V_S}{R_1} e^{-t/R_1 C} \, dt = V_S^2 \cdot C \cdot \left(1 - e^{-t/R_1 C}\right)$$



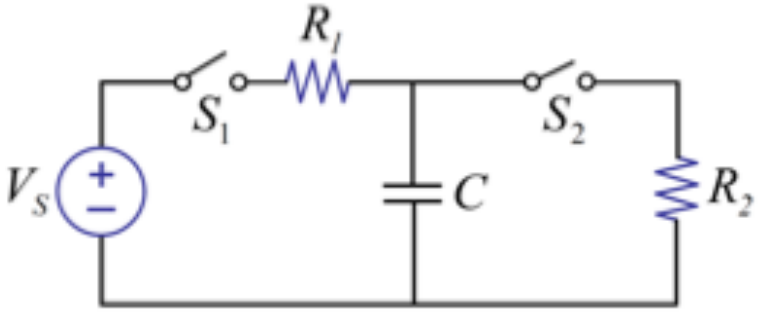
If $T_1 \gg R_1 C$, $e^{-t/R_1 C}$ can be ignored

$$E_1 \approx V_S^2 \cdot C$$

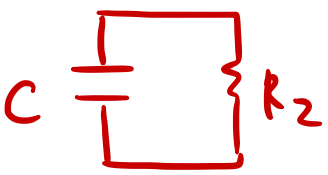
Practice :

- Energy stored on capacitor C = ?
- Energy dissipated in R_1 = ?

Second Example



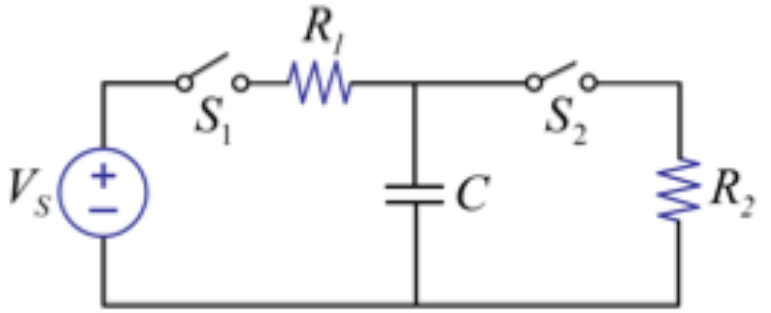
- During T_2 :
  S_2 is closed and S_1 is open.



$V_c(t = T_1) \simeq V_S$

- Initially, $V_c = V_S$
  - Energy stored on capacitor is $\frac{1}{2}CV_S^2$
- Assume $T_2 \gg R_2 \cdot C$
- Capacitor discharges more or less fully during T_2.
- Energy dissipated in R_2 during T_2 is $\frac{1}{2} C \cdot V_s^2 = E_2$ Practice
- E_2 is also independent of R_2.

Putting the Two Together



- Total energy dissipated in each cycle

$$E_{total} = E_1 + E_2 = \frac{1}{2}CV_S^2 + \frac{1}{2}CV_S^2 = CV_S^2$$

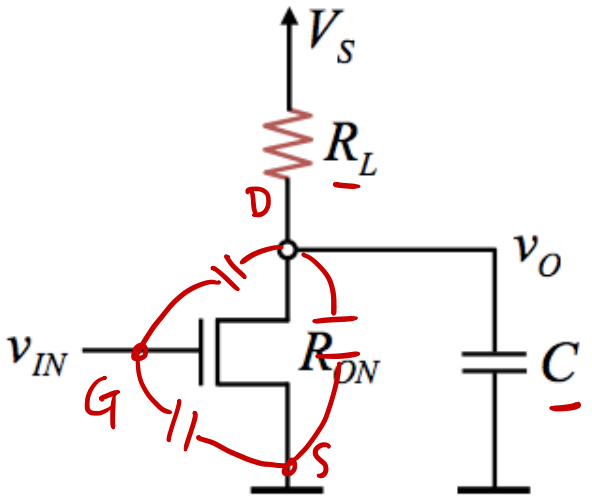
  - The energy dissipated in charging and discharging the capacitor C.
  - Assume C charges and discharges fully. $(T_1 \gg R_1 C,\ T_2 \gg R_2 C)$

- The average power is

$$\overline{P} = \frac{E_{total}}{T_1+T_2} = \frac{CV_S^2}{T_1+T_2} = \frac{CV_S^2}{T} = CV_S^2 \cdot f$$

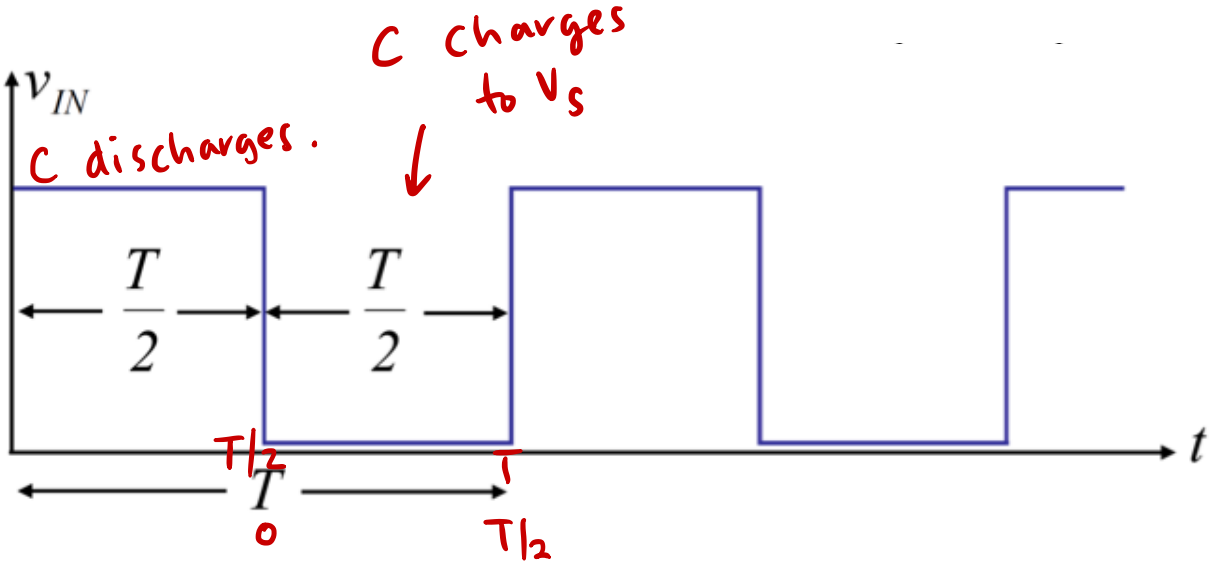
f: frequency (1/s, Hz)

Back to Our Inverter

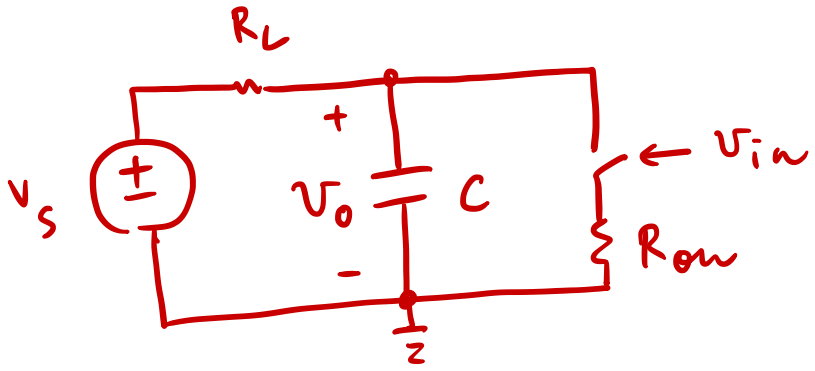


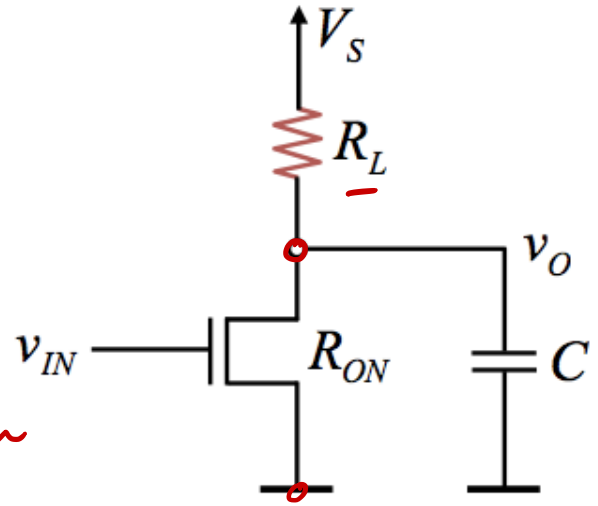
C includes
wire capacitance C_W
and gate capacitance C_{GS} of the following gates.

- What is $\overline{P}$ with the following input pattern?

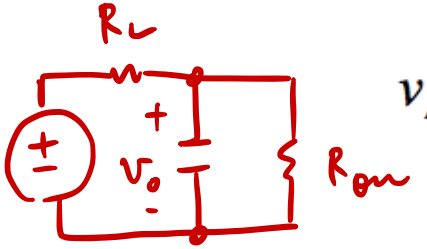


Equivalent Circuit

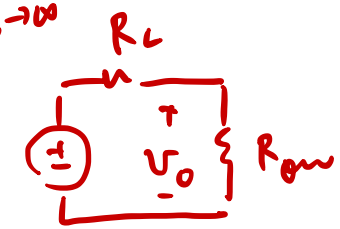




1) When v_{in} is high, discharging C.



$t \to \infty$



$V_{o,initial} = V_S$, $V_{o,final} = \frac{R_{on}}{R_L + R_{on}} \cdot V_S$

$V_{o,final} = V_S \cdot \frac{R_{on}}{R_L + R_{on}}$

$$V_o(t) = V_S \cdot \frac{R_{on}}{R_L + R_{on}} + \left(V_S - \frac{R_{on}}{R_L + R_{on}} V_S\right) \cdot e^{-t/\tau}$$

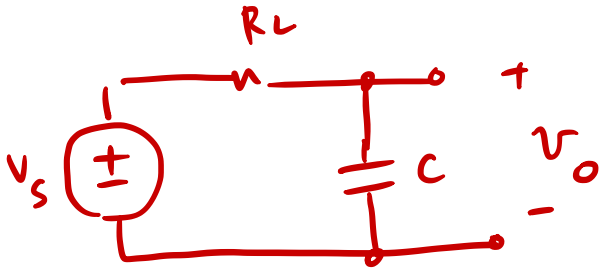
$$\tau = (R_L \| R_{on}) \cdot C$$

$$E_1 = \int_0^{T/2} \left(\frac{(V_S - V_o)^2}{R_L} + \frac{V_o^2}{R_{on}} \right) dt = \frac{V_S^2}{R_L + R_{on}} \cdot \frac{T}{2} + \frac{C \cdot V_S^2 \cdot R_L^2}{2(R_L + R_{on})^2}$$

assuming $\frac{T}{2} \gg \tau$

$$\bar{P}_1 = \frac{E_1}{T/2} = \frac{V_S^2}{R_L + R_{on}} + \frac{C V_S^2 \cdot R_L^2}{(R_L + R_{on})^2} \cdot 2f$$

2) when V_{in} is low, C charging



$$V_{o,initial} = V_S \cdot \frac{R_{on}}{R_L + R_{on}} \quad (\to 0 \text{ when } R_{on} \to 0)$$

$$V_{o,final} = V_S$$

$$V_o(t) = V_S + \left(V_S \frac{R_{on}}{R_L + R_{on}} - V_S \right) \cdot e^{-t/R_L \cdot C}$$

$$E_2 = \int_0^{T/2} \frac{(V_S - V_o)^2}{R_L} dt = \frac{C V_S^2 \cdot R_L^2}{2(R_L + R_{on})^2}$$

$$\bar{P}_2 = \frac{E_2}{T/2} = \frac{C V_S^2 \cdot R_L^2}{2(R_L + R_{on})^2} \cdot 2f$$

$e^{-(t - T/2)/R_L \cdot C}$

$\int_{T/2}^{T}$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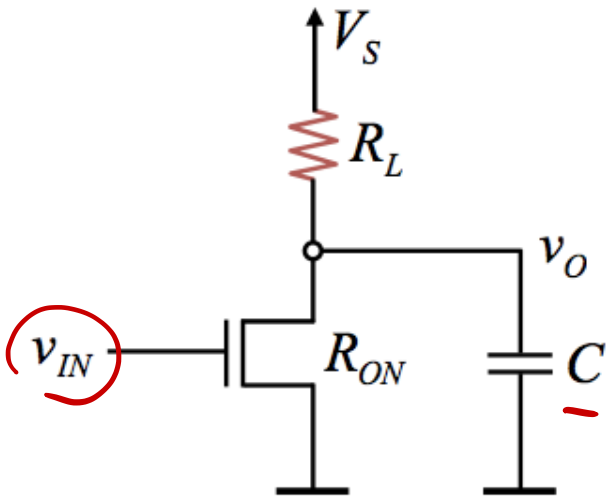
What is $\overline{P}$ for the Gate?

$$\overline{P} = \frac{V_S^2}{2(R_L + R_{ON})} + CV_S^2 f \frac{R_L^2}{(R_L + R_{ON})^2}$$

- with $R_L >> R_{ON}$, $\overline{p} = \frac{V_S^2}{2R_L} + CV_S^2 \cdot f$

Static dynamic



- During active mode, the circuit consumes static power and dynamic power.
- The first term is called the static power dissipation.
  - In both standby mode and active mode.
  - Independent of frequency f.
  - The MOSFET is ON half of the time.
- The second term is called dynamic power dissipation.
  - Proportional to frequency f and capacitance C.

of $\overline{v_{in}}$

Some Numbers

- A chip with 5 million gates running at 3 GHz. (frequency)

Assume $V_S = 5V$, $R_L = 10K\Omega$, $R_{on} \to 0\Omega$, $C = 1fF$

$$\bar{P} = \left(\frac{V_S^2}{2R_L} + CV_S^2 \cdot f\right) \cdot 5 \times 10^6$$

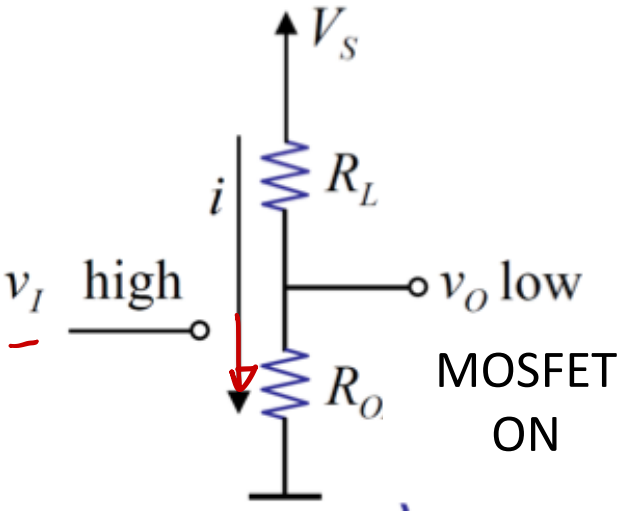
$$= \left(\frac{25}{2 \times 10^4} + 10^{-15} \times 25 \times 3 \times 10^9\right) \times 5 \times 10^6$$

$$= 6.25\,KW + 375\,KW$$

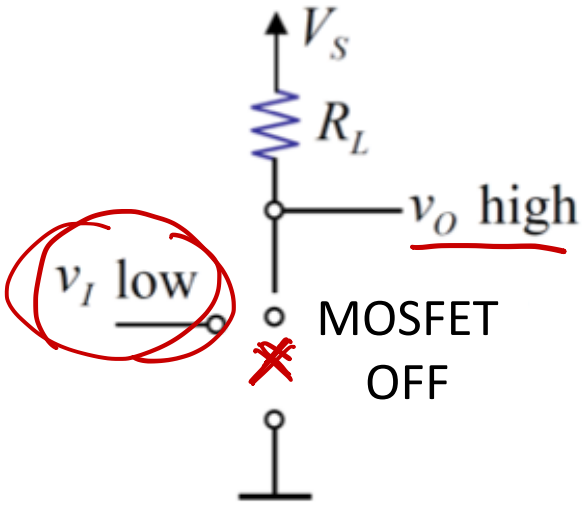
static dynamic

How to Get Rid of Static Power Dissipation?

- Intuition:

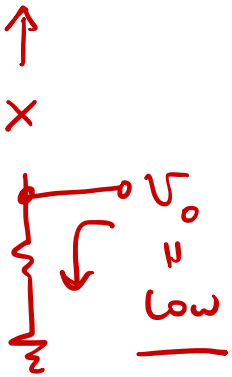


Problem case!!



no problem

V_I high



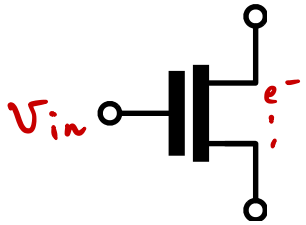
no dc path $\Rightarrow P_{static} = 0$

PMOS

CMOS : NMOS + PMOS

Complementary

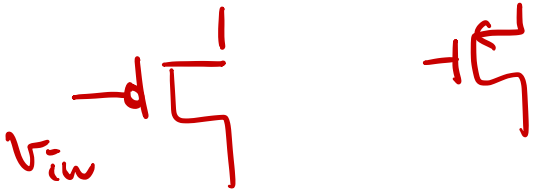
- N-channel MOSFET (NMOS)



v_{in} high, NMOS turns on (R_{on})

v_{in} low, NMOS turns off. (open, C_{off})

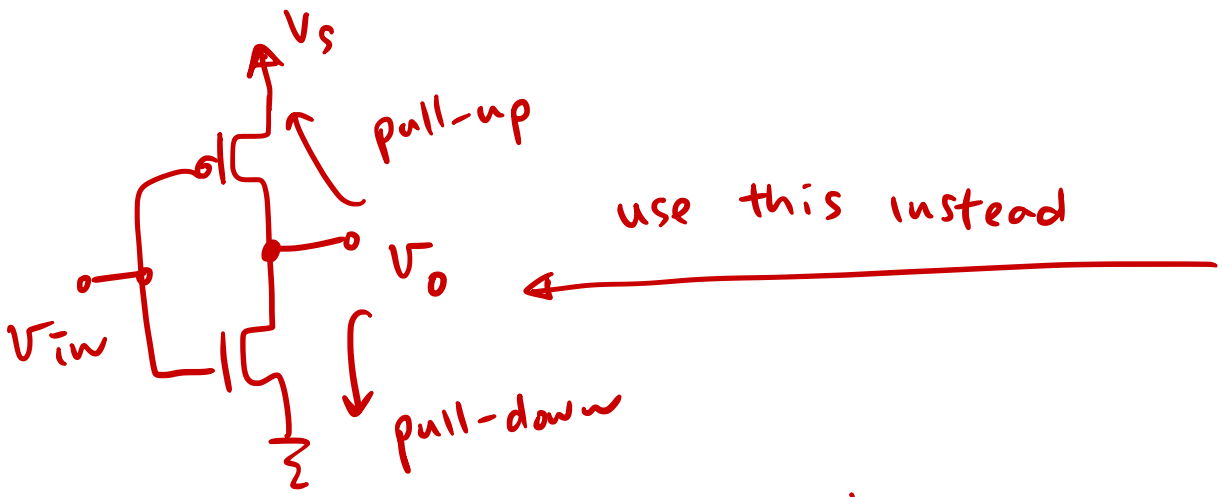
- P-channel MOSFET (PMOS)



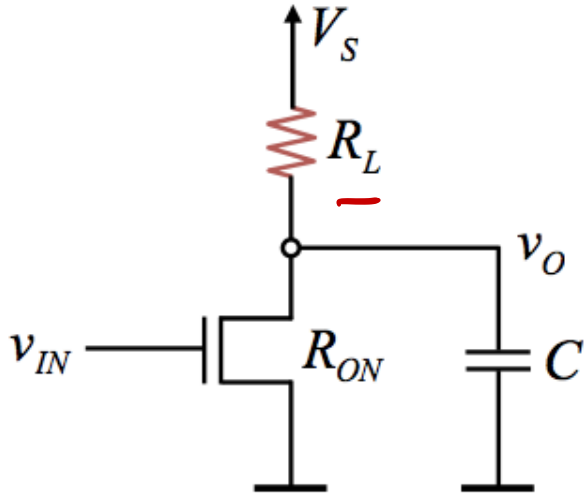
v_{in} high, PMOS turns off (open, C_{off})

v_{in} low, PMOS turns on (R_{on})

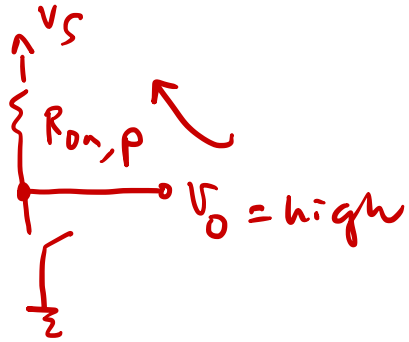
Consider This Circuit

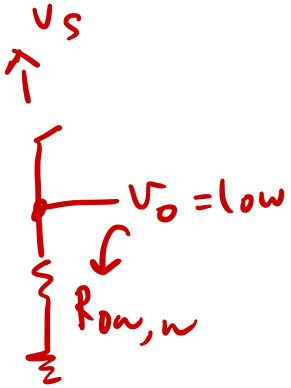


use this instead



v_{in}=high

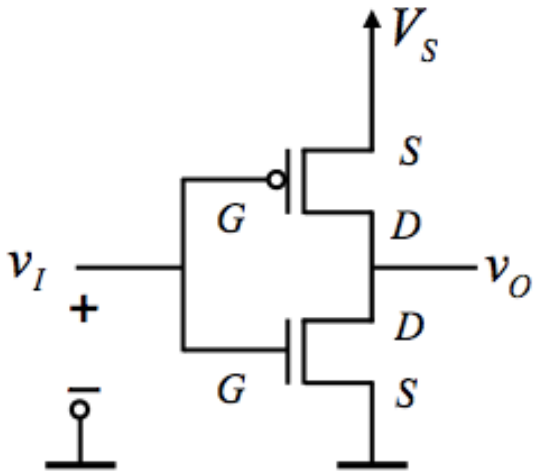




$R_{on,p} \neq R_{on,n}$

- When v_I high, pull-up path should behave like open circuit.

Behavior of the Circuit



- Input HIGH

  $v_I = 5$ V

  NMOS on
  PMOS off
  $V_o = 0$ V

Input LOW

$v_I = 0$ V

NMOS off
PMOS on
$V_o = 5$ V

(optional)

- Assume $V_{TN} = 1$ V and $V_{TP} = -1$ V

  NMOS on: $V_{in} \geq V_{TH,n}$
  NMOS off: $V_{in} < V_{TH,n}$
  PMOS on: $V_{in} \leq V_{TH,p}$
  PMOS off: $V_{in} \geq V_{TH,p}$

- Never a path from V_S to ground.
- Called complementary MOS, 'CMOS' logic.