

# The MOSFET Switches

## Key Devices Inside the Digital Gate

Chenhsin Lien and Po-Tai Cheng

CENTER FOR ADVANCED POWER TECHNOLOGIES

Dept. of Electrical Engineering

National Tsing Hua University

Hsinchu, TAIWAN

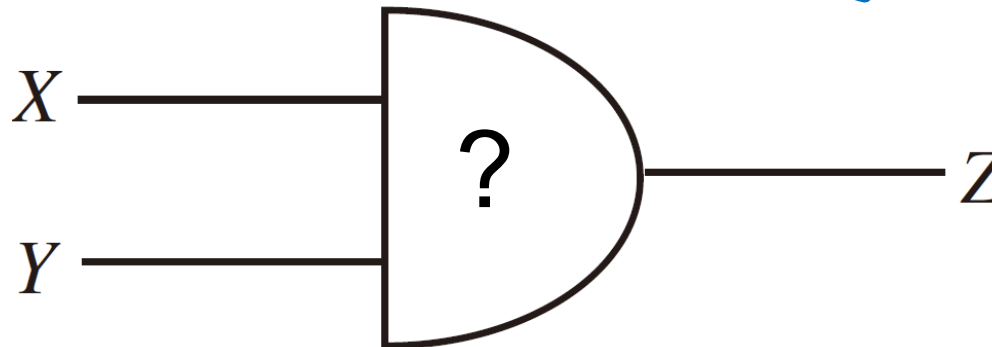


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# Inside the Digital Gate



- What kinds of elements and the circuits are inside the digital gate?

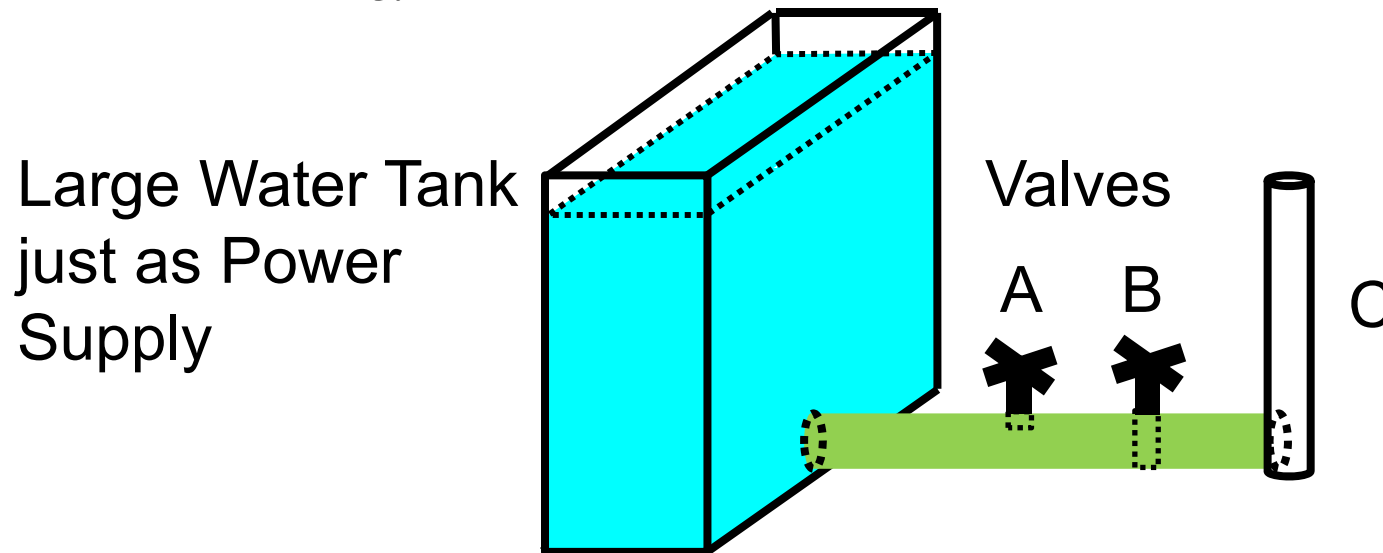


$$Z = X \cdot Y$$

# How to build an AND gate



- Water Analogy

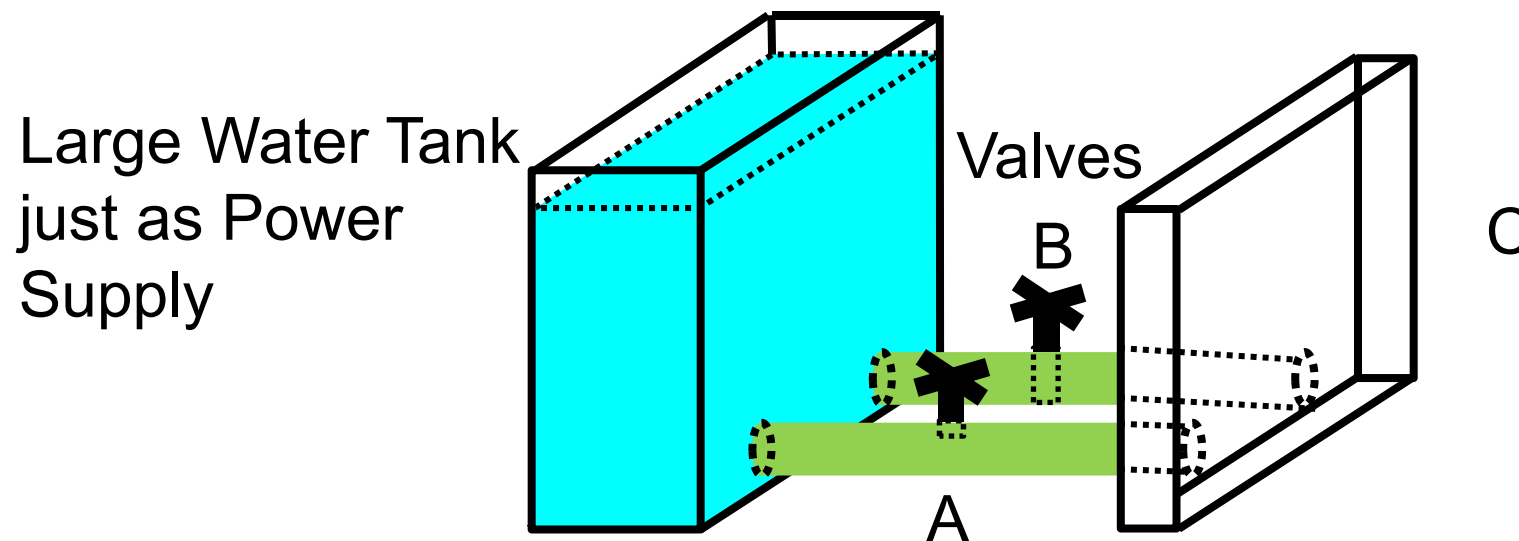


- If A is open AND B is open, then C has water else C has no Water.
- Similarly, we can use this insight to build an AND gate.

# How to build an OR gate



- Water Analogy

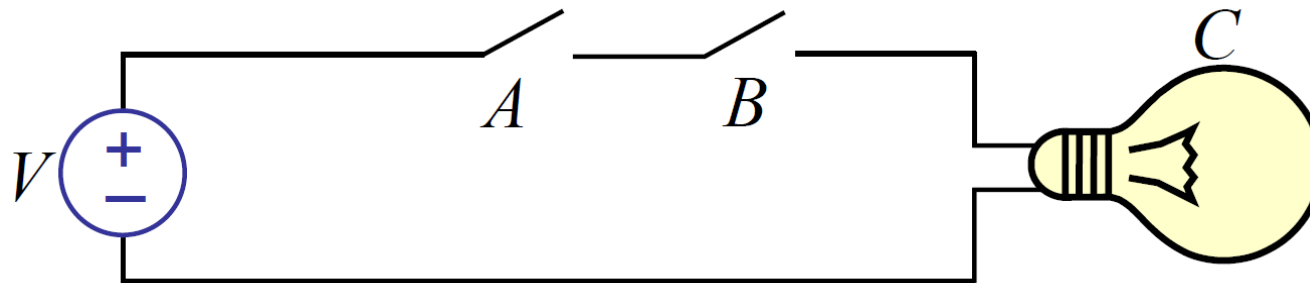


- If A is open OR B is open, then C has water else C has no Water.
- Similarly, we can use this insight to build an OR gate.

# How to build an AND gate



- Electrical Analogy

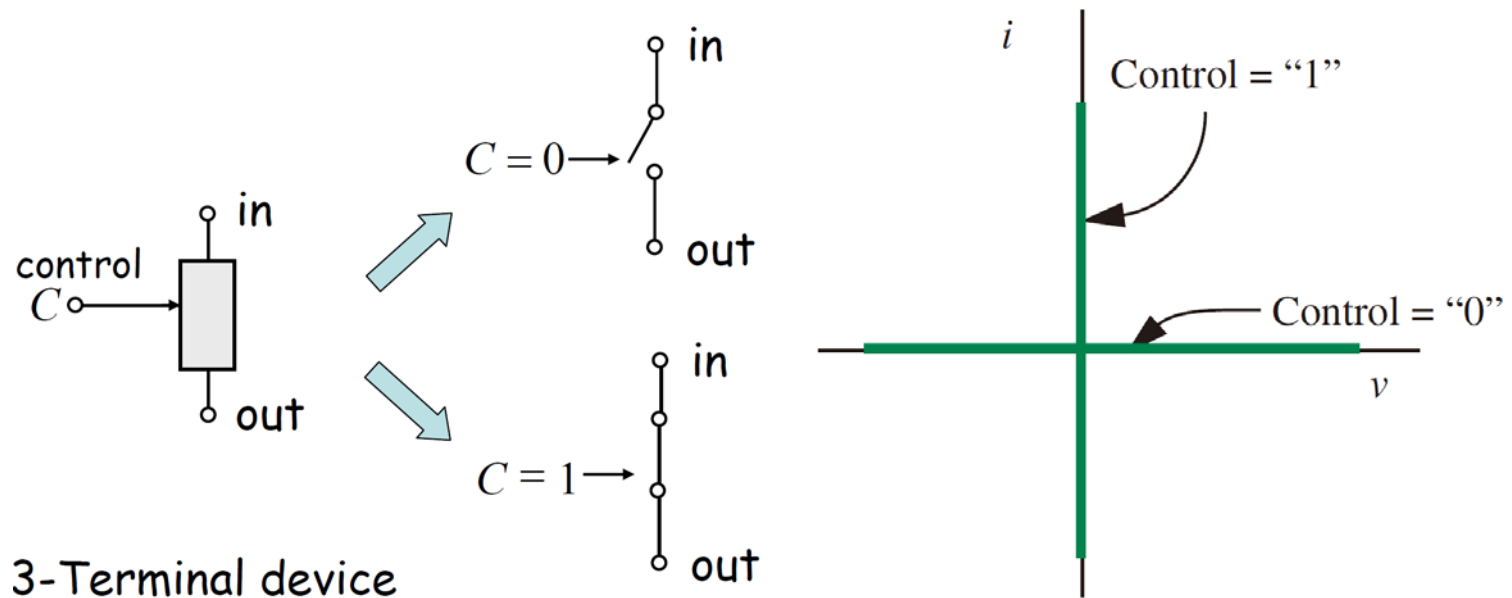


- If  $A$  is closed AND  $B$  is closed, then  $C$  is lighted else  $C$  is darken.
- *Switch* is the *Key device*.

# The Three-terminal Switch



- Three-terminal switch model.

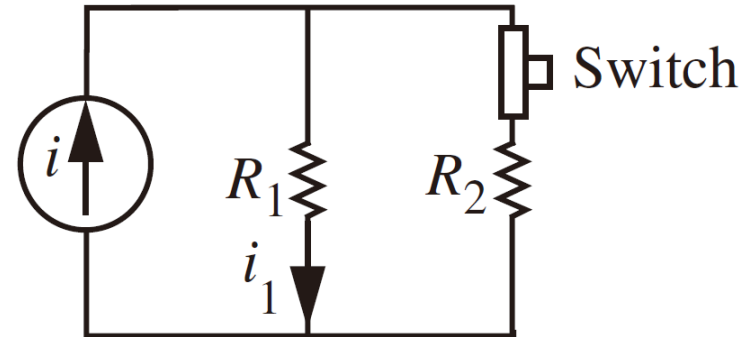


- If  $C = 1$ , *short circuit* between in and out, else ( $C = 0$ ) *open circuit* between in and out.
- For mechanical switch, Control (C) means the mechanical pressure.

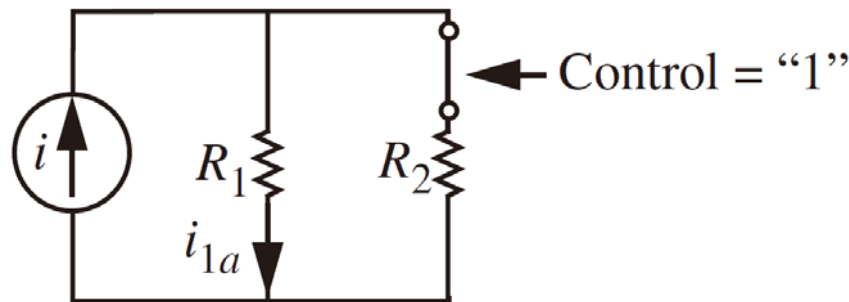


# Example

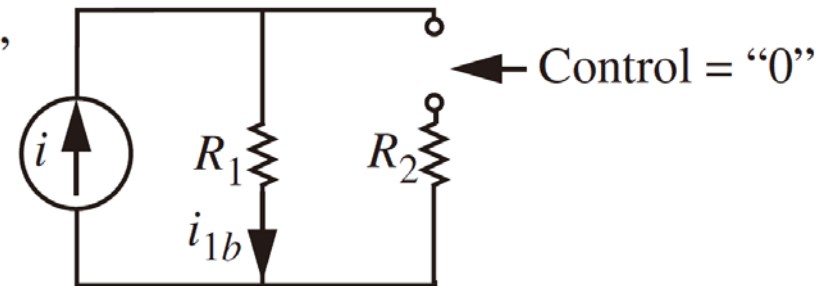
- Find the current through  $R_1$ .



- If  $C = 1$ ,  $R_2$  is connected to the circuit. If  $C = 0$ ,  $R_2$  is disconnected from the circuit.



- $$i_{1a} = \frac{R_2}{R_1 + R_2} I$$

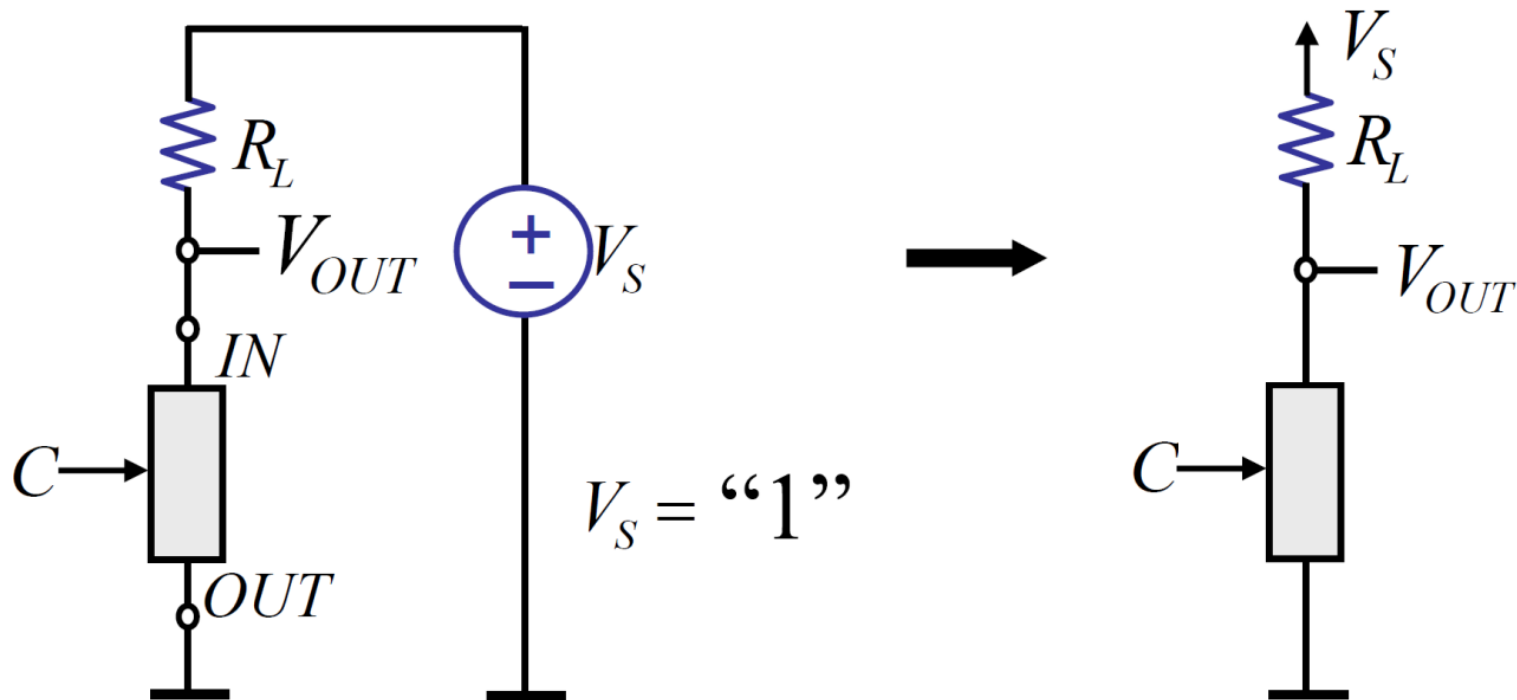


$$i_{1b} = I$$



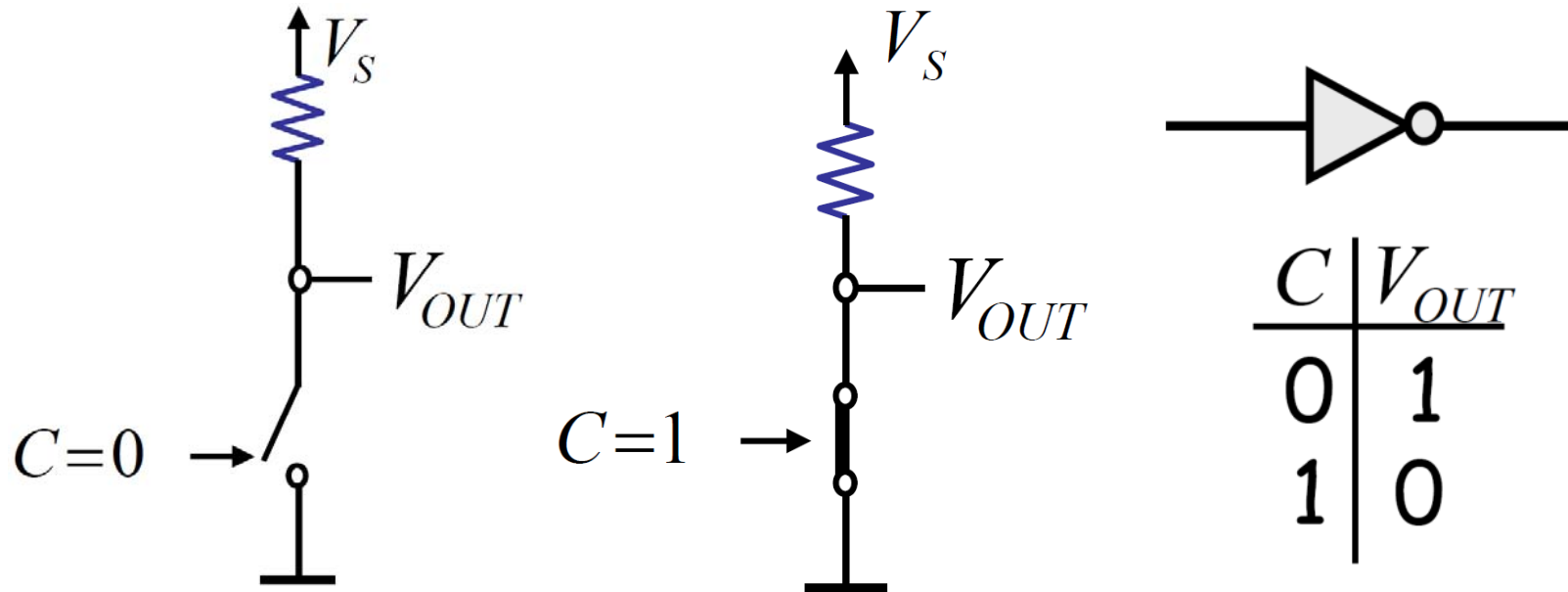
# Logic Function Using Switches

- The Inverter Circuit.
- This is a very common circuit topography which we will encounter over and over again. We have a special short hand for this kind of circuit.



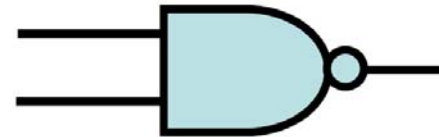
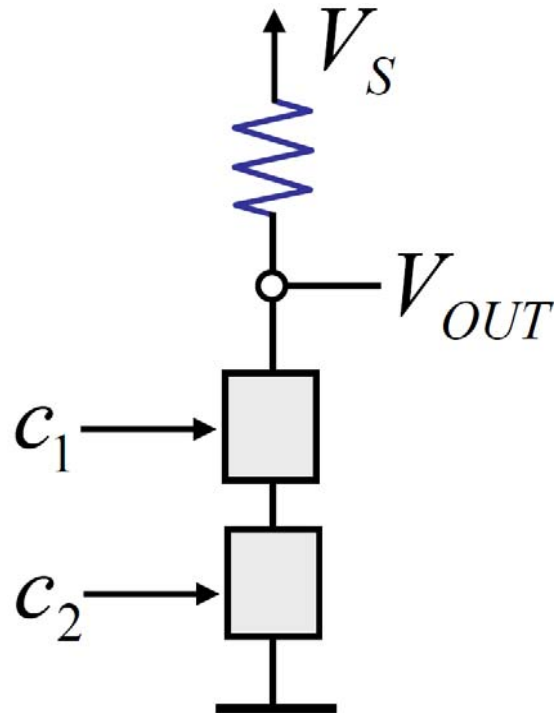


# The Inverter



If  $C = 0$ , then  $V_{out} = 1$   
else ( $C = 1$ )  $V_{out} = 0$ .

# The NAND Gate

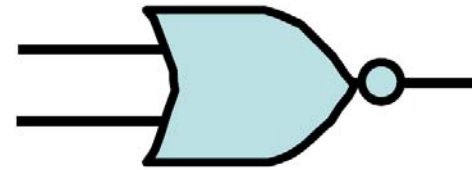
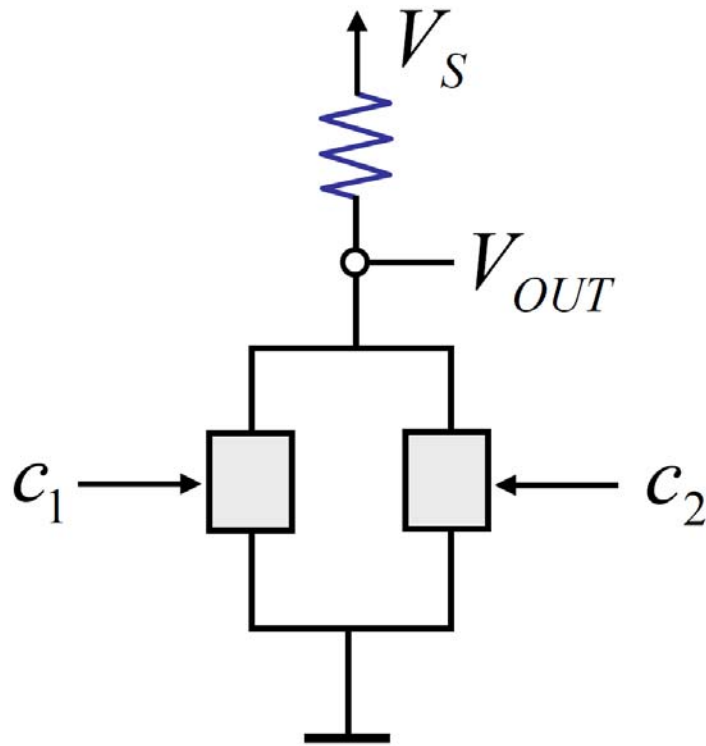


$c_1$	$c_2$	$V_O$
0	0	1
0	1	1
1	0	1
1	1	0

If  $c_1 = 1$  AND  $c_2 = 1$  , then  $V_{out} = 0$   
Else  $V_{out} = 1$ .



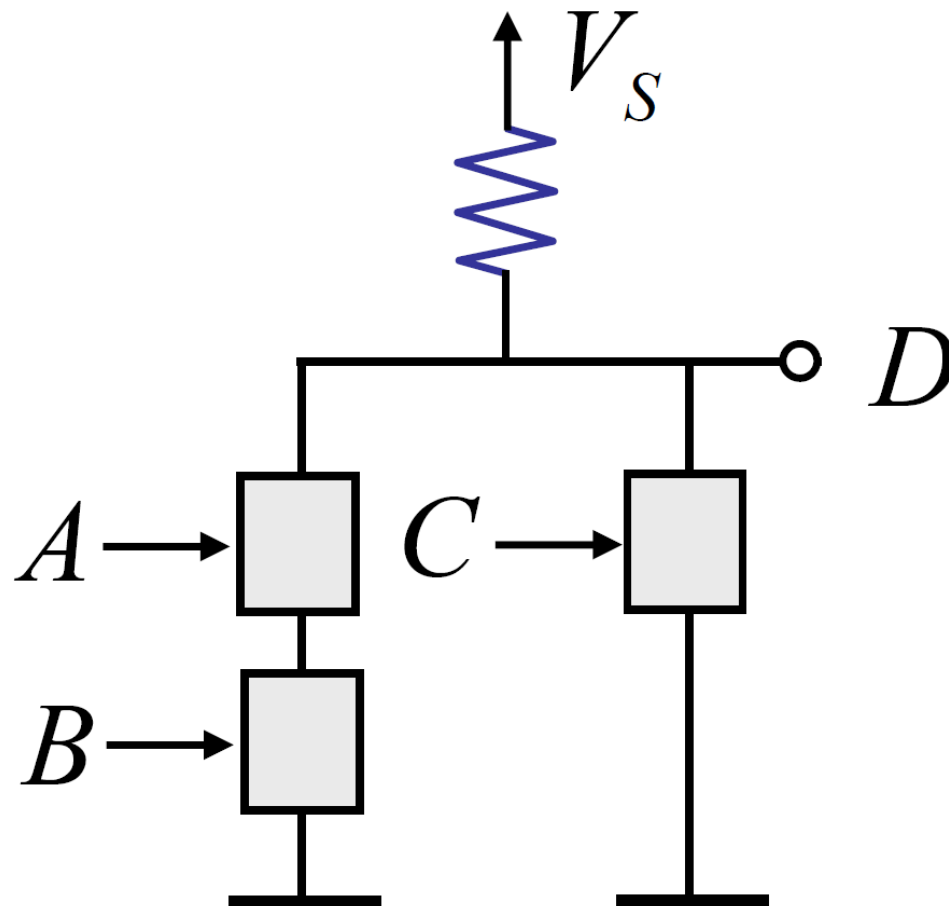
# The NOR Gate



$c_1$	$c_2$	$V_o$
0	0	1
0	1	0
1	0	0
1	1	0

If  $c_1 = 0$  AND  $c_2 = 0$  , then  $V_{out} = 1$   
Else  $V_{out} = 0$ .

# A Complex Gate

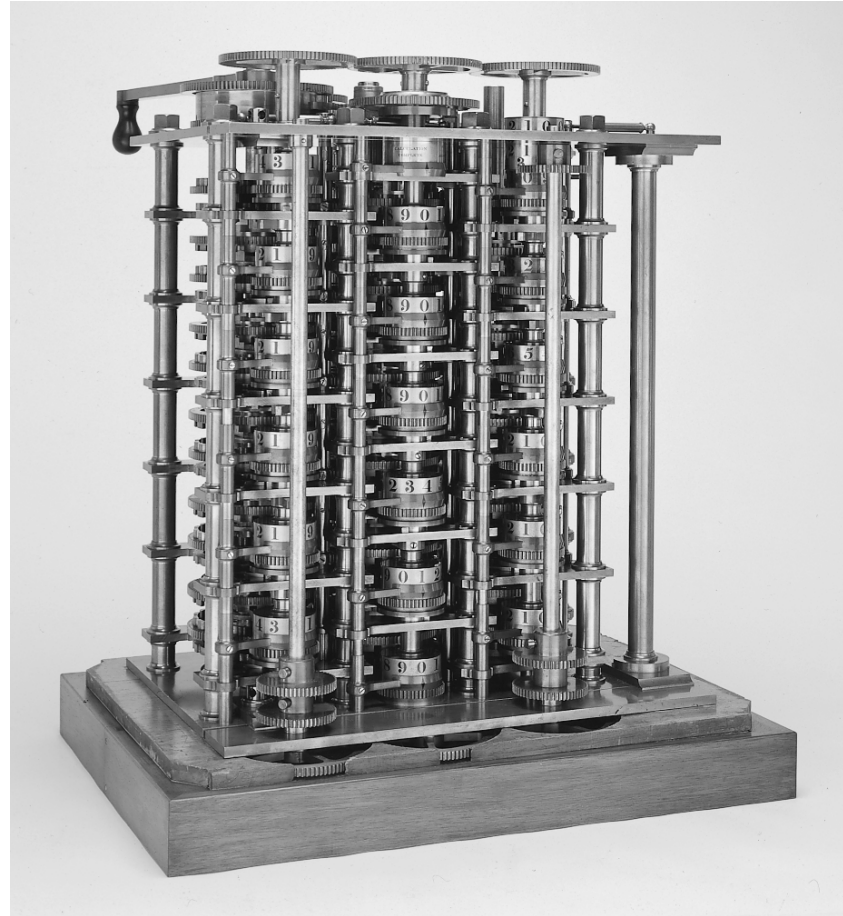


$$D = \overline{(A \cdot B) + C}$$

# The Babbage Difference Engine

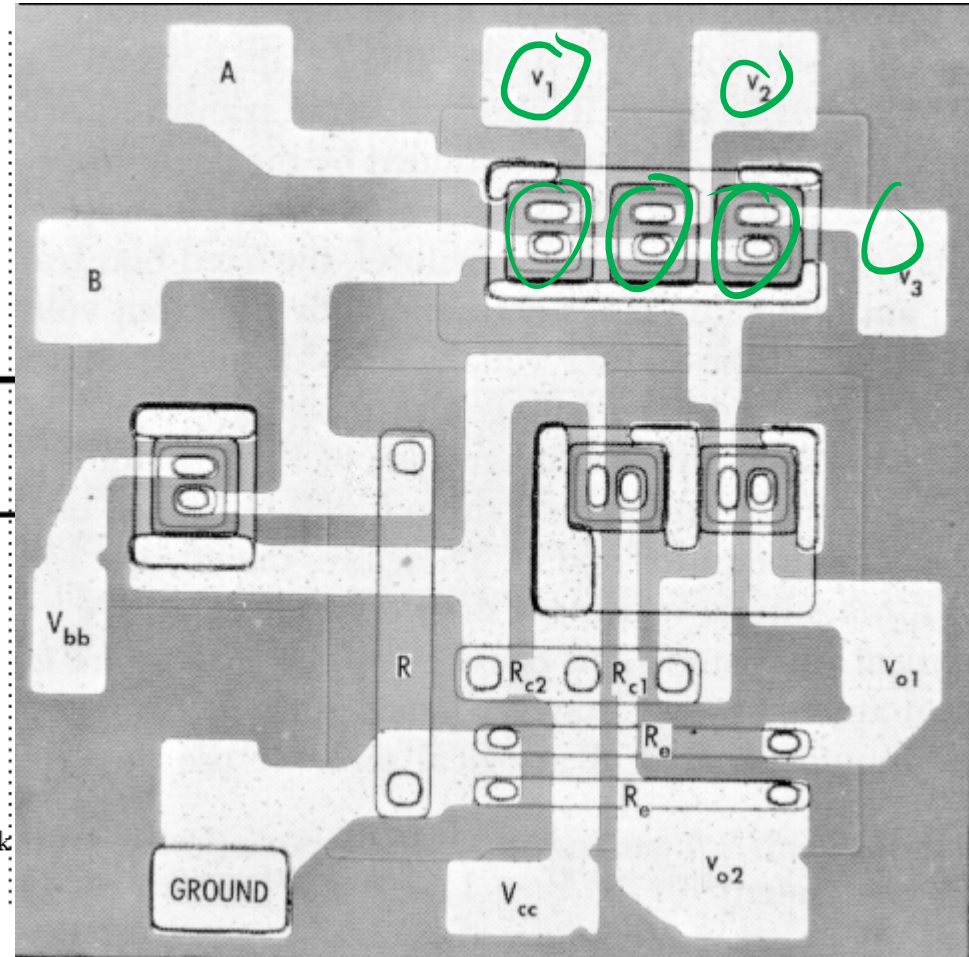
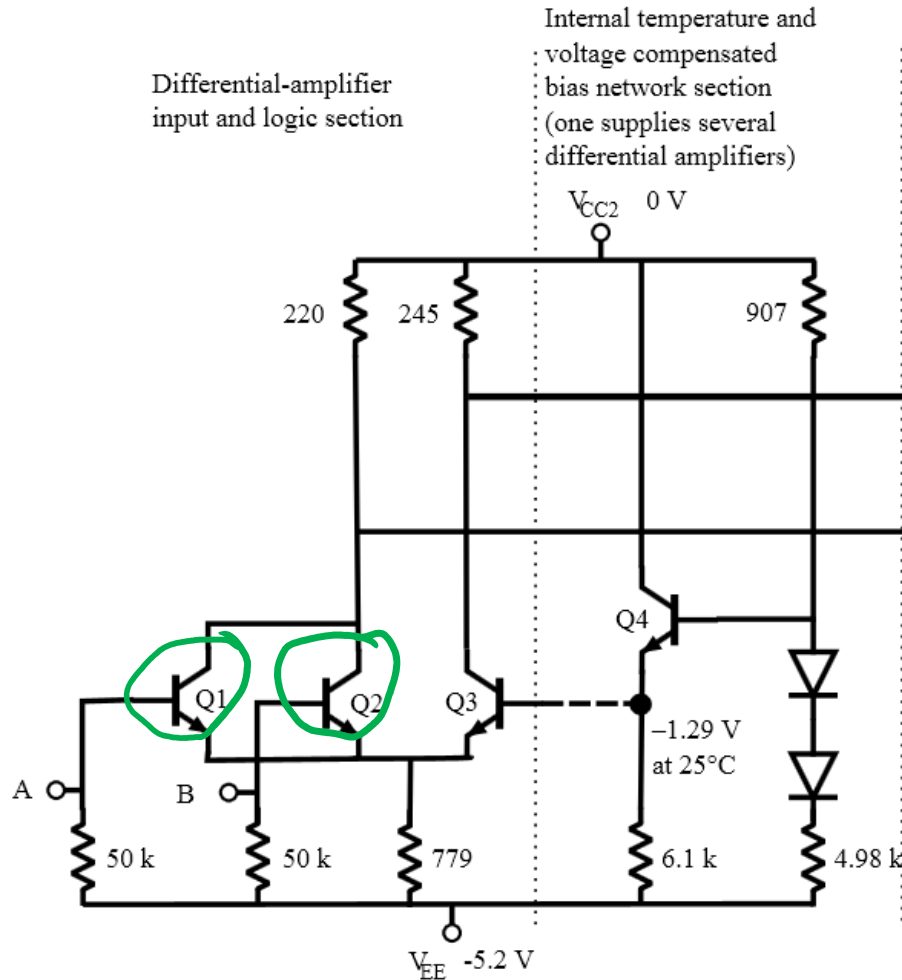


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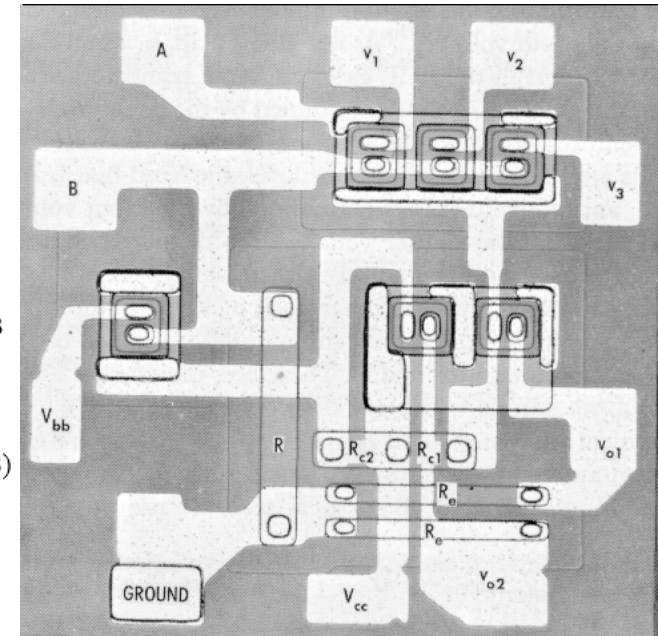
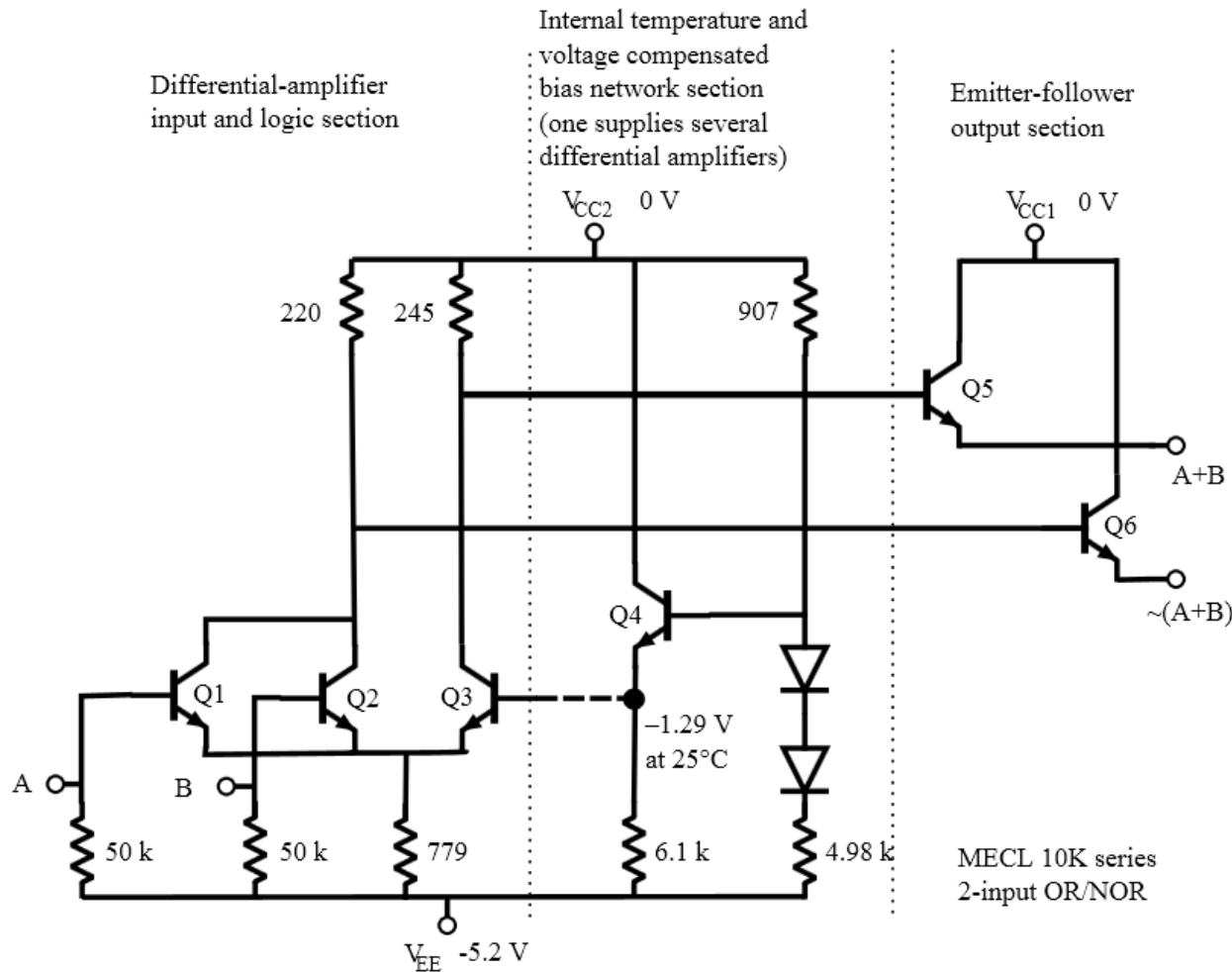
- 25,000 parts, cost: £17,470

# 3 Input NOR Gate



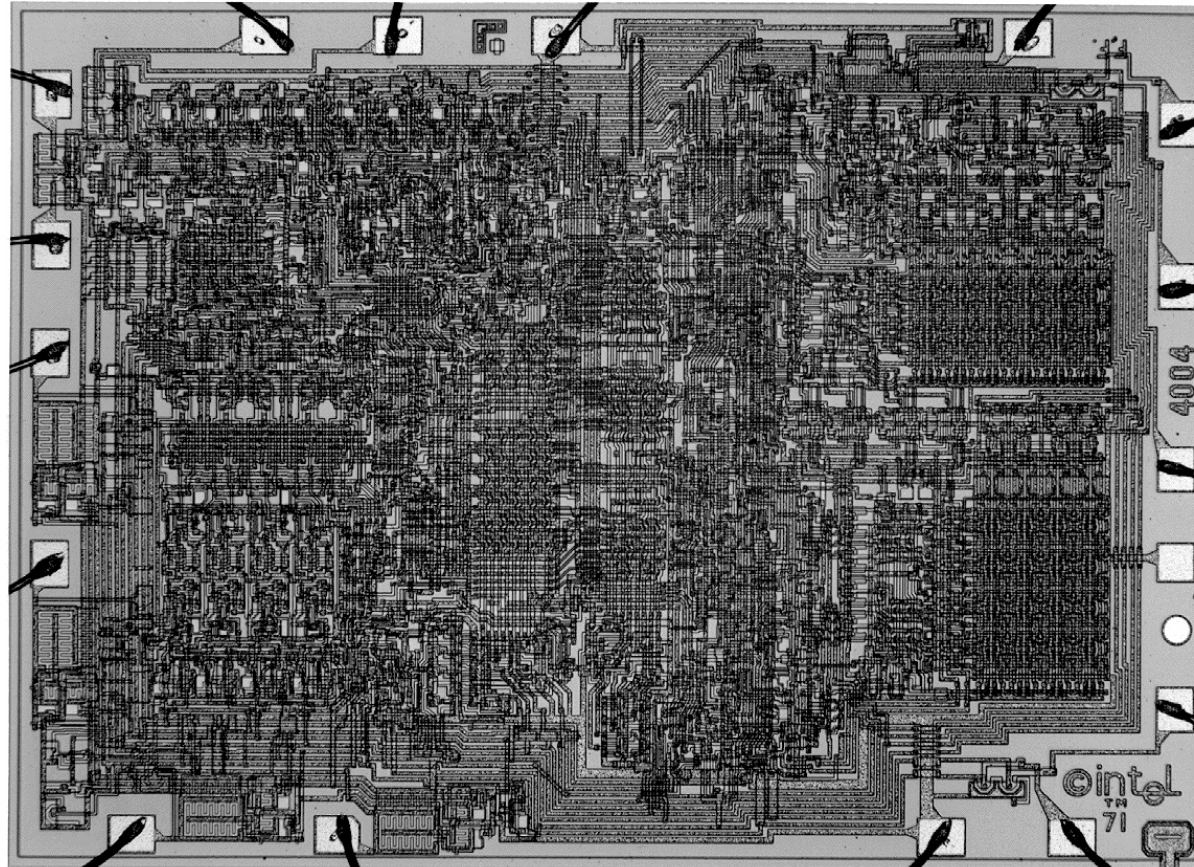
- Bipolar logic, 1960's, ECL 3-input NOR Gate, Motorola 1966

# 3 Input NOR Gate



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# Intel 4004 Microprocessor



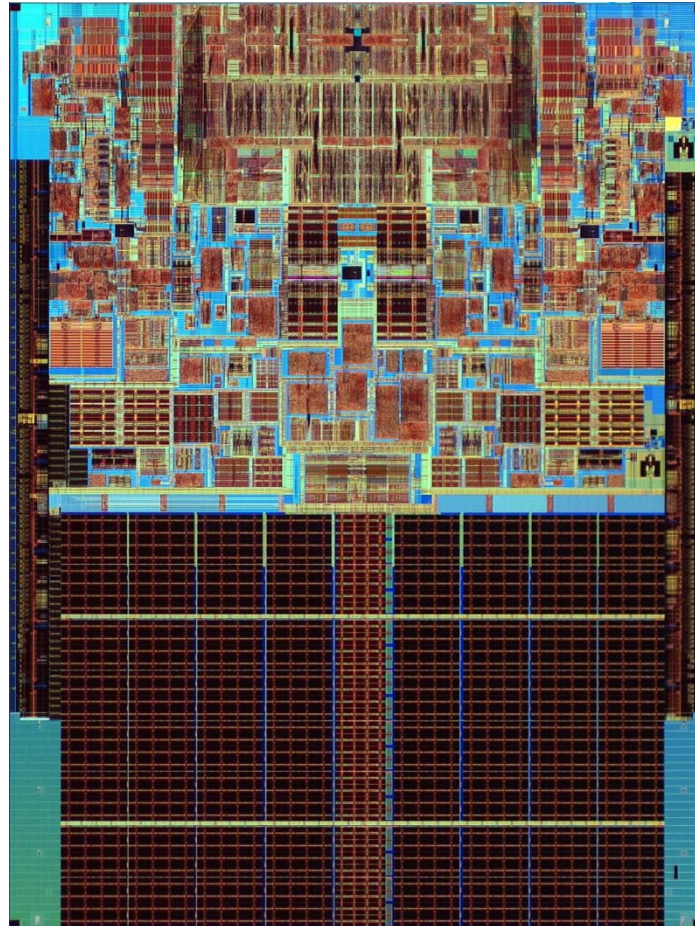
- Intel, 1971, 2,300 transistors ( $12\text{mm}^2$ ), 740 KHz operation, ( $10\mu\text{m}$  PMOS technology)



# Intel Core 2 Microprocessor



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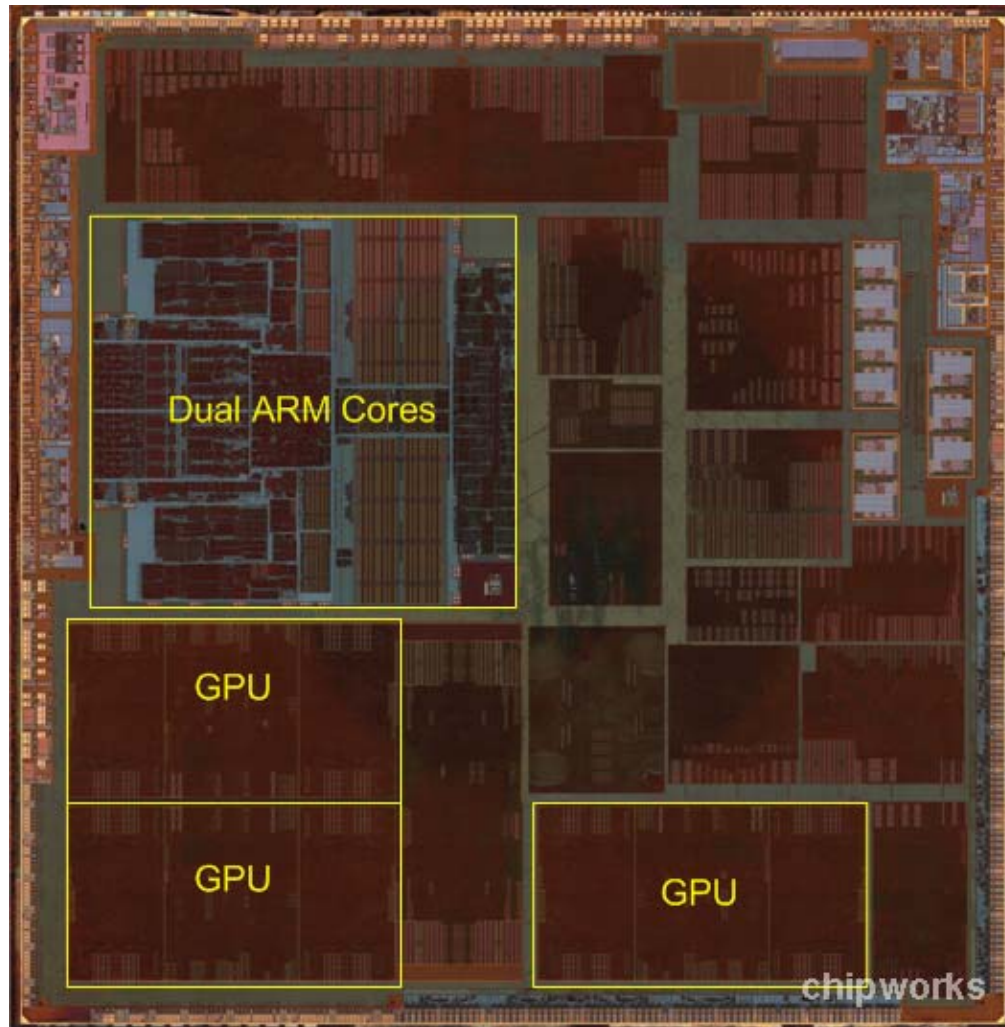


- Intel, 2006, 291,000,000 transistors, (143mm<sup>2</sup>), 3 GHz operation, (65nm CMOS technology)

# Apple A6 Microprocessor



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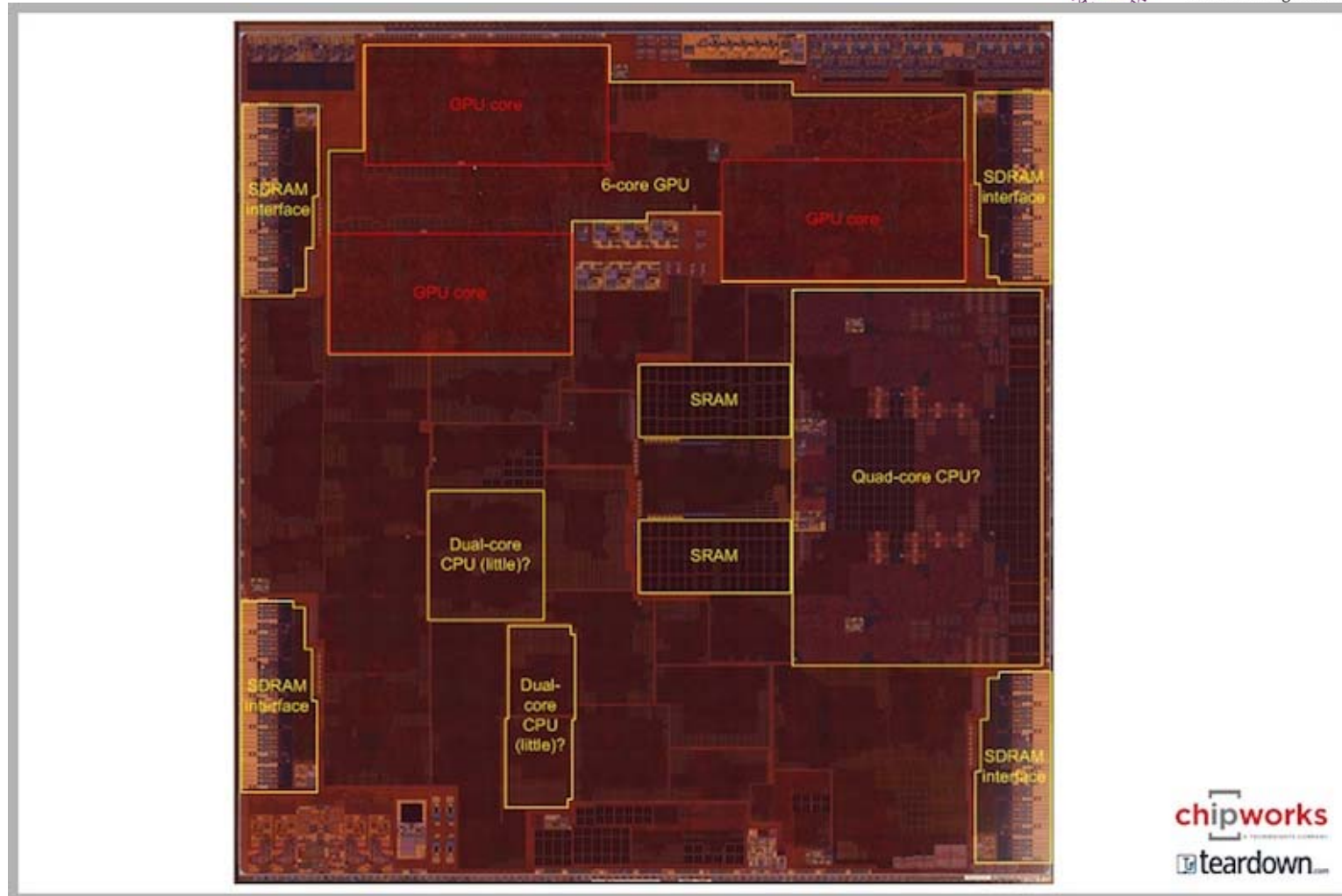


- Apple, 2012, (96.7mm<sup>2</sup>), (32nm CMOS technology)

# Apple A10 Microprocessor



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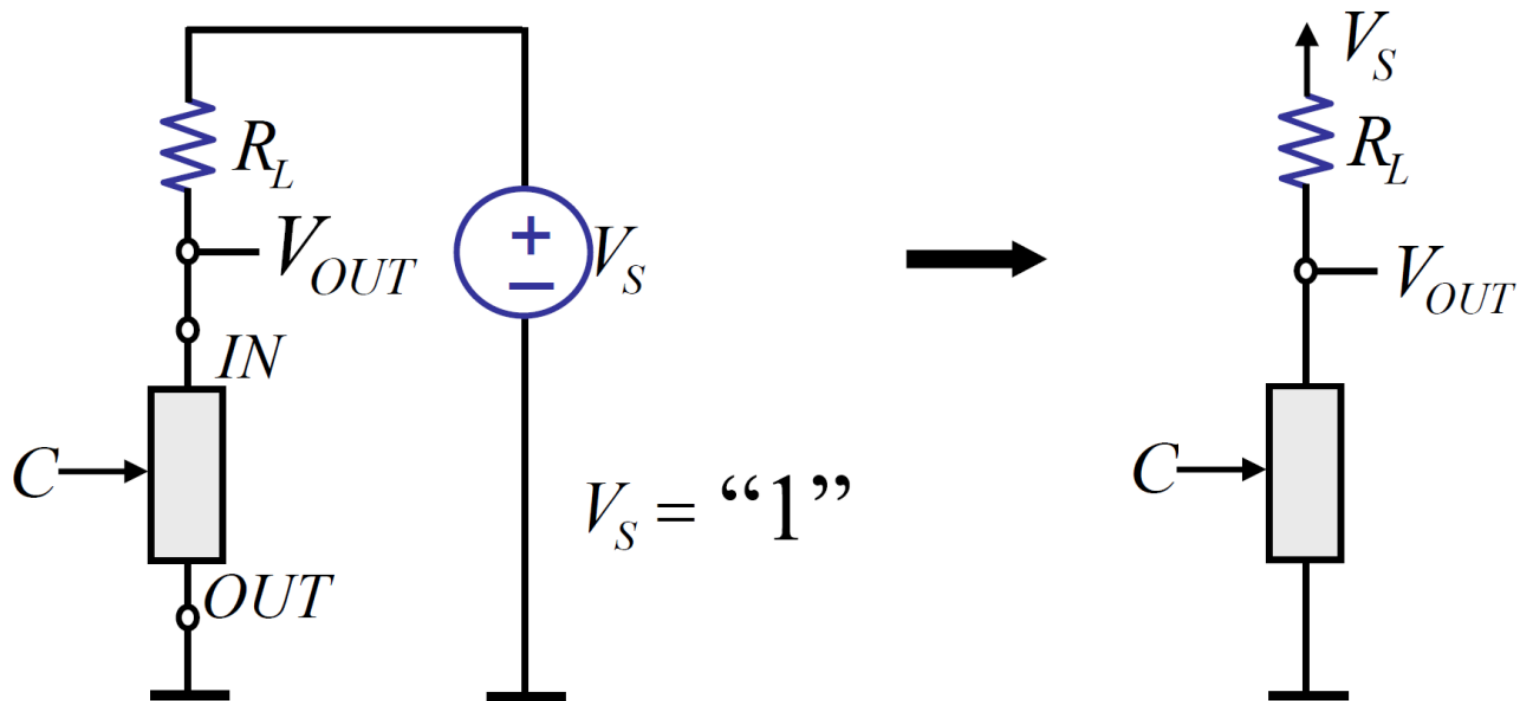
chipworks  
teardown

- Apple, 2016, (125 mm<sup>2</sup>), (16nm FinFET CMOS technology)

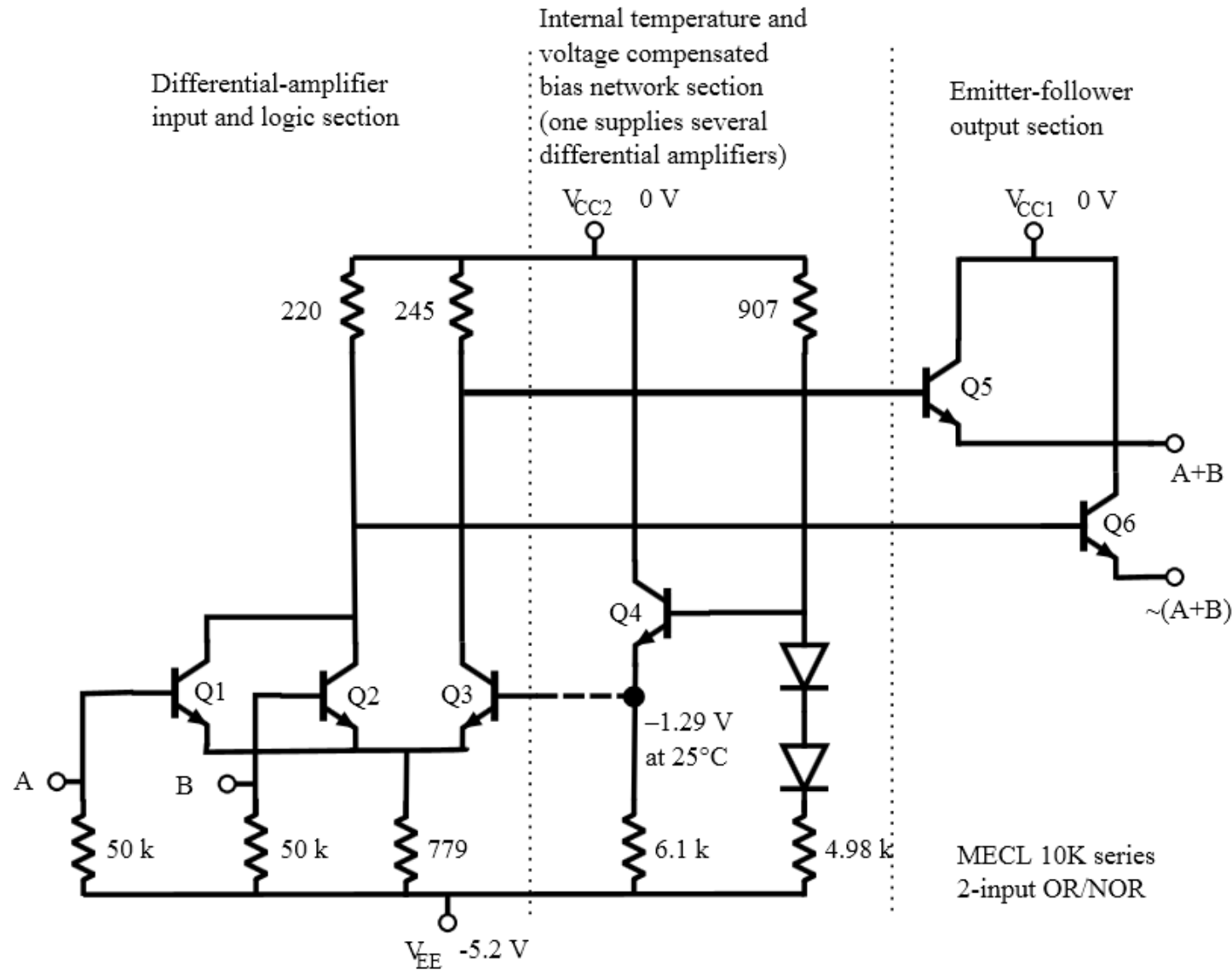


# Logic Function Using Switches

- The Inverter Circuit.
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# 3 Input NOR Gate



- iBpolar logic, 1960's, ECL 3-input NOR Gate, Motorola 1966

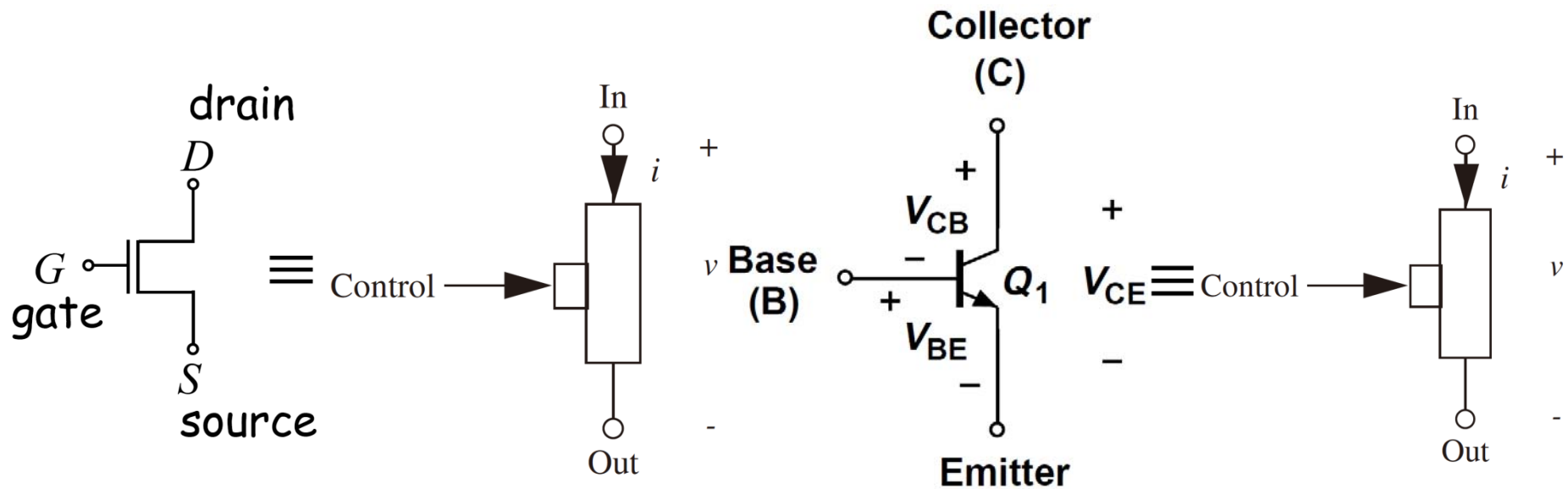
# The Semiconductor Switches



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- Two kinds of semiconductor switches: MOSFET and BJT
- Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)
- Bipolar Junction Transistor (BJT)

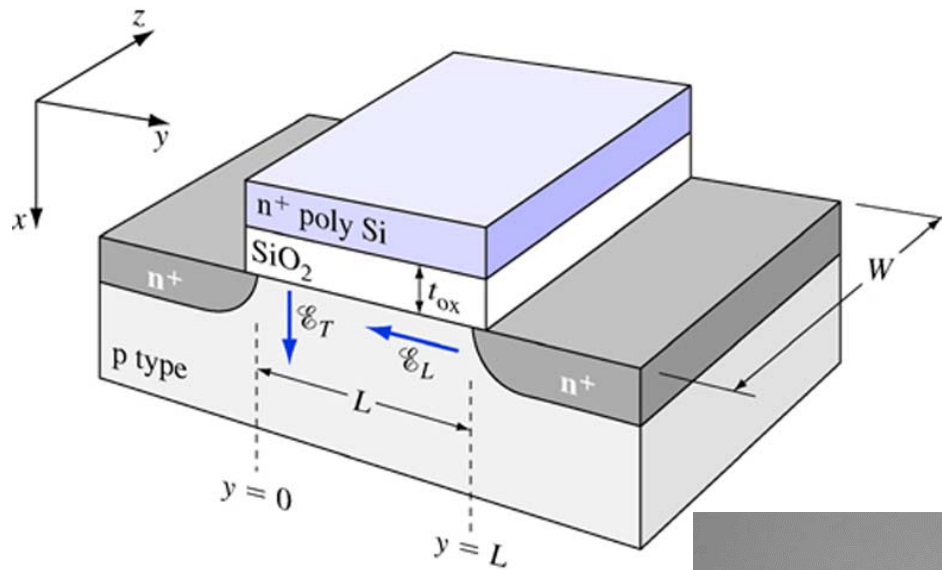


MOSFET

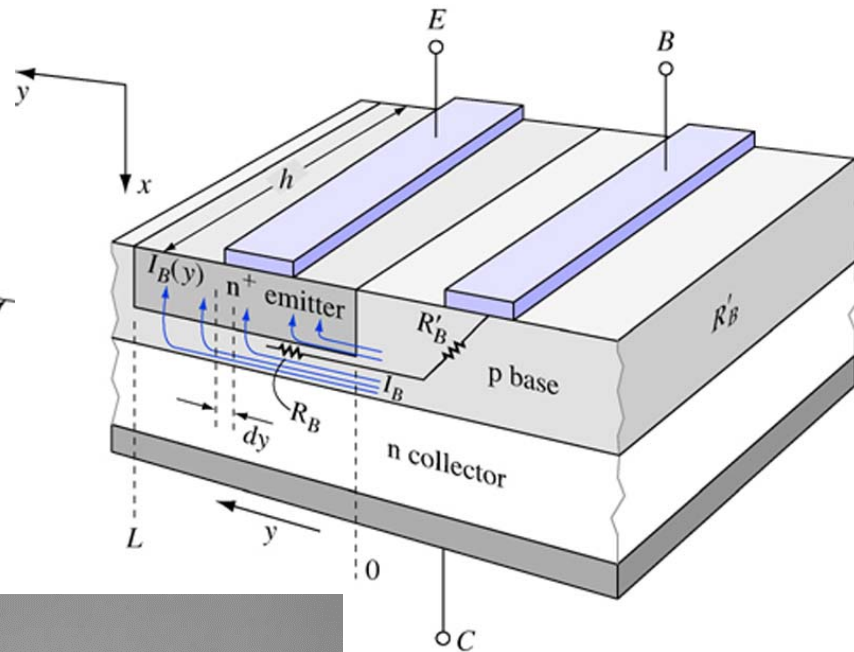
BJT

- 3 terminal lumped element behaves like a switch with Gate (G) or Base (B) as control terminal and Drain (D) to Source (S) or Collector (C) to Emitter (E) as in and out port.

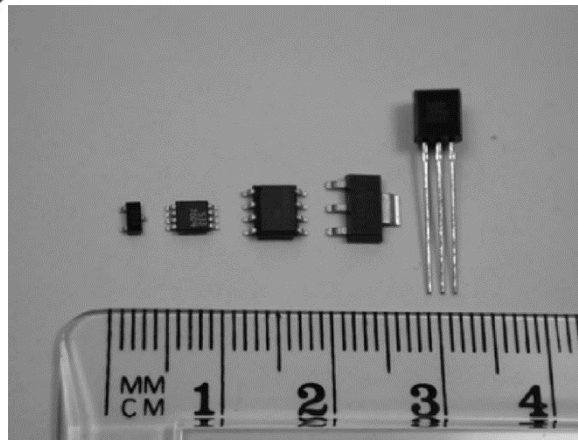
# The BJT and MOSFET



MOSFET



BJT

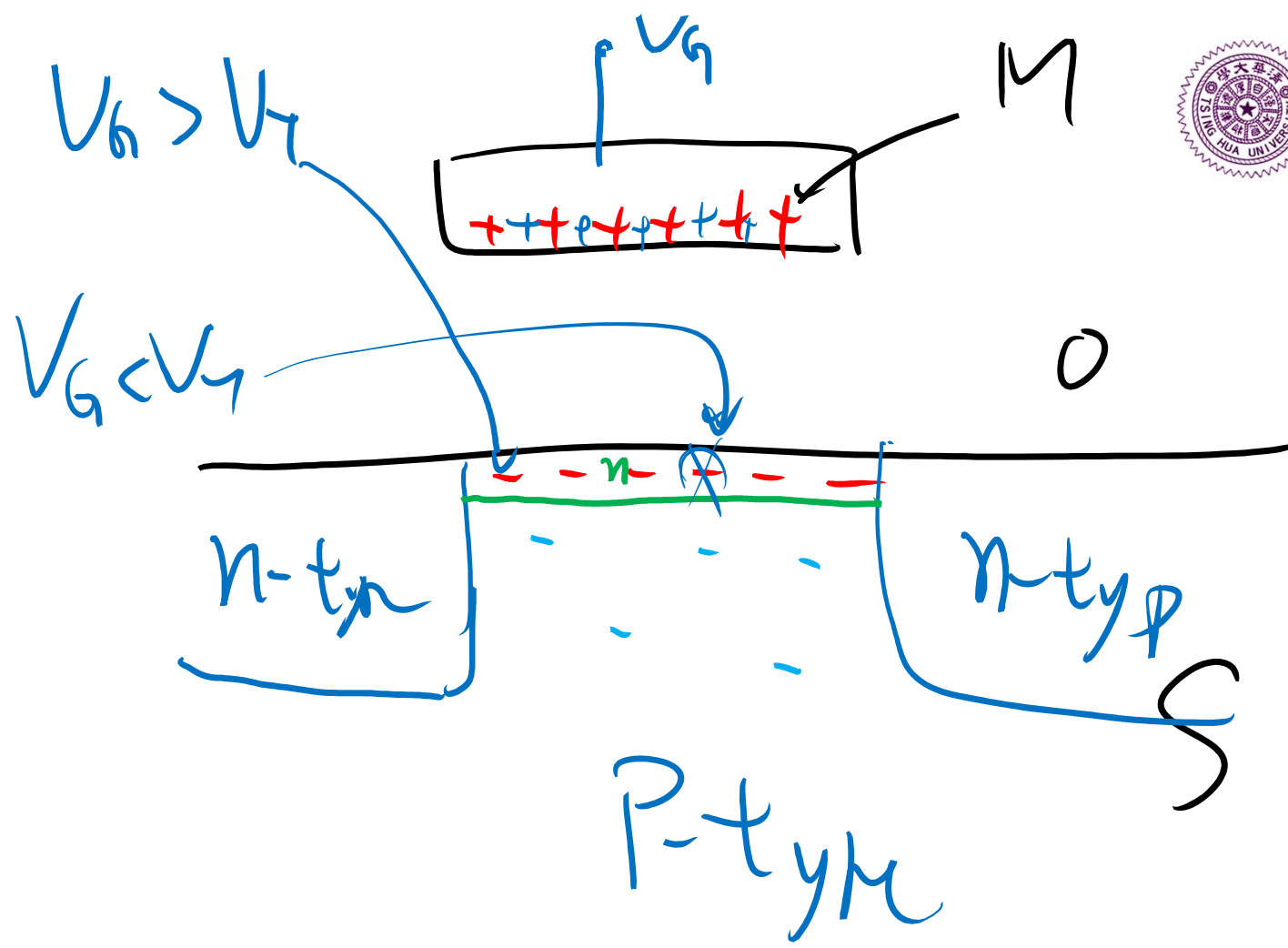




P-type

n-type



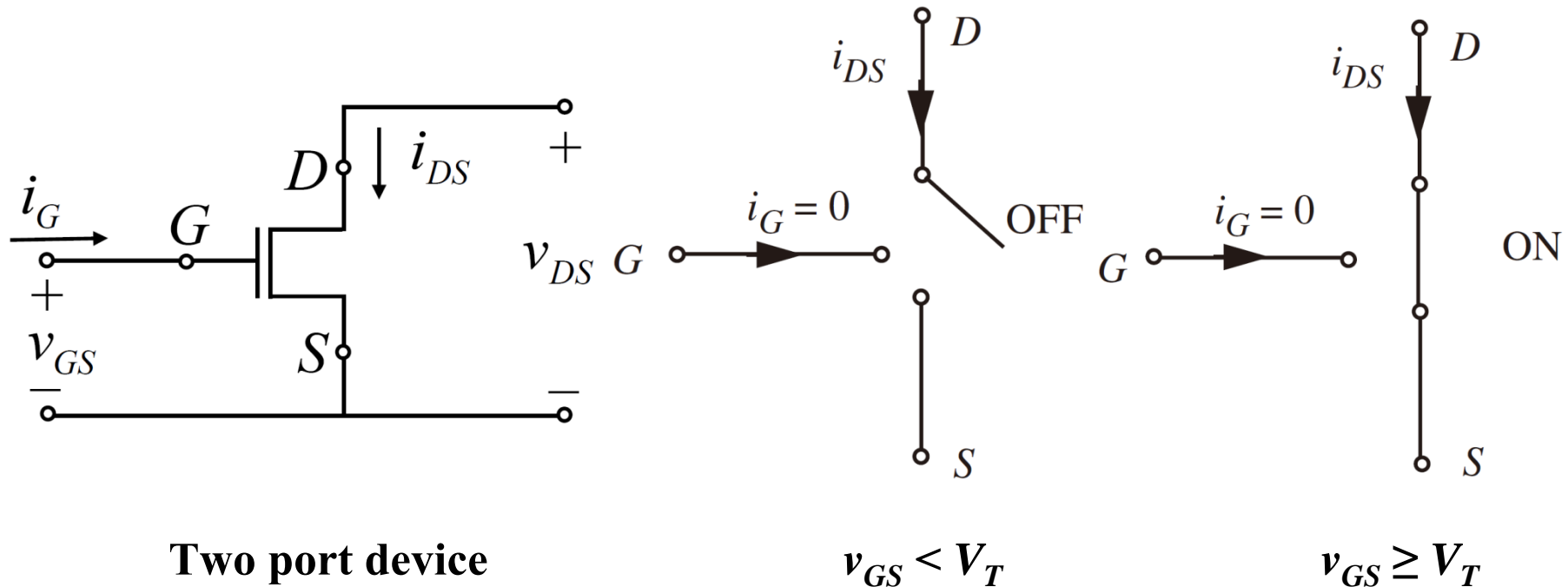


1. 5. 4. 2.



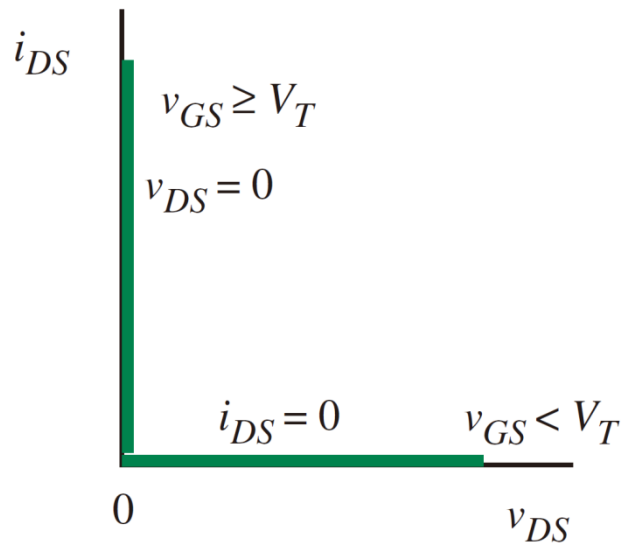
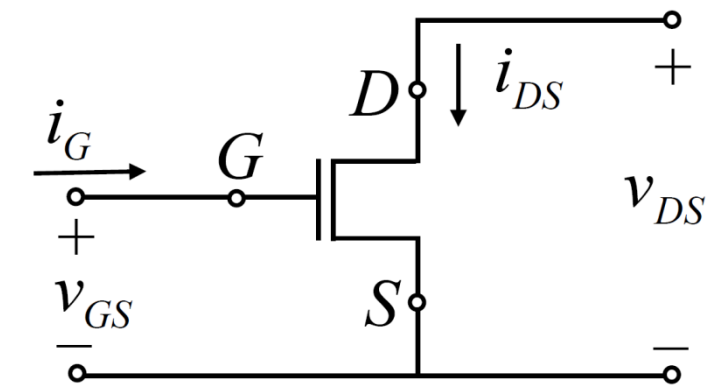
# Switch model (S model) of the MOSFET

- Port Representation: Understand the operation of MOSFET by viewing it as a two-port element.

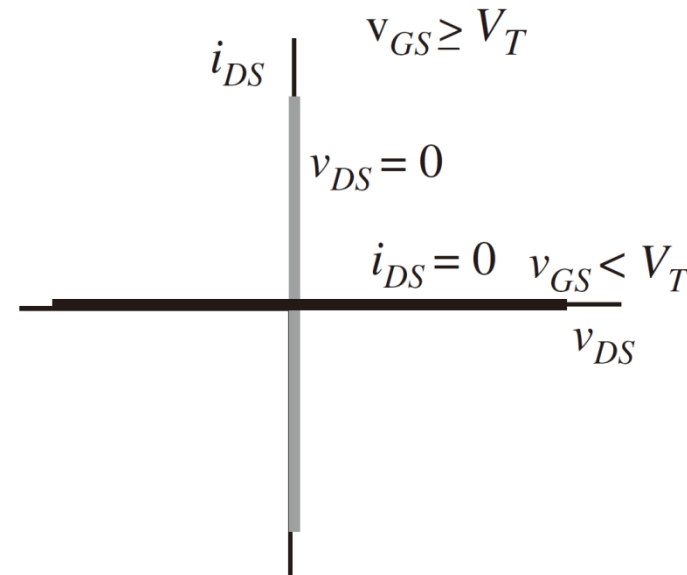




# Switch model (S model) of the MOSFET



MOSFET  $i$ - $v$  characteristics

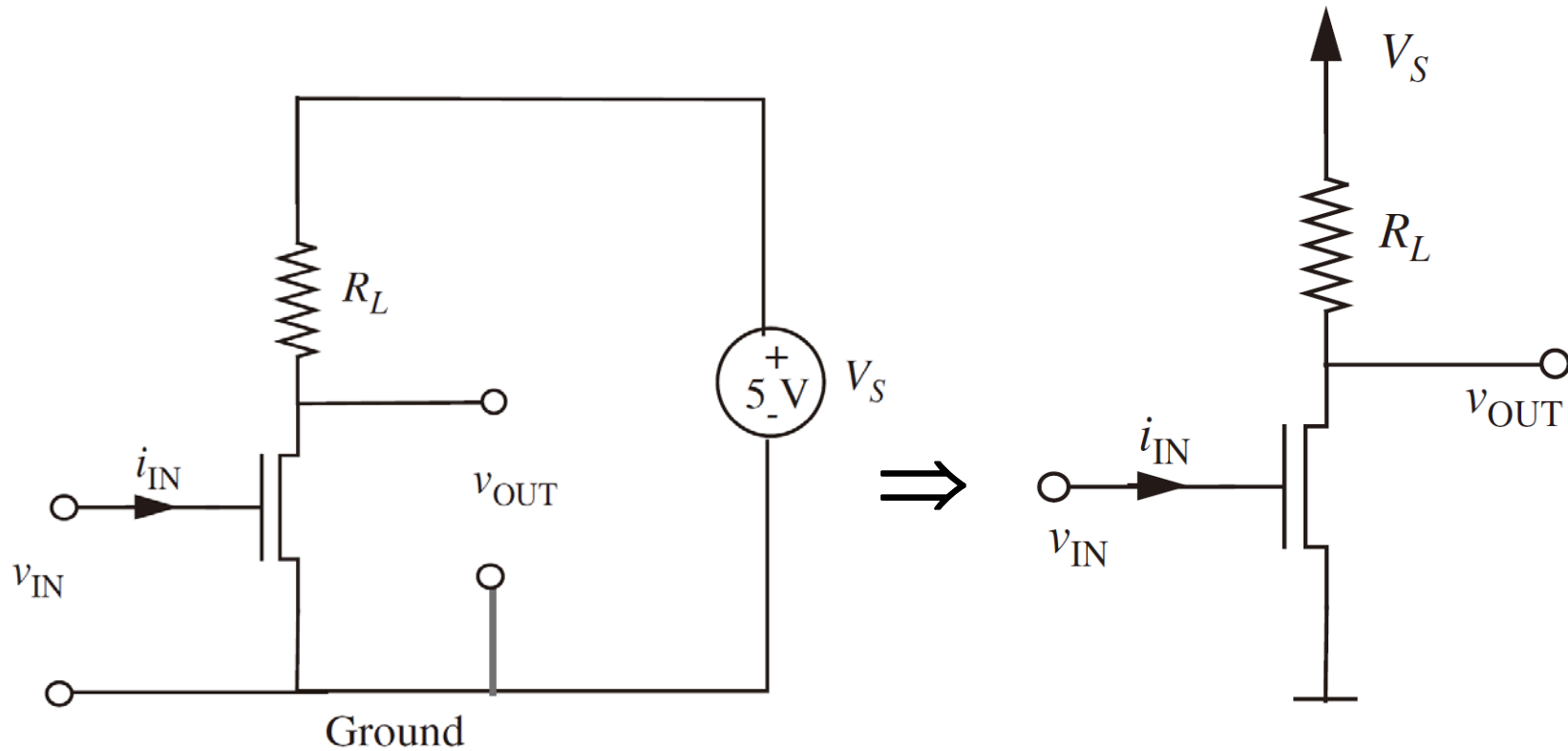


For  $v_{GS} < V_T$ ,  $i_{DS} = 0$   
and  
For  $v_{GS} \geq V_T$ ,  $v_{DS} = 0$



# The MOSFET inverter

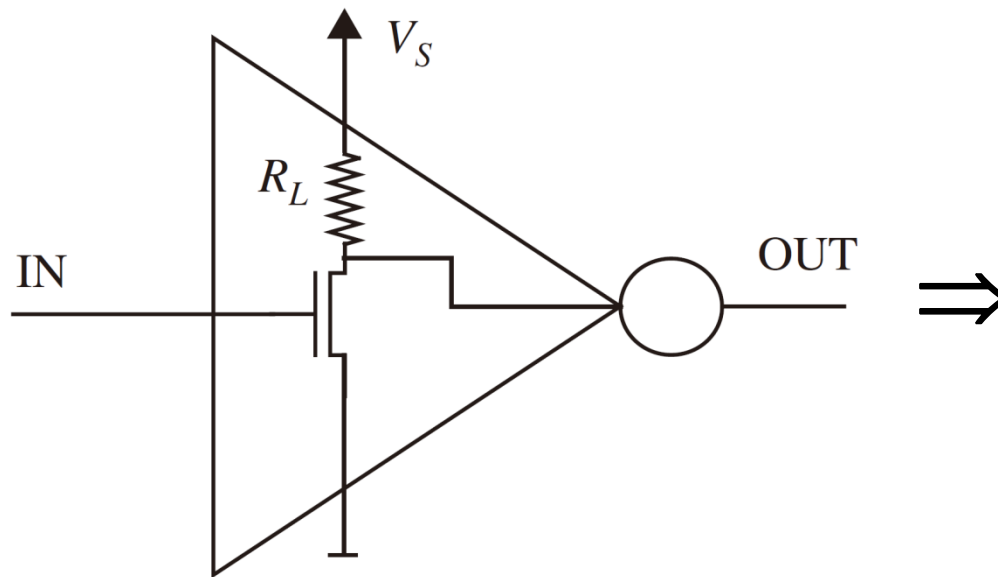
- The MOSFET Inverter Circuit.



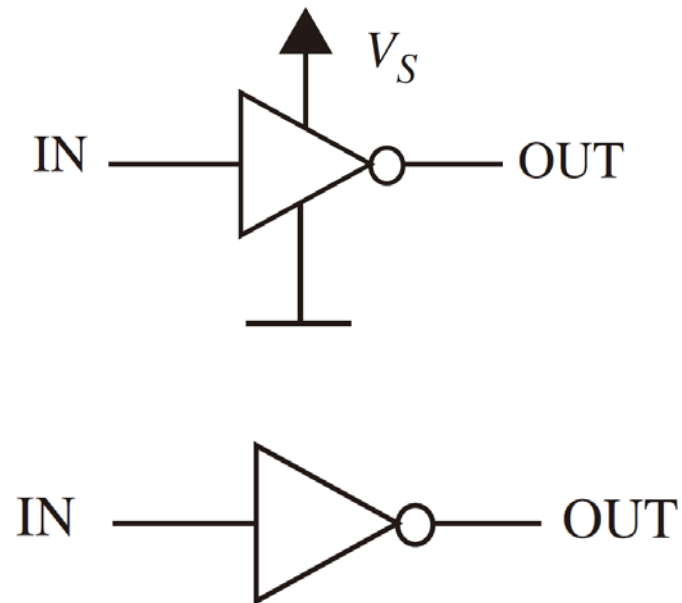
MOSFET Inverter Circuit

Shorthand notation for power and ground

# The inverter abstraction



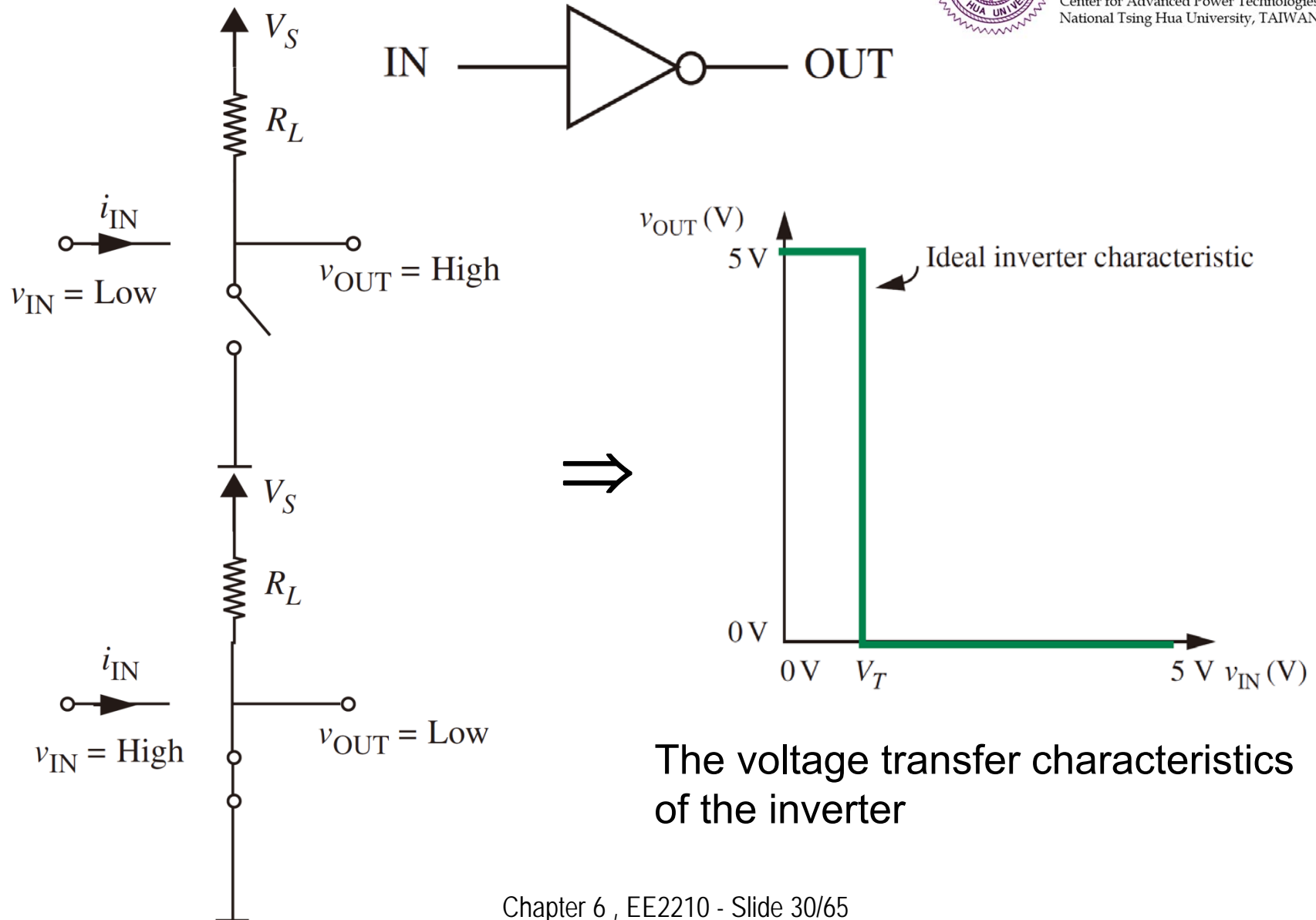
The inverter abstraction and its internal circuit



The inverter abstraction

**Note the power of abstraction:** The *inverter abstraction* hides the internal details such as power supply, transistor, ground connections.

# Voltage Transfer Characteristics



# Static Analysis Using S Model

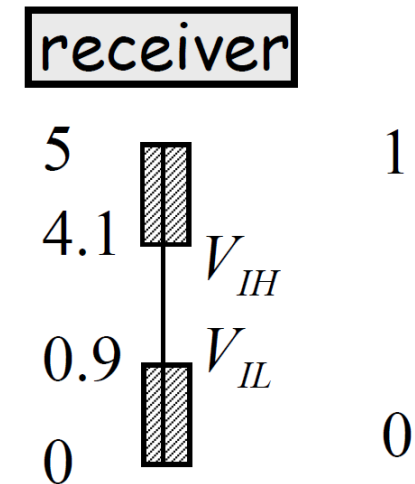
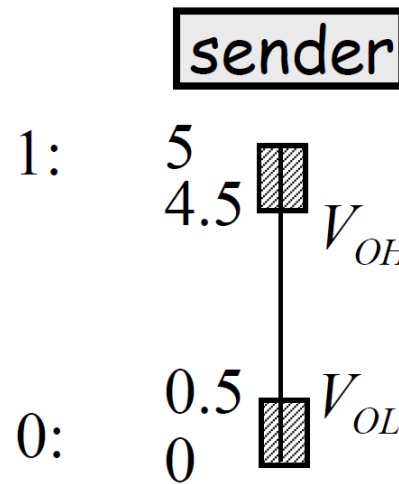
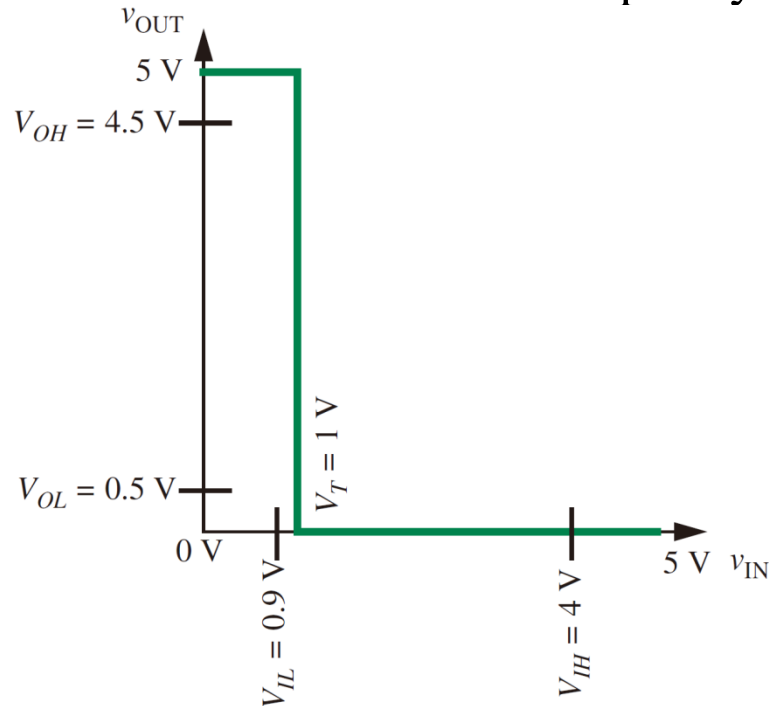


- Suppose gates should satisfy the following static discipline.

$$V_{OL} = 0.5 \text{ V}, \quad V_{OH} = 4.5 \text{ V}$$

$$V_{IL} = 0.9 \text{ V}, \quad V_{IH} = 4.1 \text{ V}$$

- Does this inverter qualify?



- This inverter satisfies the above static discipline.

# Static Analysis Using S Model



- Does this inverter satisfy the following two static disciplines A and B:

- Static disciplines A

$$V_{OL} = 0.2 \text{ V}, \quad V_{OH} = 4.8 \text{ V}$$

$$V_{IL} = 0.5 \text{ V}, \quad V_{IH} = 4.5 \text{ V}$$

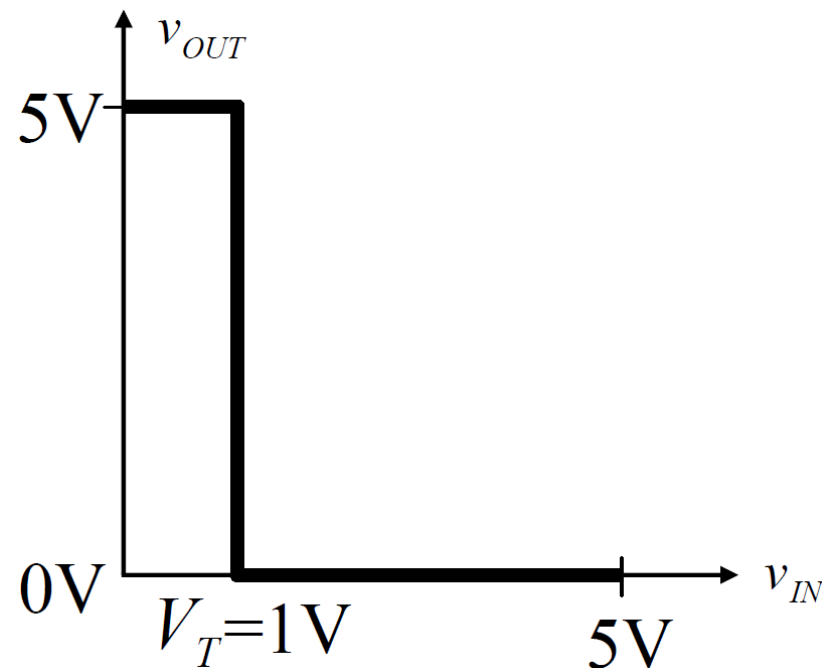
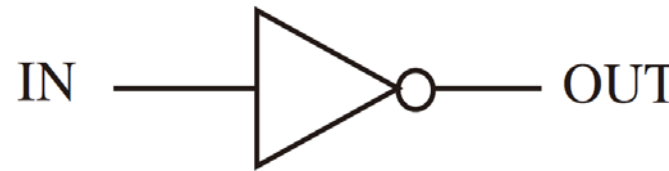
**Yes**, for Static disciplines A.

- Static disciplines B

$$V_{OL} = 0.5 \text{ V}, \quad V_{OH} = 4.5 \text{ V}$$

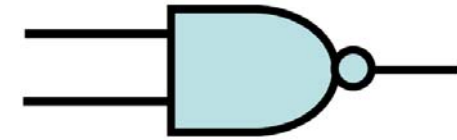
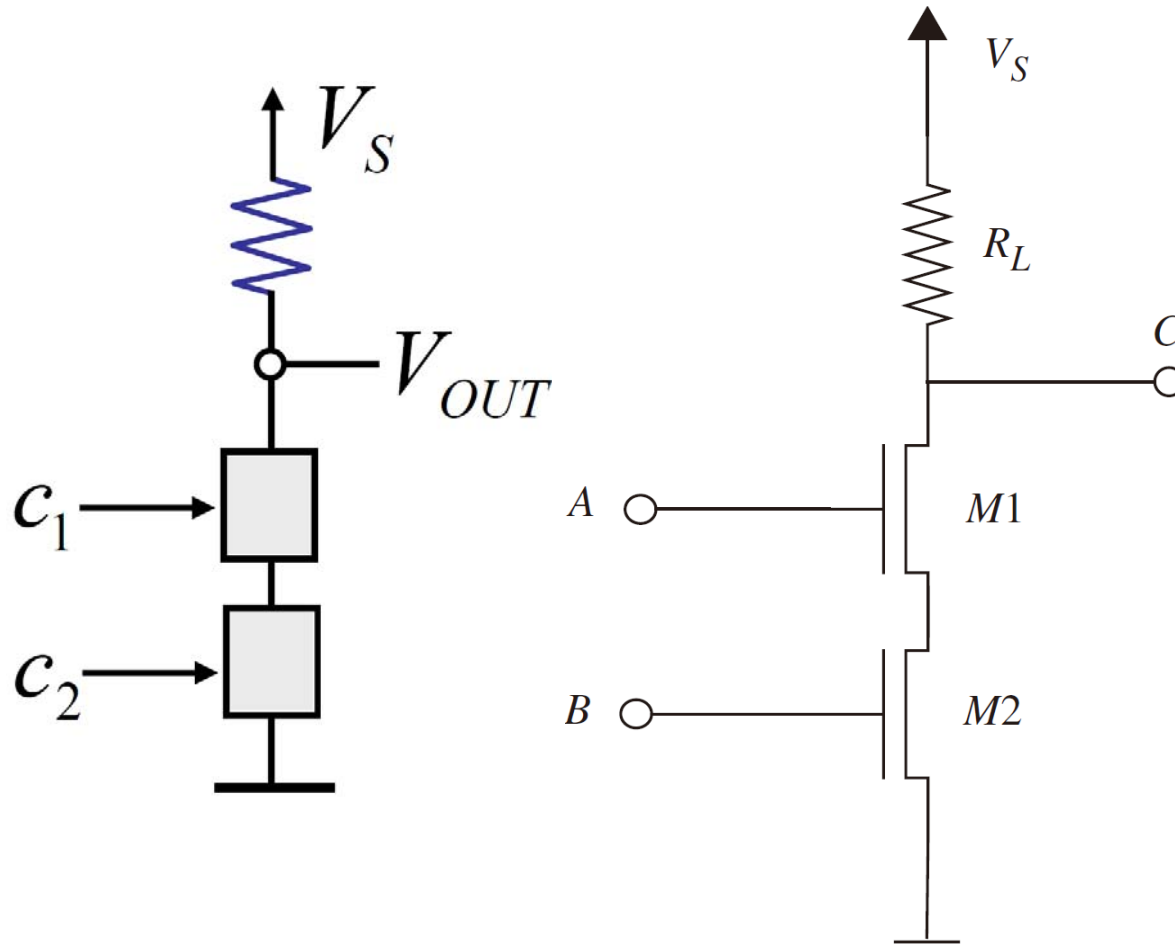
$$V_{IL} = 1.5 \text{ V}, \quad V_{IH} = 3.5 \text{ V}$$

**No**, for Static disciplines A





# The NAND Gate



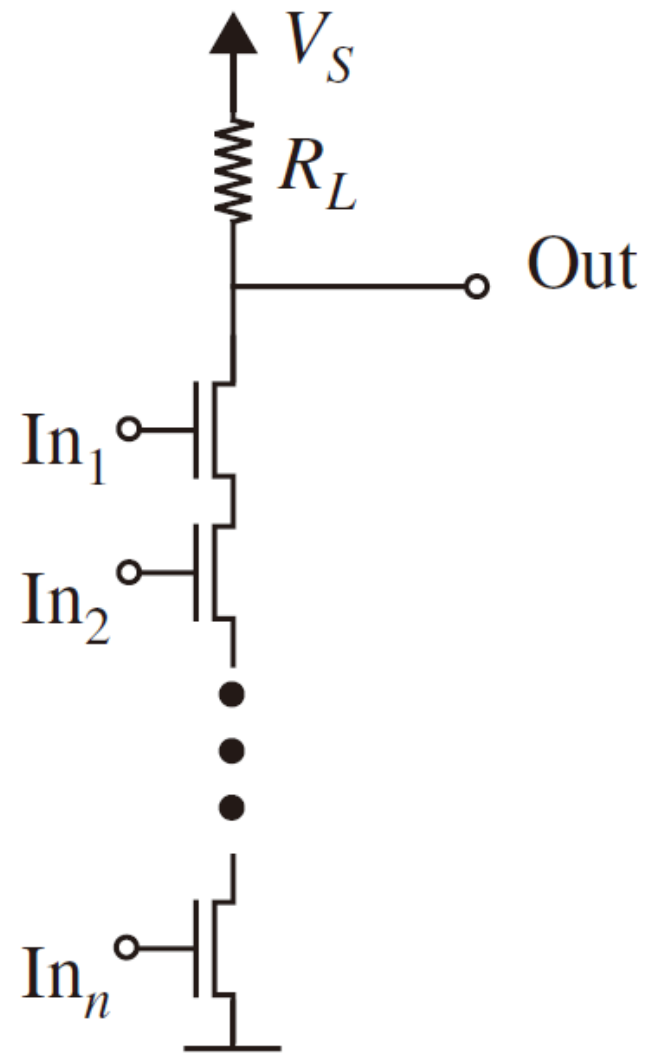
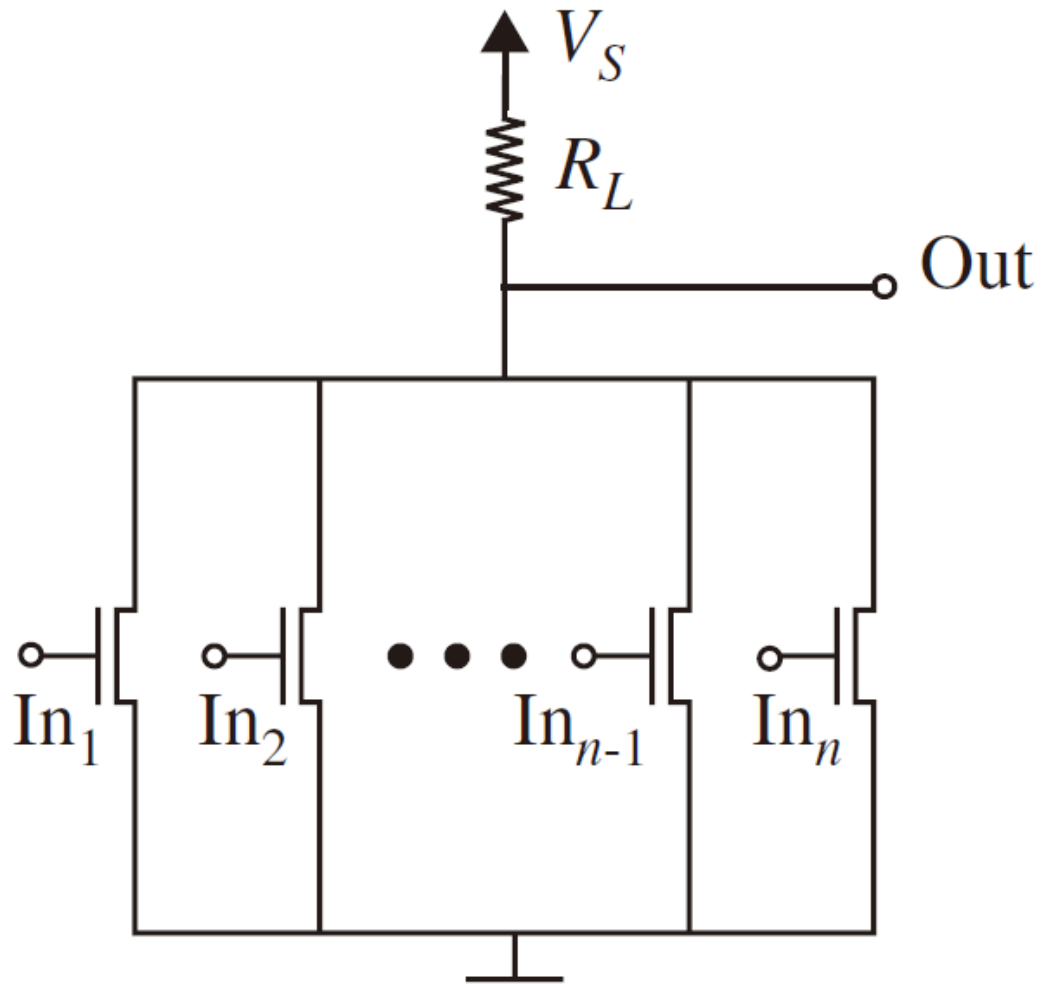
$c_1$	$c_2$	$V_O$
0	0	1
0	1	1
1	0	1
1	1	0

If  $V_A \geq V_T$  AND  $V_B \geq V_T$ , then  $V_{out} = 0$  Else  $V_{out} = V_S$ .

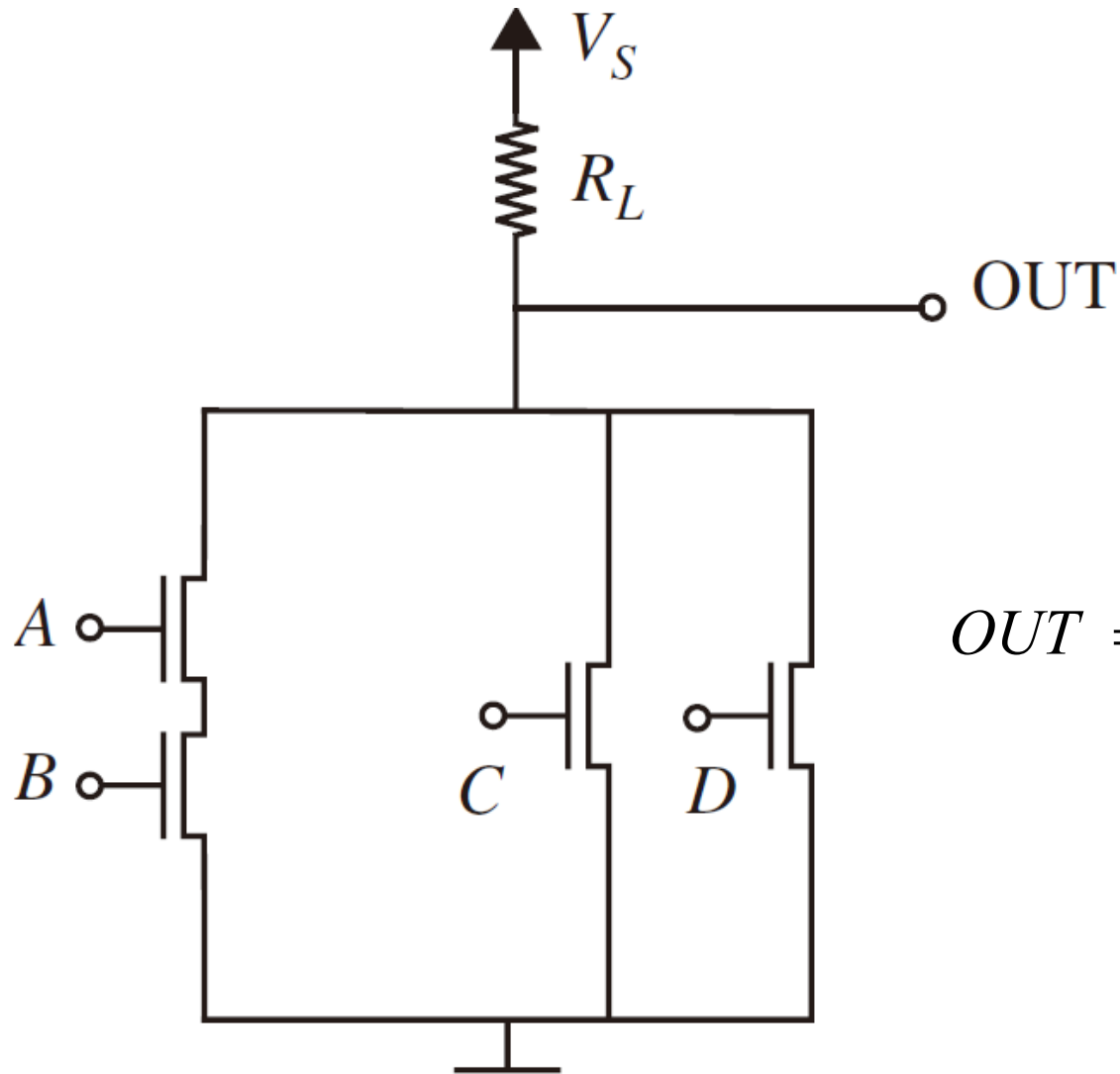
# Multiple-input NOR and NAND gates



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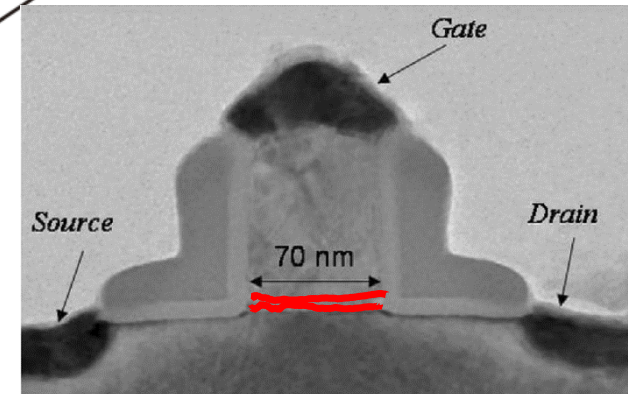
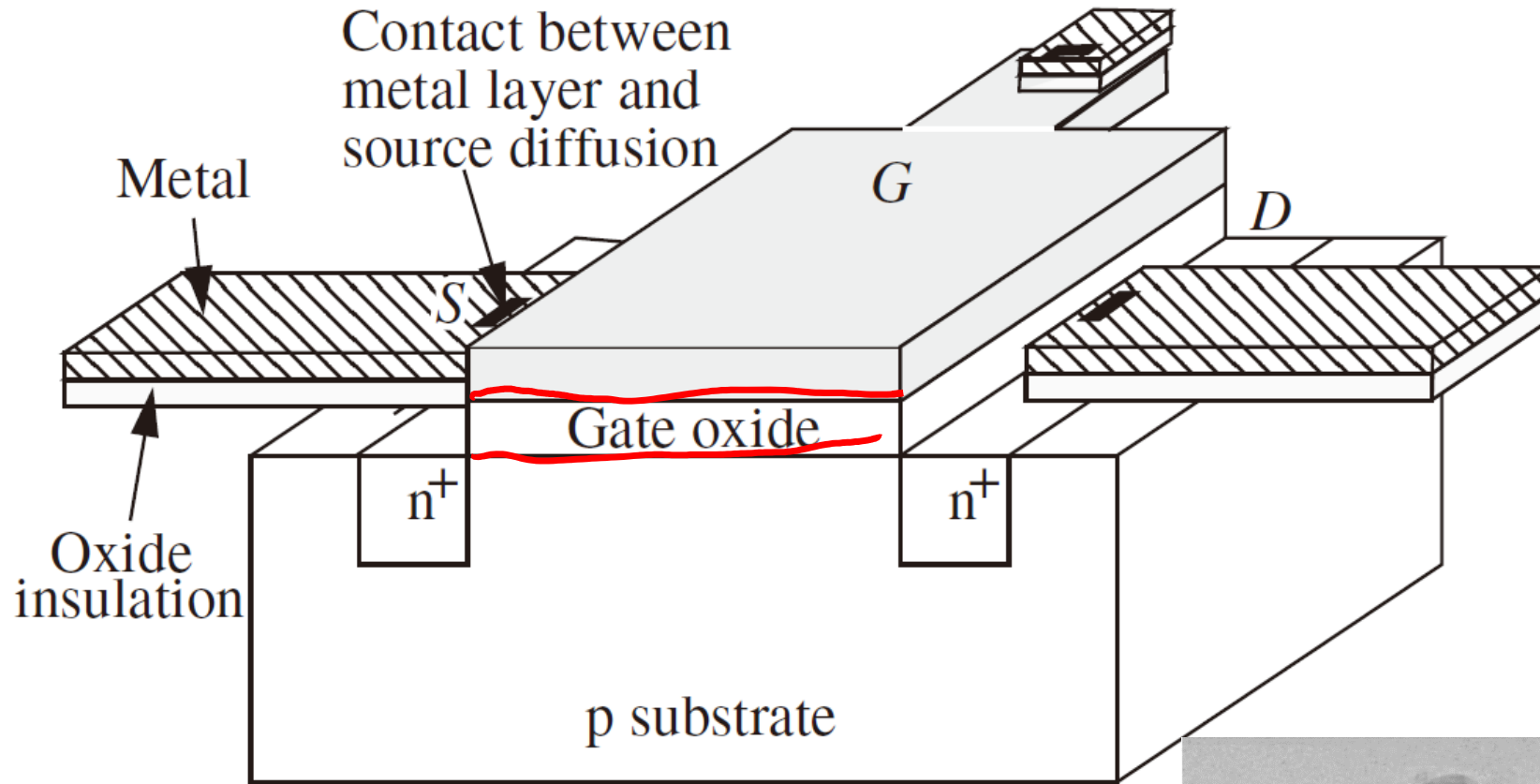


# A Complex Gate



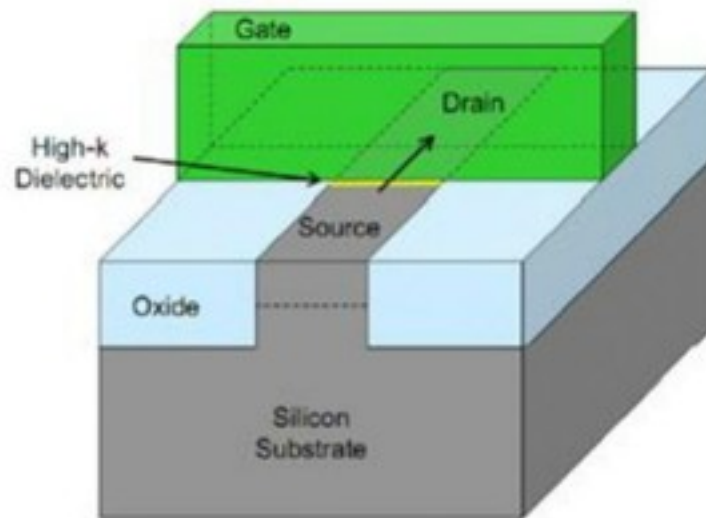
$$OUT = \overline{A \cdot B + C + D}$$

# The Physical Structure of MOSFET



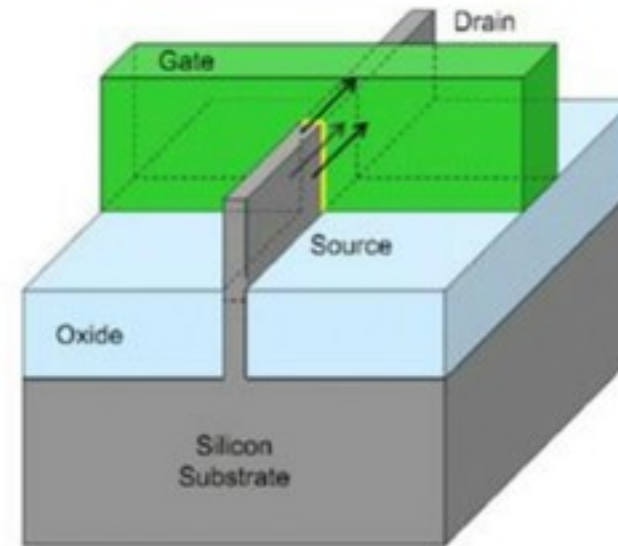


## Traditional Planar

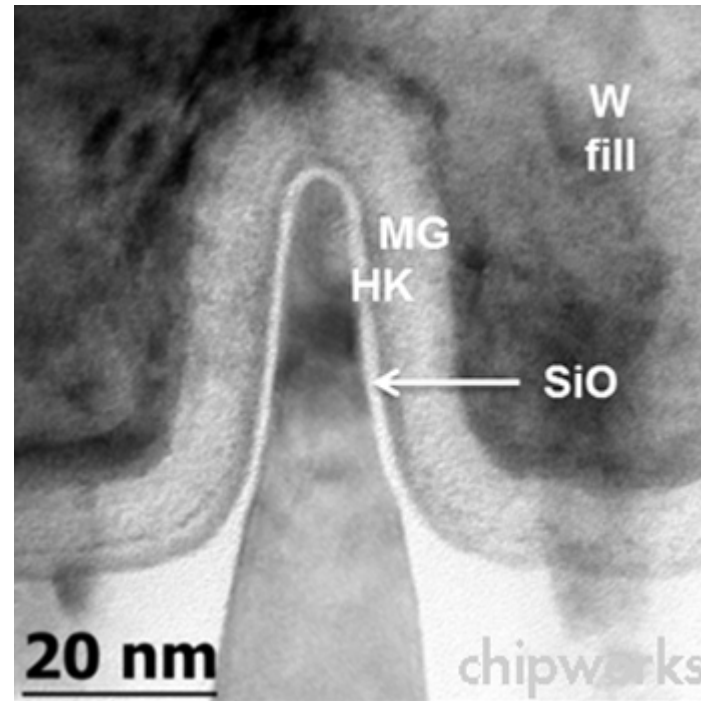
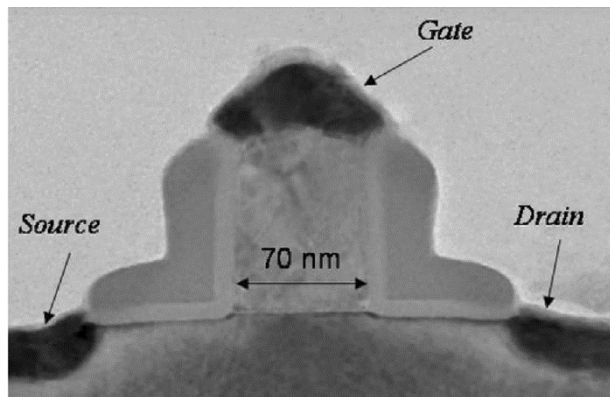
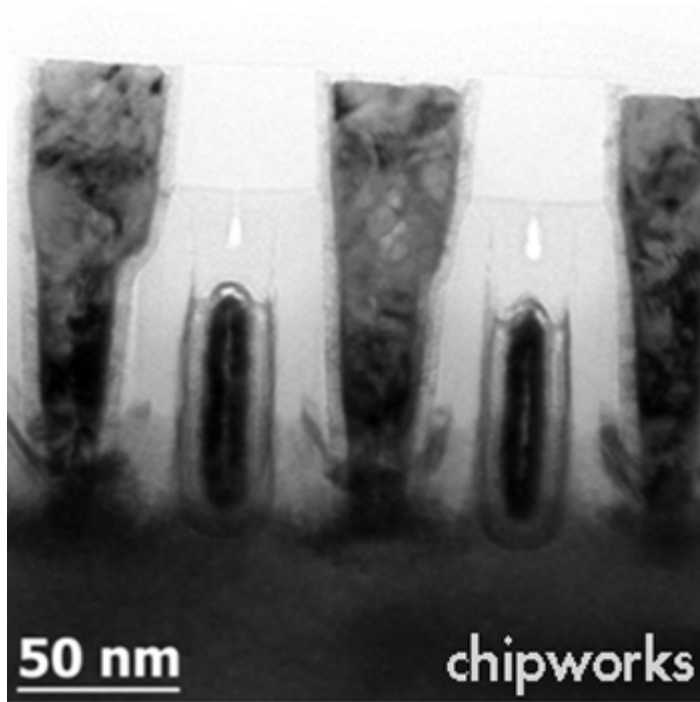


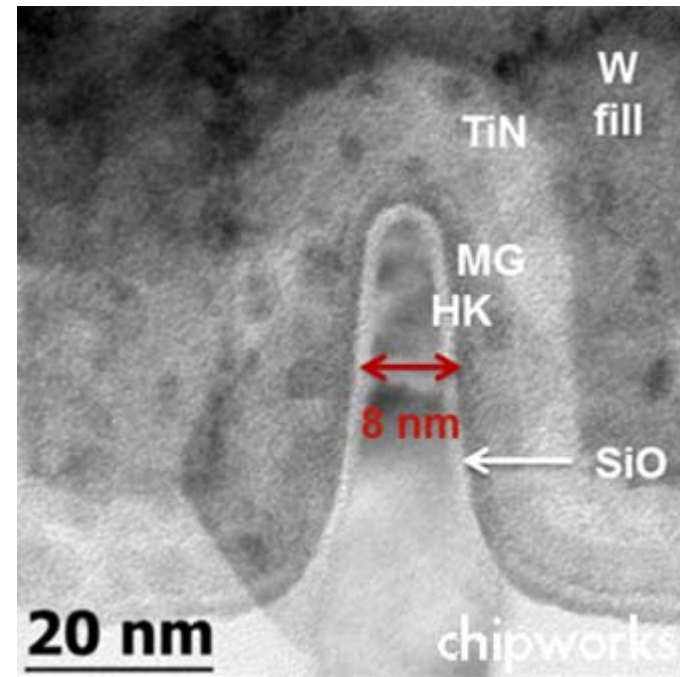
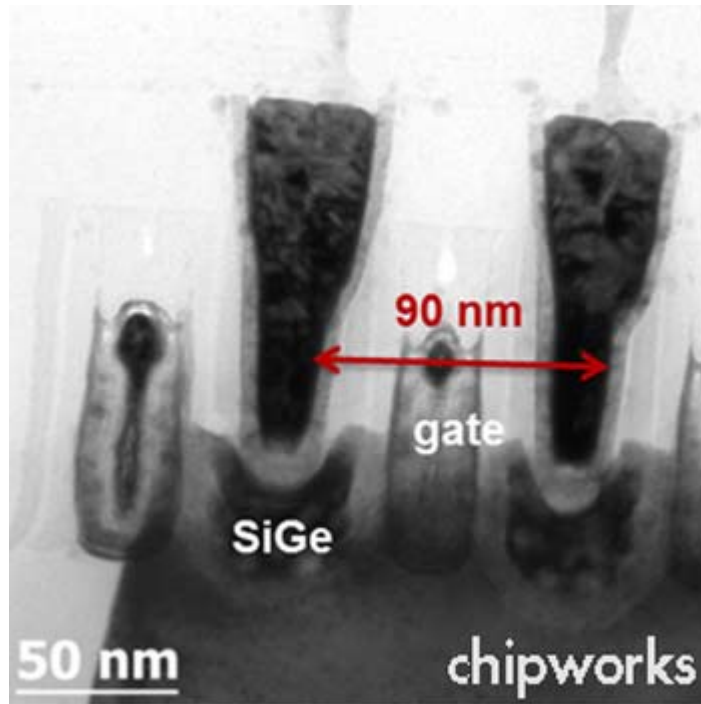
Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

## 3D FinFET

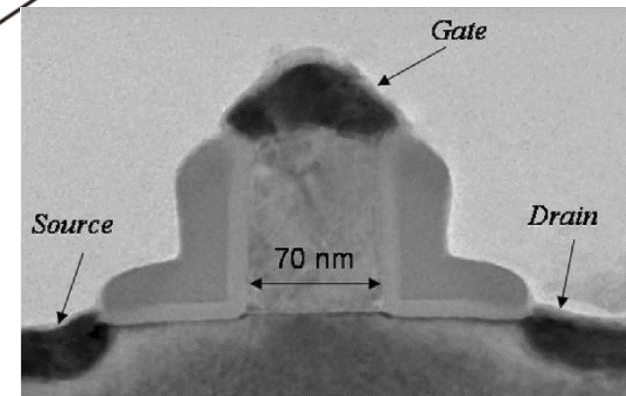
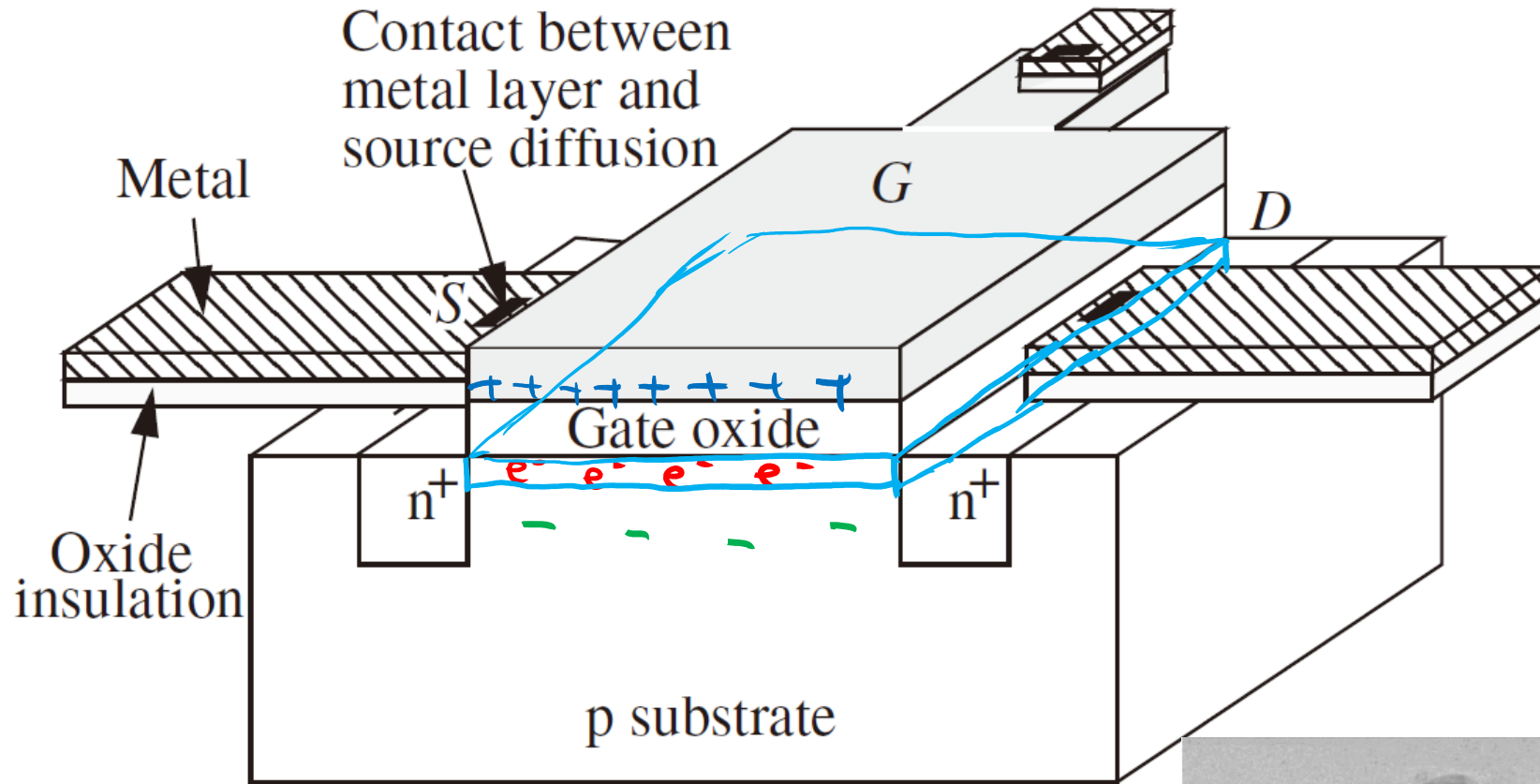


3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

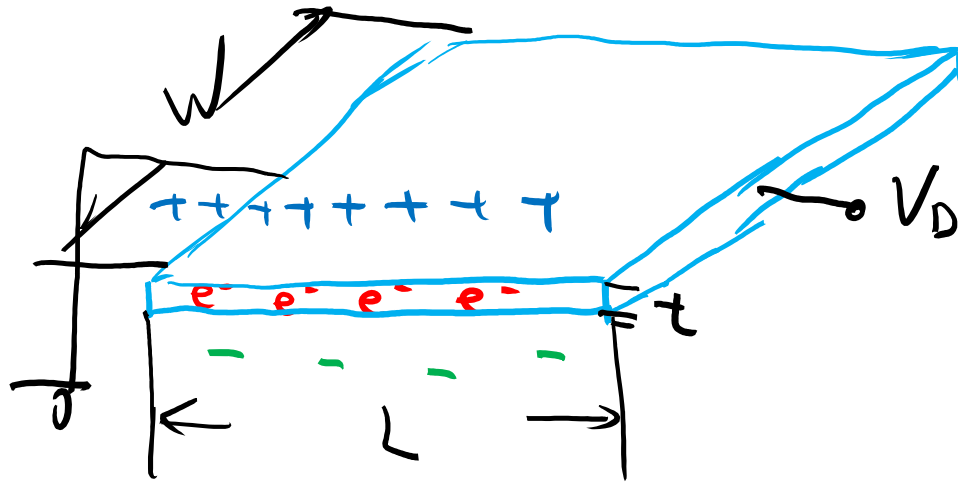




# The Physical Structure of MOSFET

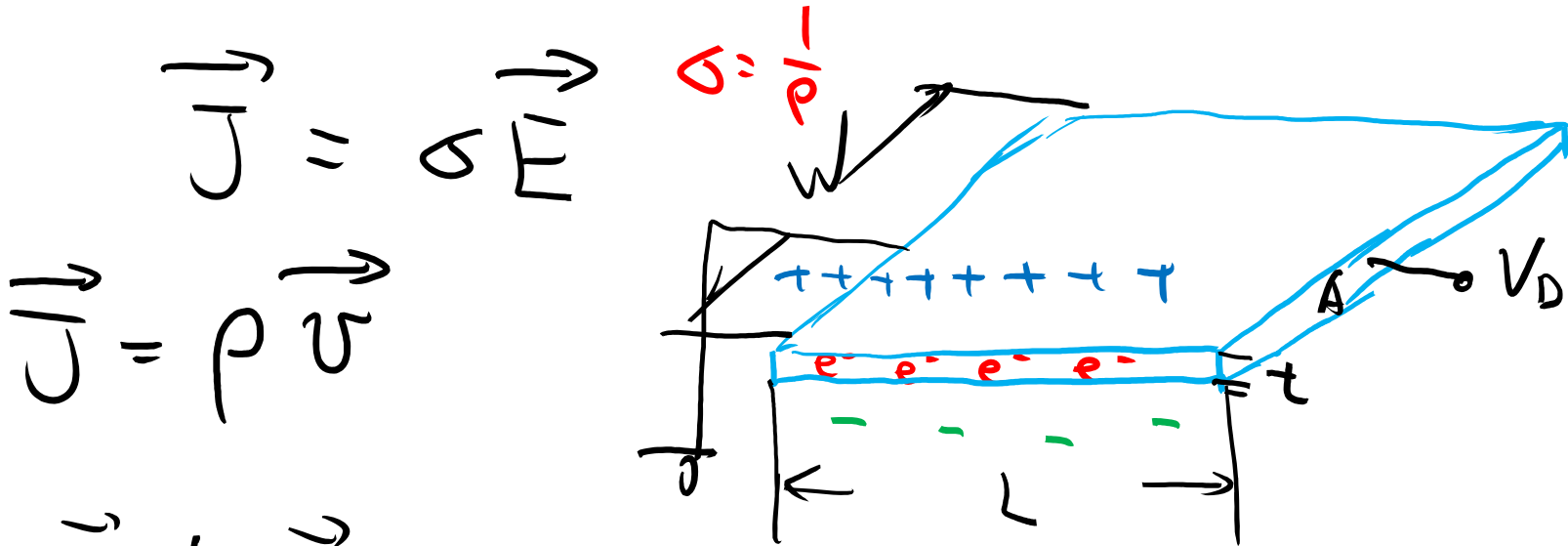








$$R = \rho \frac{L}{A} = \rho \frac{L}{wt}$$



$$I = \vec{J} \cdot A = \vec{J} \cdot w \cdot t$$

$$\rho = q \cdot n$$

$$q = 1.6 \times 10^{-19} \text{ C}$$

$$n: \text{電子濃度} \frac{\#}{\text{cm}^3}$$



$$\vec{S} = \mu \vec{E} \times \vec{H}$$

$$\vec{E} = \frac{V_D}{L}$$

$I$  vs  $V_D$

$$\vec{J} = \rho \vec{v}$$

$$I = \frac{V}{R}$$

$$I \cdot W \cdot t = \rho v \cdot W \cdot t = qn \mu E \cdot W \cdot t$$

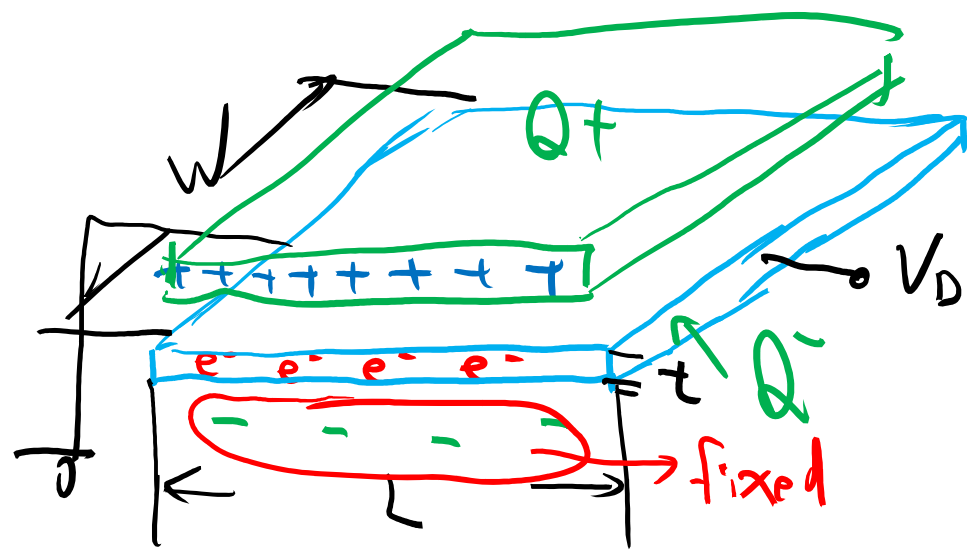
$$= qn \mu \frac{V_D}{L} \cdot W \cdot t$$

$$R = \frac{L}{qn \mu W}$$

$$C_{ox}(V_G - V_T)$$

$$R = R_n \frac{L}{W}$$

$$R_n = \frac{1}{\mu C_{ox}(V_G - V_T)}$$



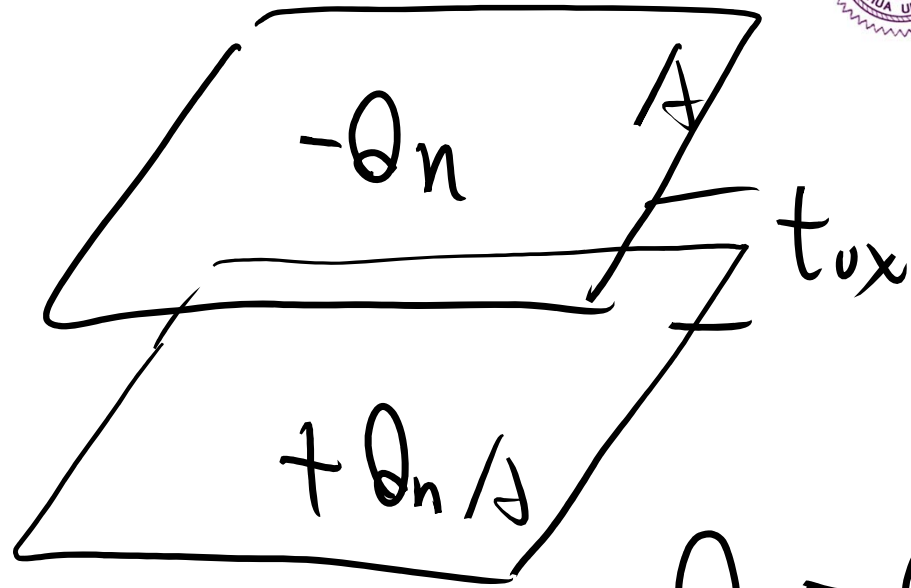
$$Q = CV - Q_{\text{fixed}} = C(V - \frac{Q_{\text{fixed}}}{C})$$

$$P_{nt} = C(V_G - V_T)$$

$$\frac{q_{nt}}{\frac{C}{\text{cm}^3} \cdot \text{cm}} = \frac{P_n \cdot t}{\frac{C}{\text{cm}^2}} = \frac{C}{A} (V_G - V_T) = C' (V_G - V_T)$$

$$q_n = P_n$$

電子電荷密度



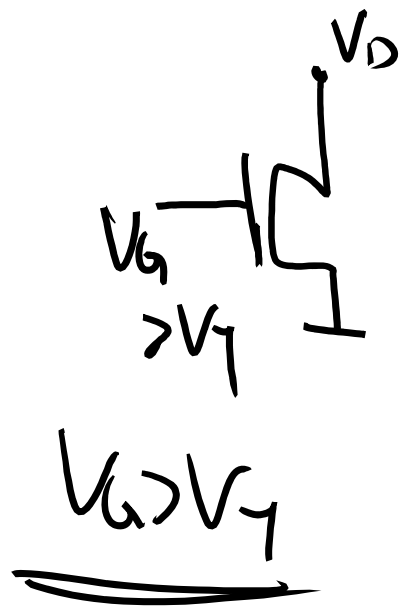
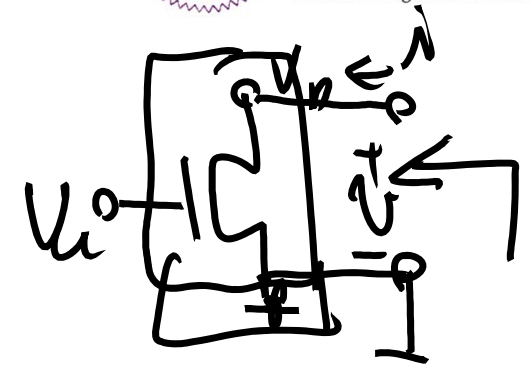
$$C = \epsilon_{SiO_2} \cdot \frac{A}{t_{ox}}$$

$$Q_n = -C(V_G - V_T)$$
$$\frac{Q_n}{A} = -\frac{C}{A}(V_G - V_T)$$

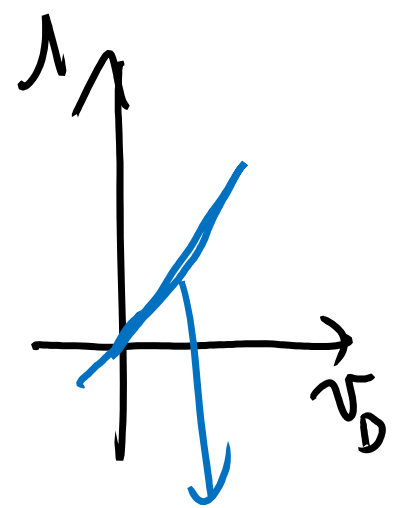


$$R = R_n \frac{L}{W}$$

$$R_n = \frac{1}{\mu C_{ox} (V_G - V_T)}$$



$$R_n \frac{L}{W}$$

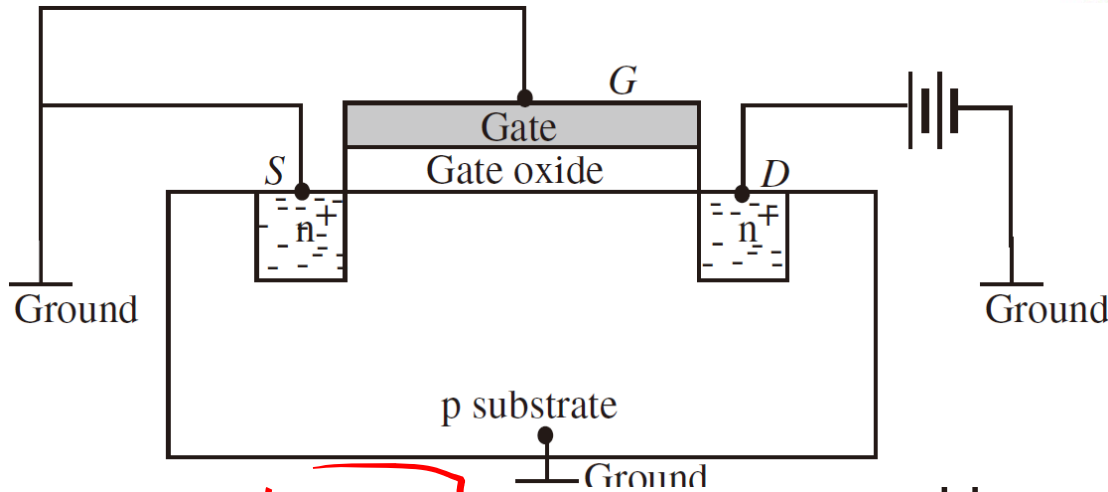


$$\text{slope} = \frac{1}{R_n \frac{L}{W}}$$

# The MOSFET with Gate Bias



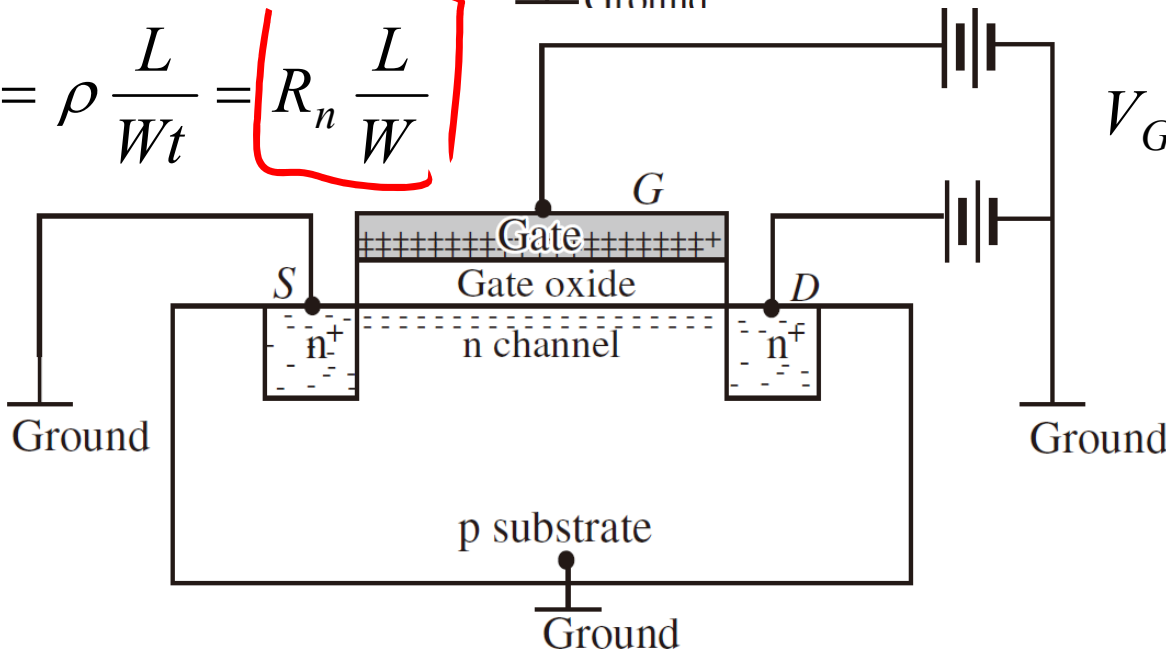
$$V_G = 0V$$



$$R_{on} = \rho \frac{L}{A} = \rho \frac{L}{Wt} = R_n \frac{L}{W}$$

$$R_{on} \neq 0 \Omega$$

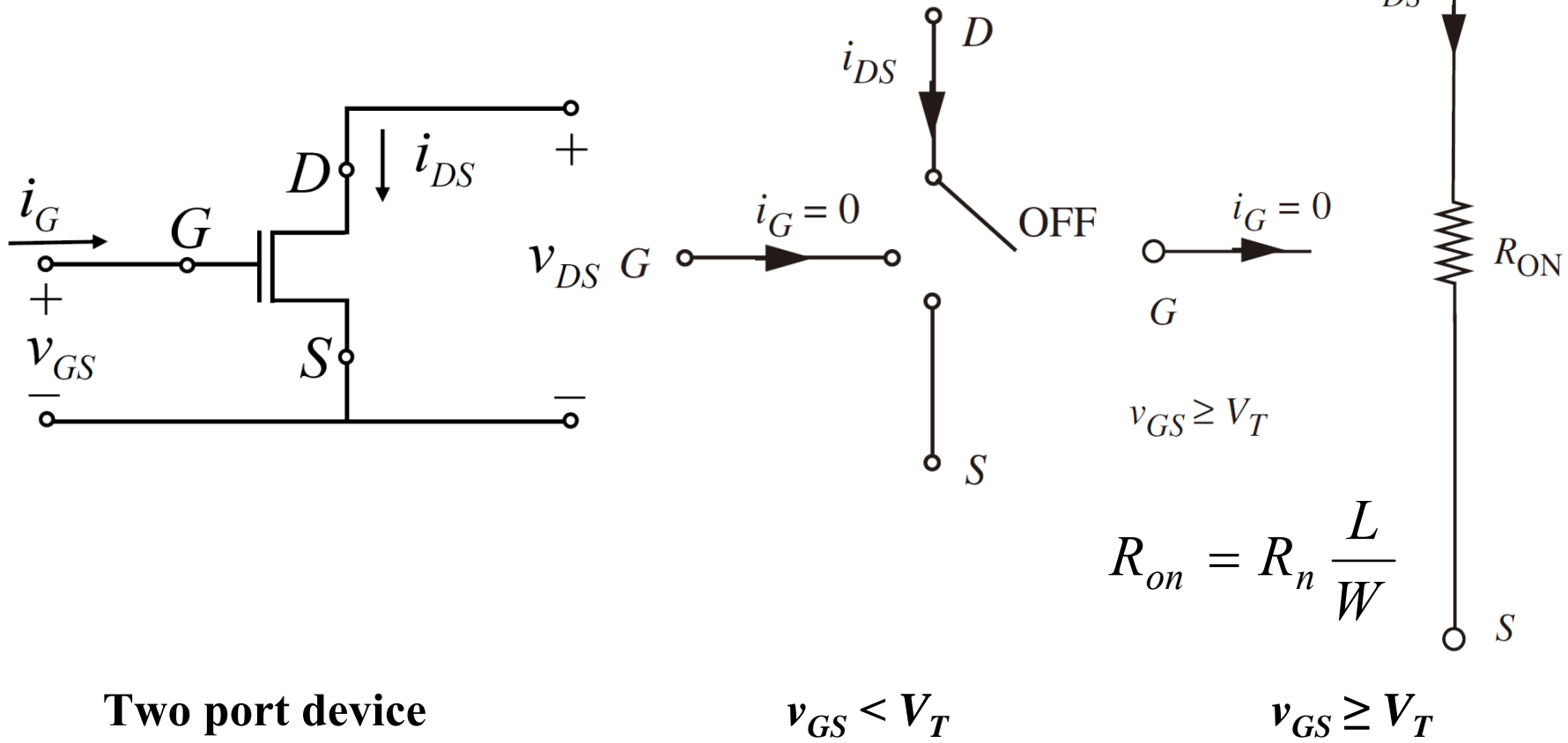
$$V_G = 5V > V_T$$



# SR model of MOSFET



- Switch resistor (SR) model of MOSFET.
- This is a more accurate MOSFET mode



Two port device

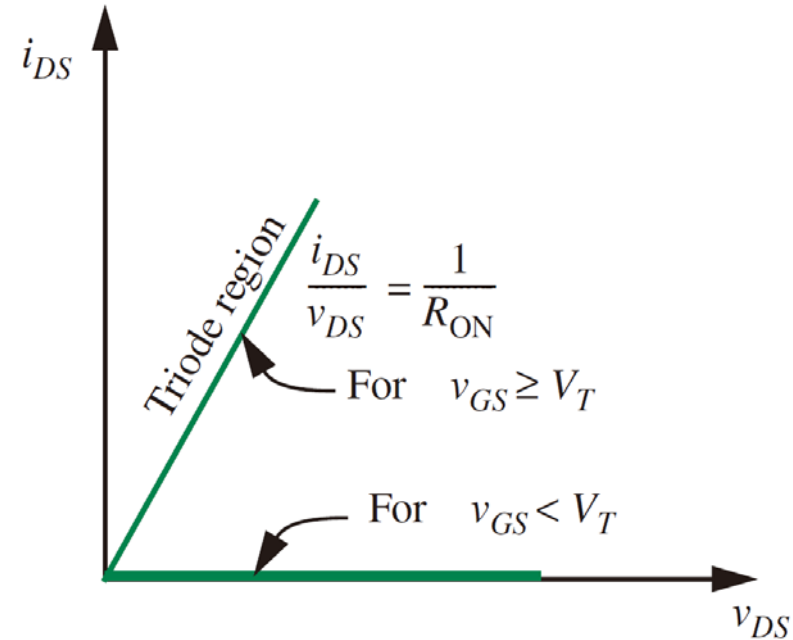
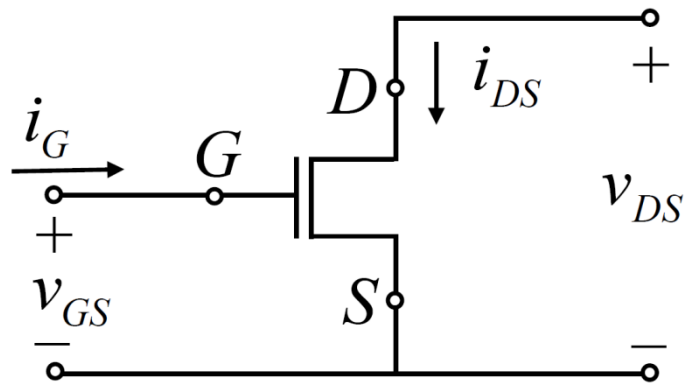
$$v_{GS} < V_T$$

$$v_{GS} \geq V_T$$





# SR model of the MOSFET



$$R_{on} = R_n \frac{L}{W}$$

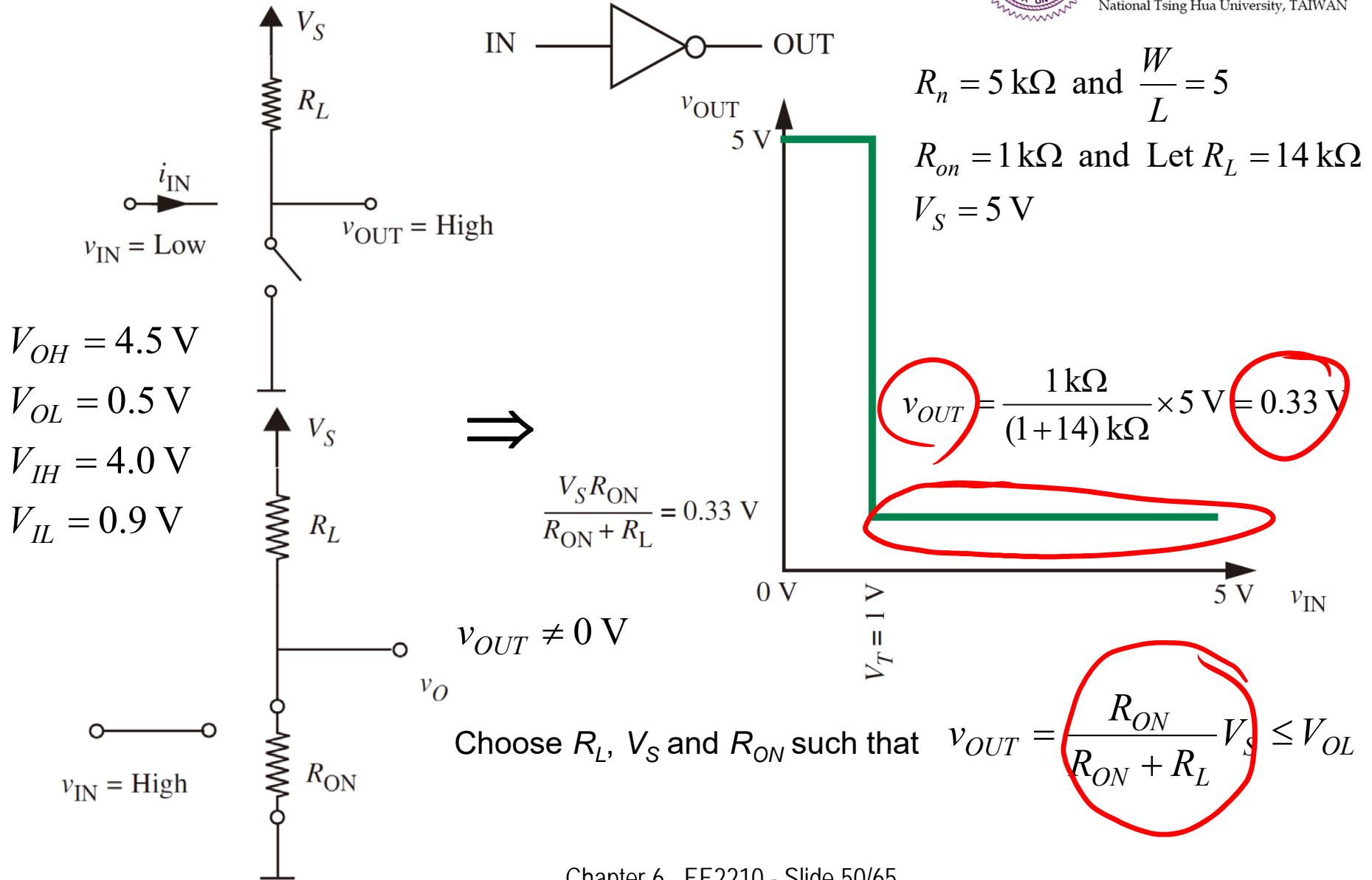
MOSFET  $i$ - $v$  characteristics

For  $v_{GS} < V_T$ ,  $i_{DS} = 0$

and

For  $v_{GS} \geq V_T$ ,  $i_{DS} = v_{DS} / R_{on}$

# Voltage Transfer Characteristics



# The NAND Gate



**CAPT**

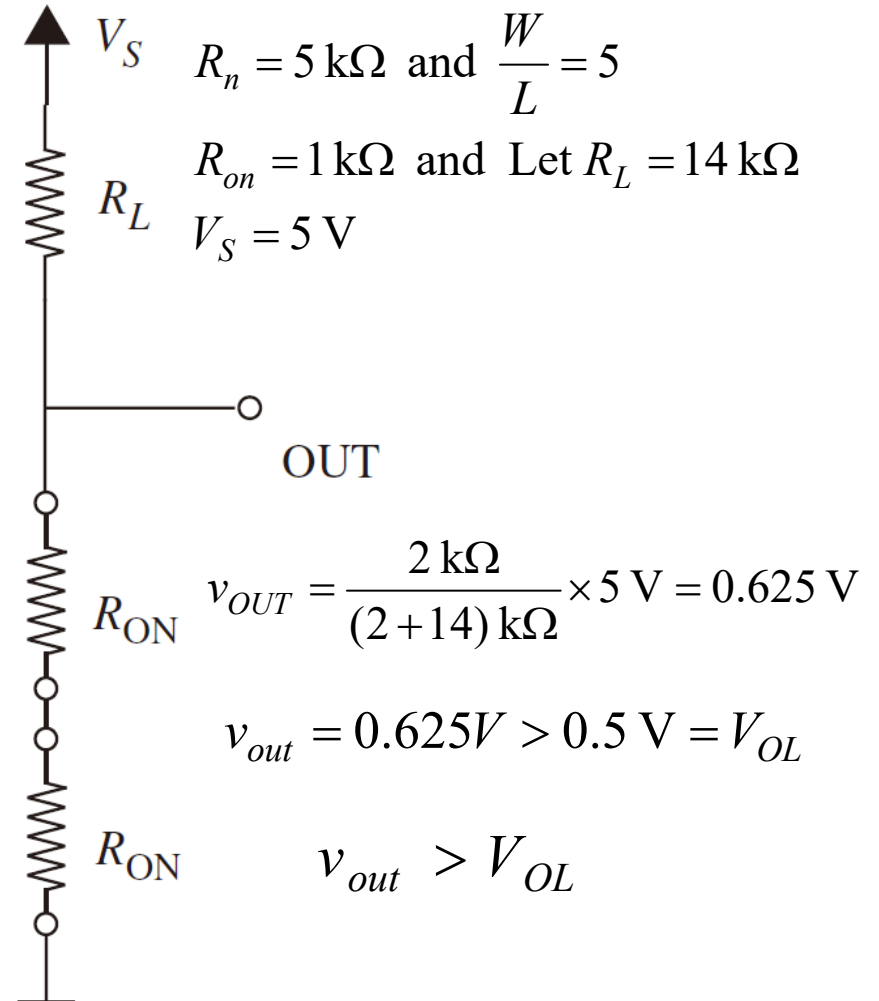
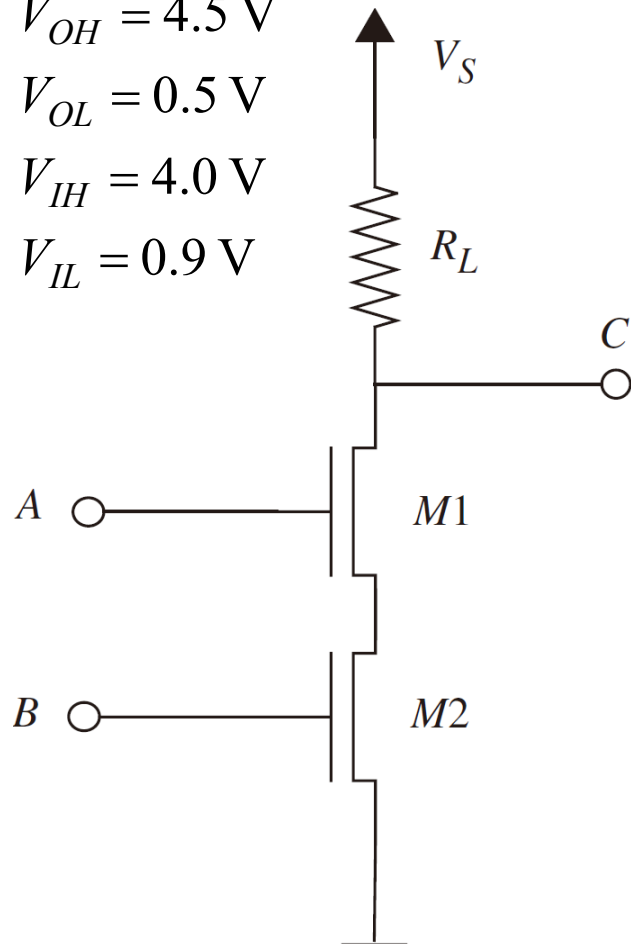
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$$V_{OH} = 4.5 \text{ V}$$

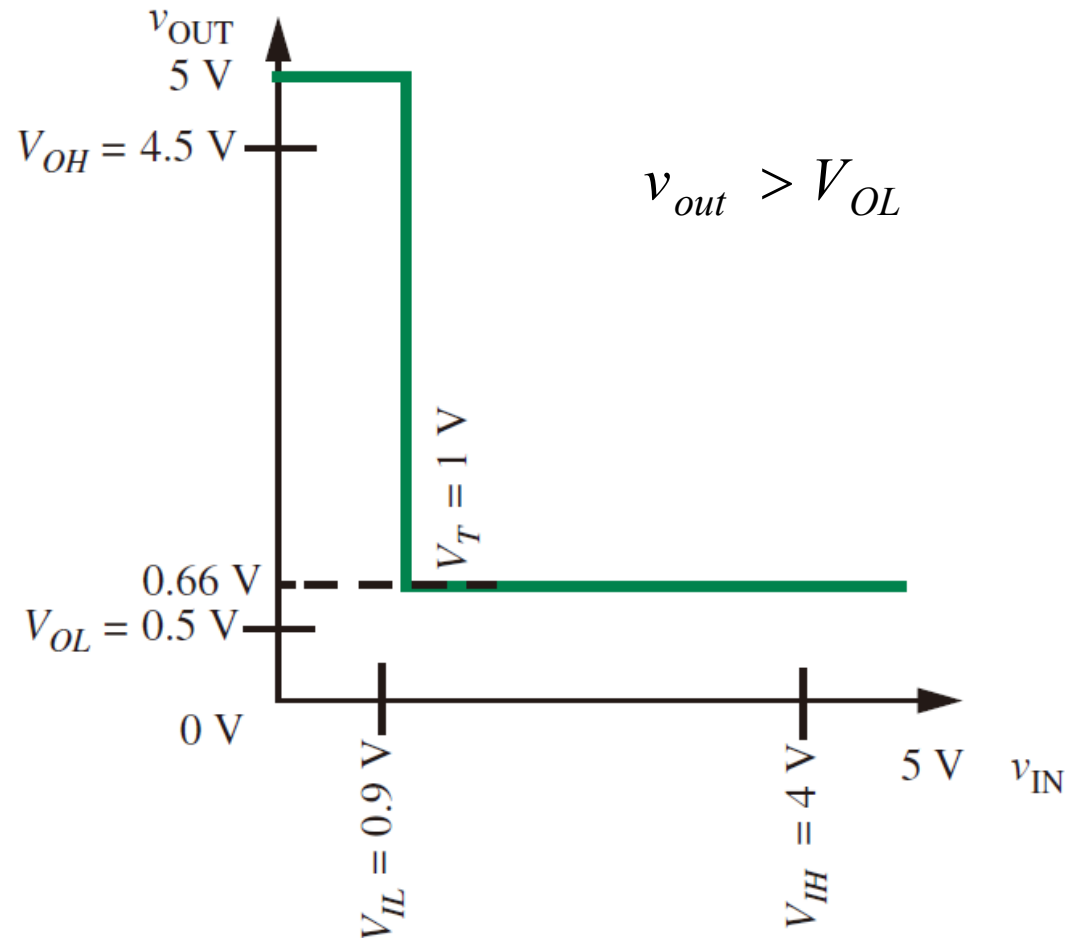
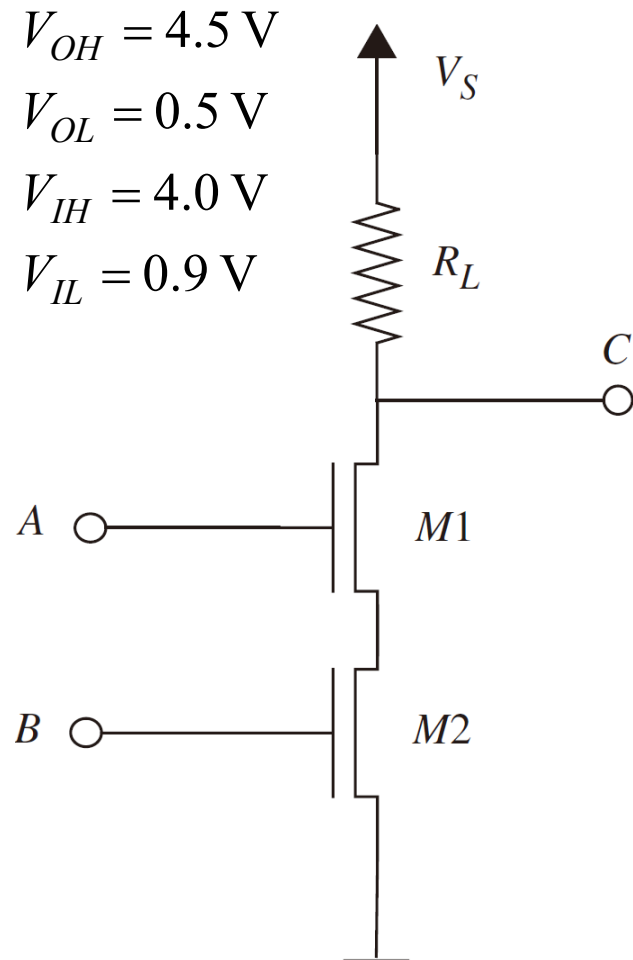
$$V_{OL} = 0.5 \text{ V}$$

$$V_{IH} = 4.0 \text{ V}$$

$$V_{IL} = 0.9 \text{ V}$$



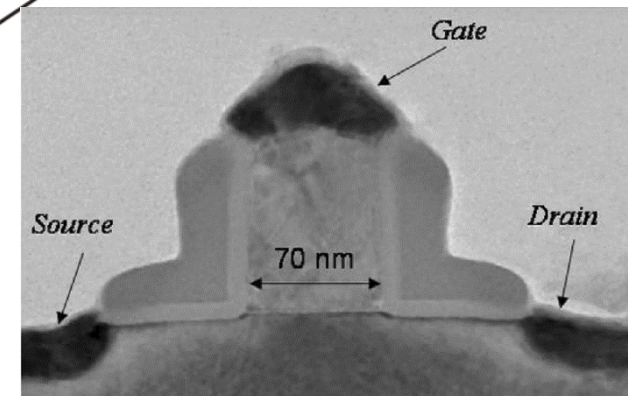
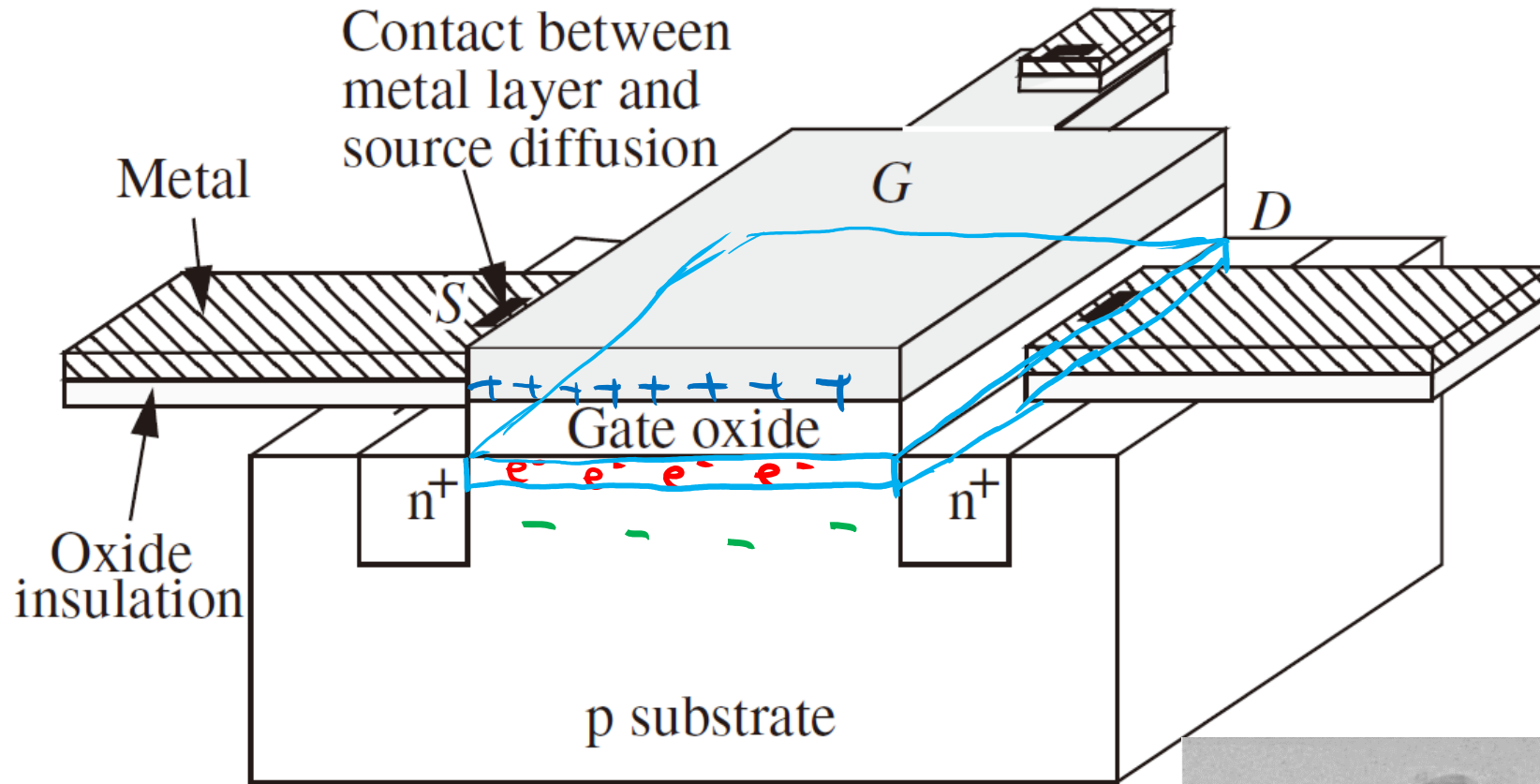
# The NAND Gate



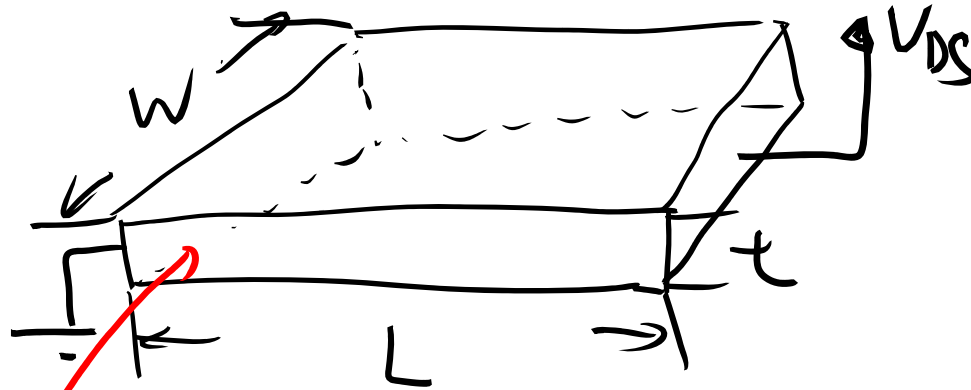
# The Physical Structure of MOSFET



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①



$$\vec{E} \approx \frac{V_{DS}}{L} \quad V_{DS} \ll h$$

$$I_D = W Q_n v \quad \vec{J} = \rho \vec{v} = \underbrace{qn}_{\rho_p} (\mu \vec{E}) = \rho_p \mu \frac{V_{DS}}{L}$$

$$I = \vec{J} \cdot A = \vec{J} \cdot Wt = \rho_p \mu \frac{V_{DS}}{L} \cdot Wt$$

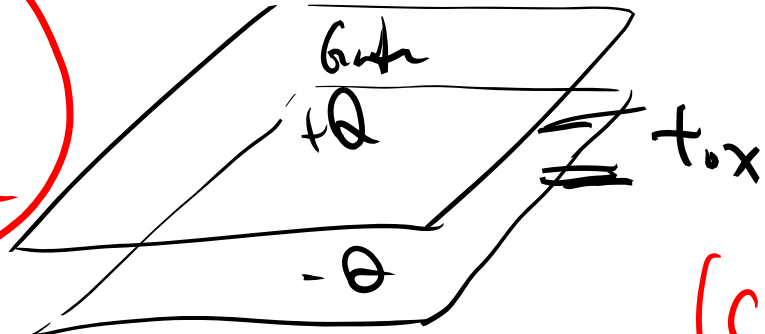
$$= \mu \frac{W}{L} (qn t) V_{DS}$$

$$\rho_p t = \left( \frac{C}{m^3} \right) (m) = \left( \frac{C}{m^2} \right)$$

$$\rho_p t = p \cdot t$$



①  $\mu \frac{W}{L} V_D$



$$I_D = \mu \frac{W}{L} C_{ox} (V_G - V_T) V_D$$

(C) (F) (V)

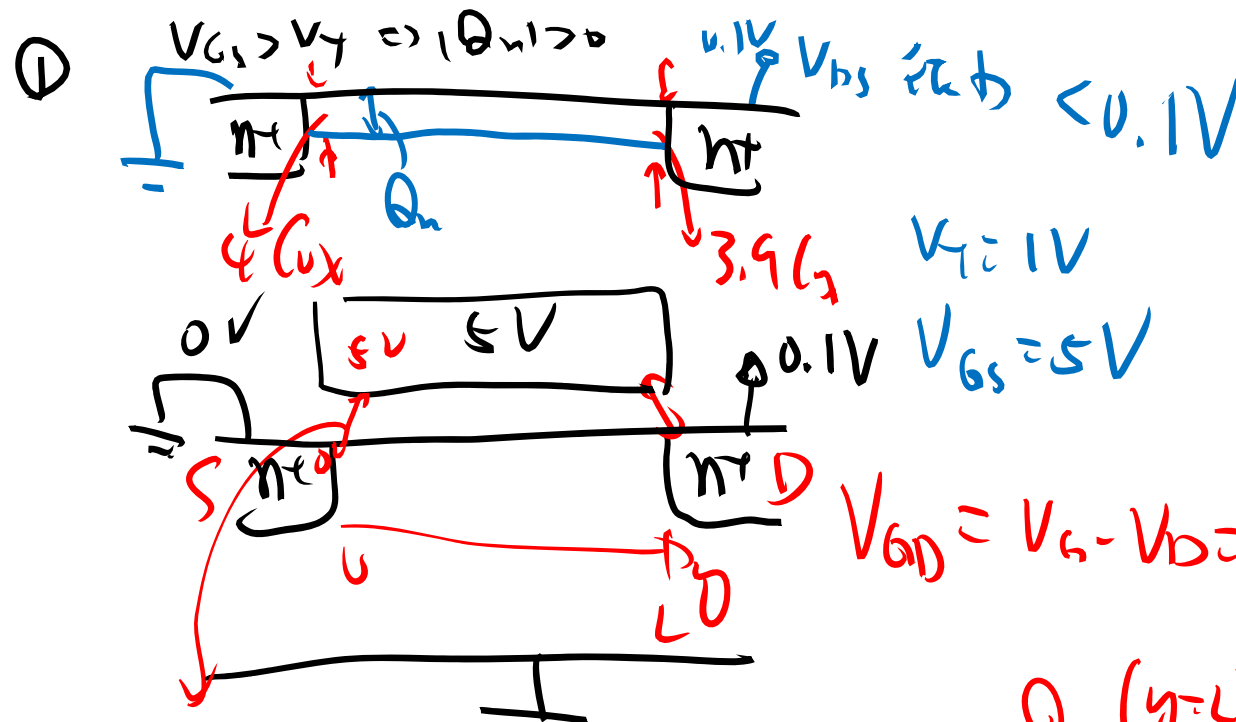
$$C = \epsilon_{ox} \cdot \frac{A}{t_{ox}} \quad Q = CV = \epsilon_{ox} \frac{A}{t_{ox}} V$$

$$I_D = \mu \frac{W}{L} Q_n V_{DS}$$

$$Q_n = \frac{Q}{A} = \frac{\epsilon_{ox}}{t_{ox}} V$$

~~$$Q_n = C_{ox} V$$~~

$$Q_n = -C_{ox} (V_{GS} - V_T)$$



$$V_{GD} = V_{GS} - V_{DS} = 5 - 0.1 = 4.9V$$

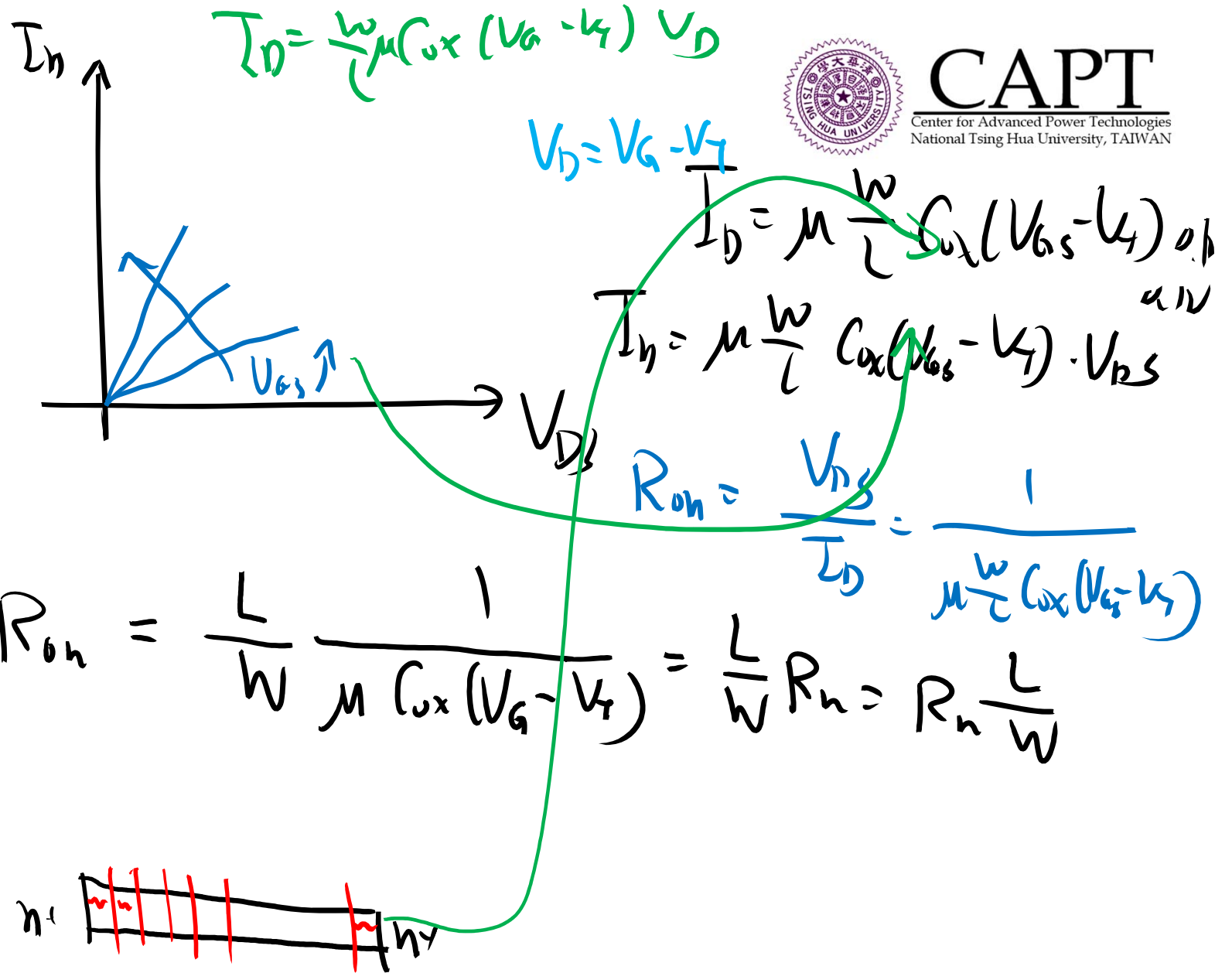
$$Q_n(y=L) = -C_{ox}(5 - 0.1 - 1V)$$

$$= -C_{ox}(5 - 0.1 - 1V)$$

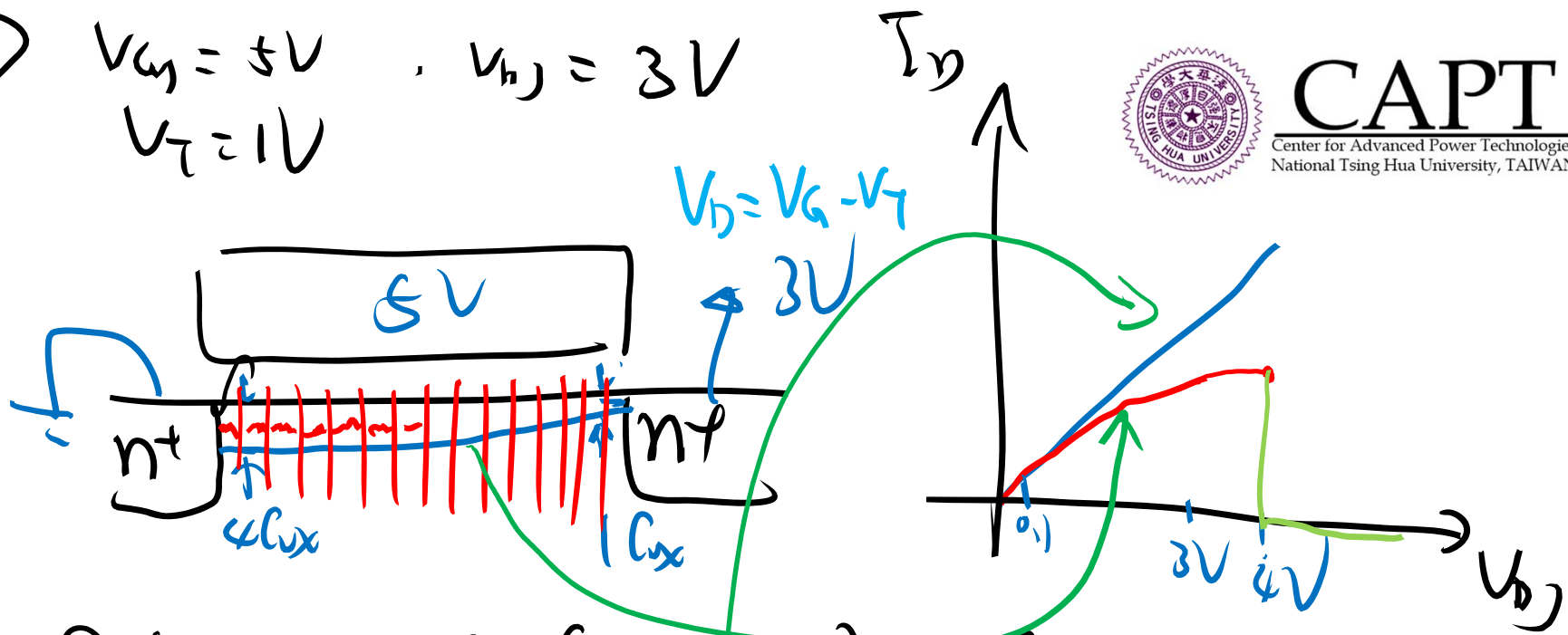
$$Q_n(y=0) = -C_{ox}(5 - 0 - 1V)$$

$$I_n = \mu_n \frac{W}{L} C_{ox} (V_{GS} - V_T) \cdot 0.1V$$





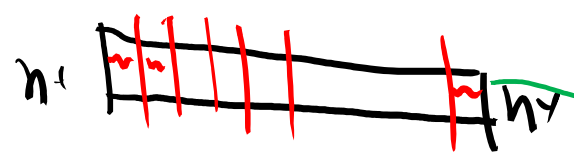
②  $V_{G_s} = 5V$  ,  $V_{D_s} = 3V$   
 $V_T = 1V$

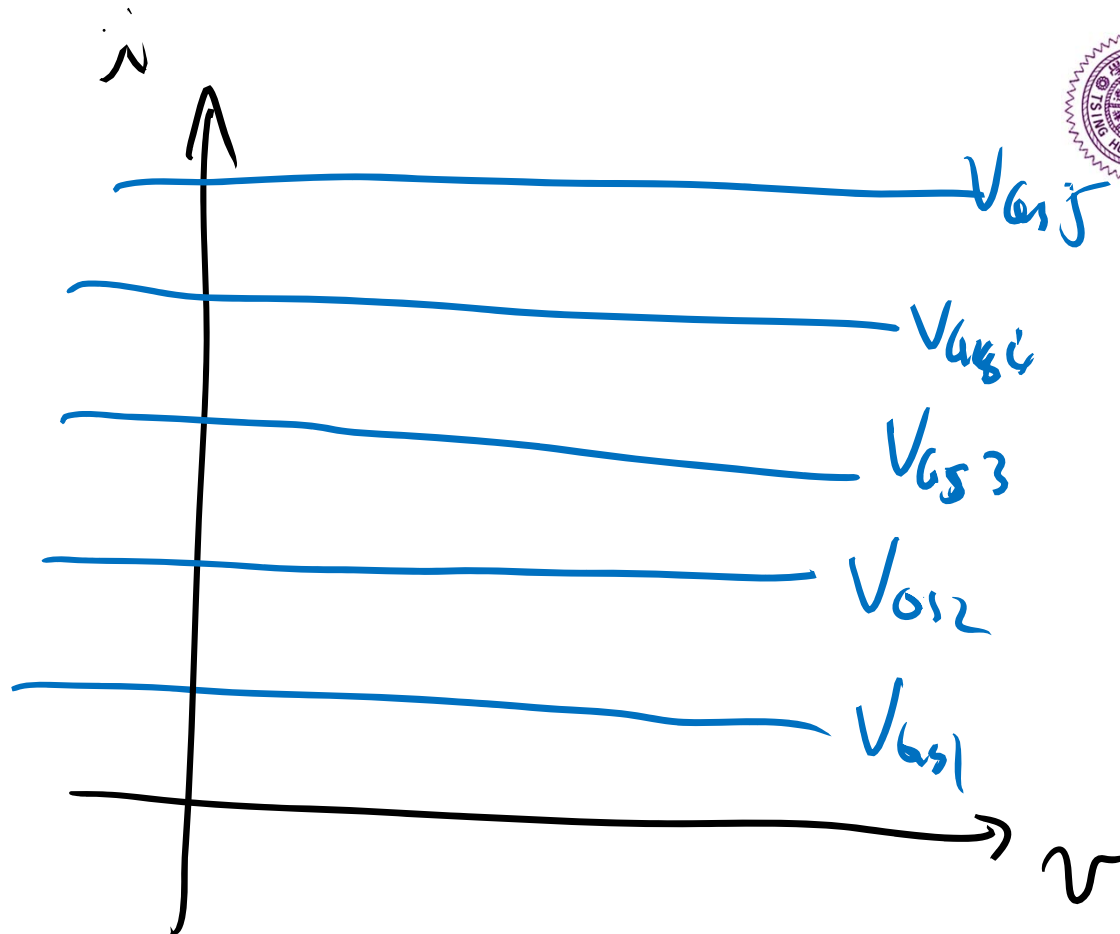


$$Q_n(y=0) = -C_{ox}(5 - 0 - 1) = -4C_{ox}$$

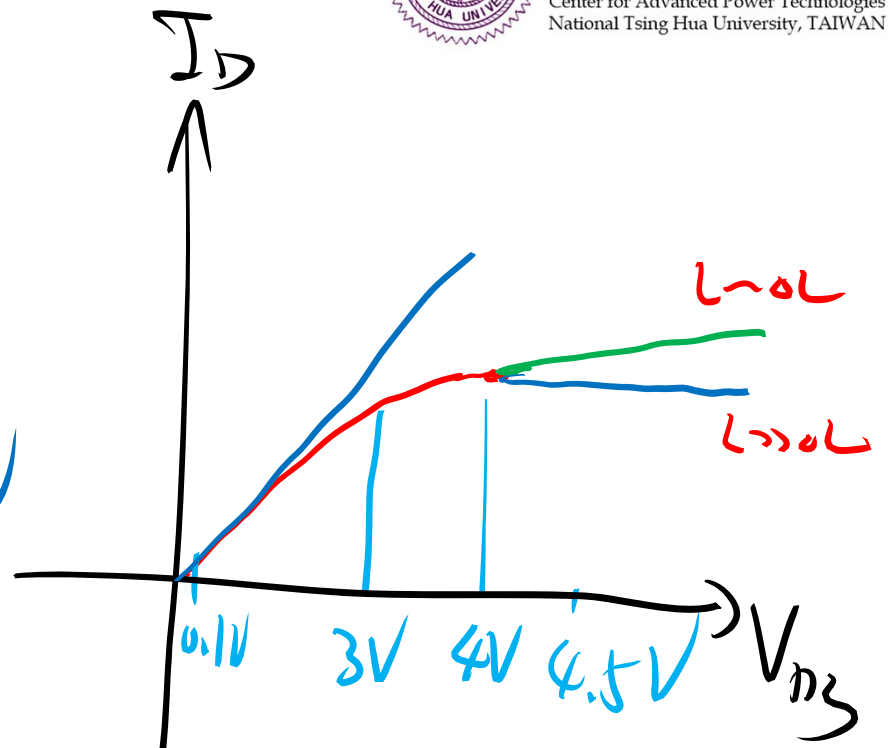
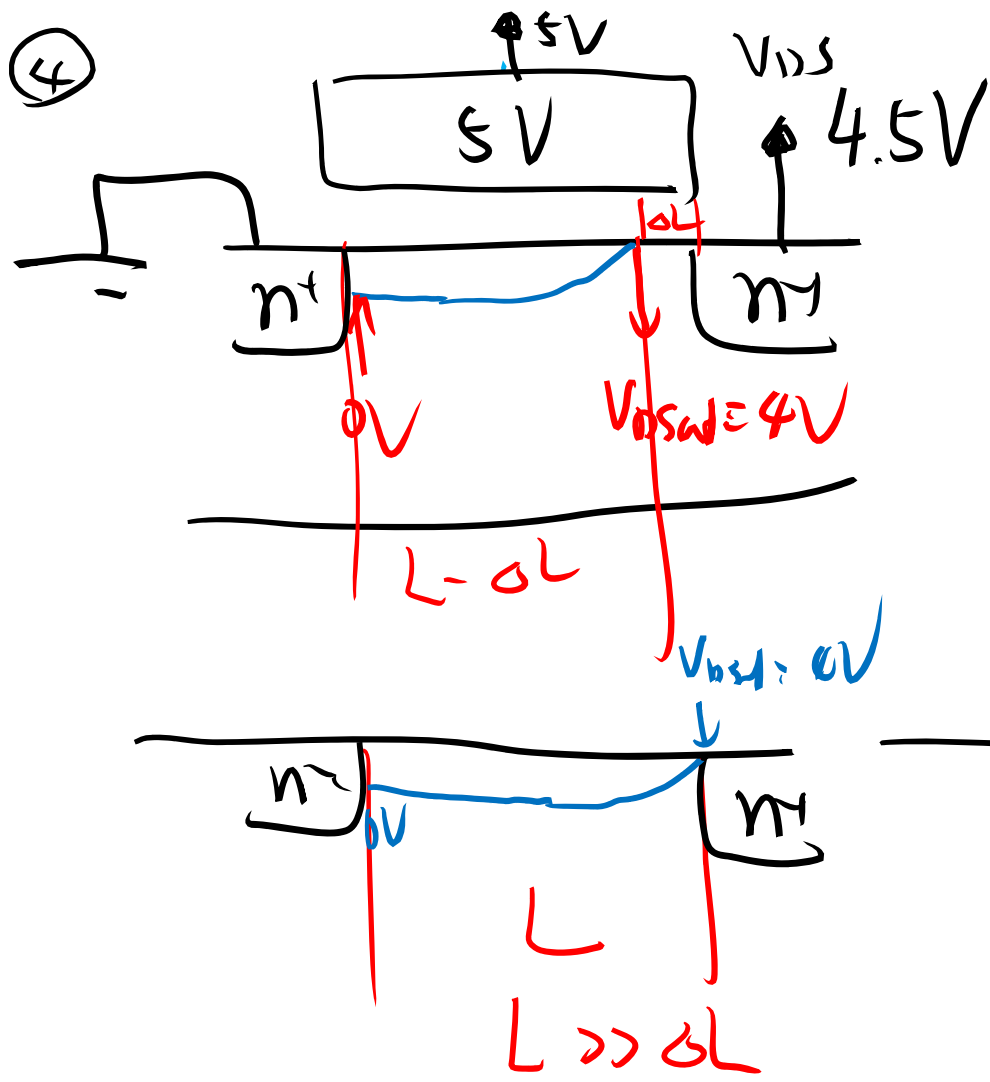
$$Q_n(y=L) = -C_{ox}(5V - 3V - 1) = -C_{ox}$$

③  $V_{D_s} = 4V = V_{Dsat} = V_{G_s} - V_T$      $Q_n = 0$



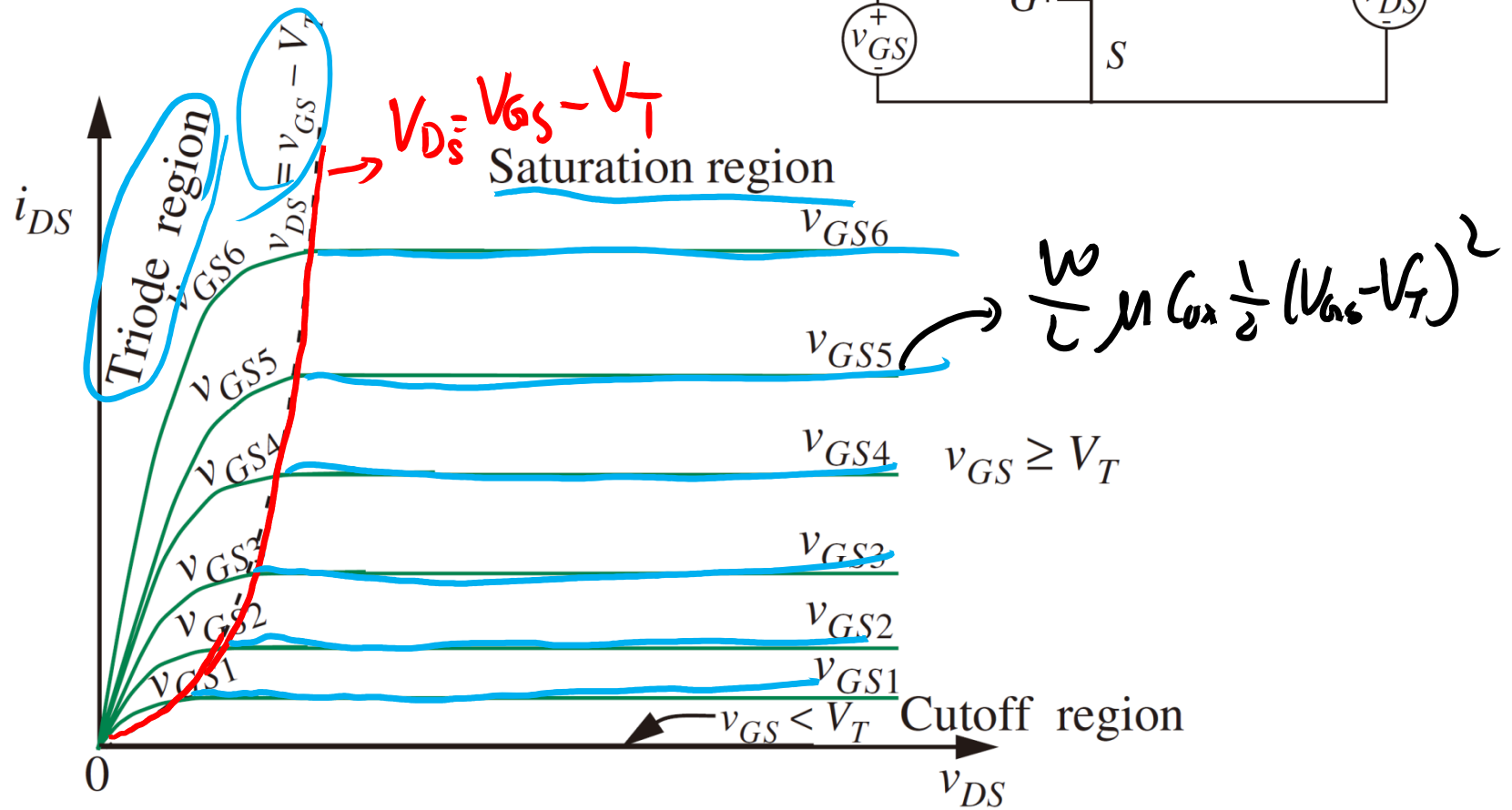
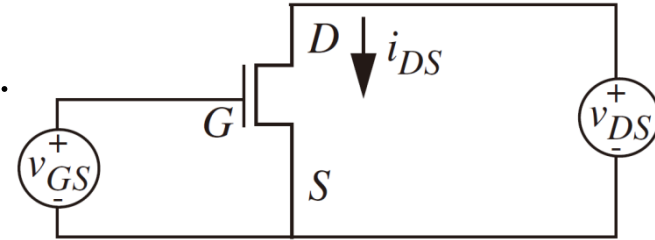


$$i = g_m V_{GS}$$

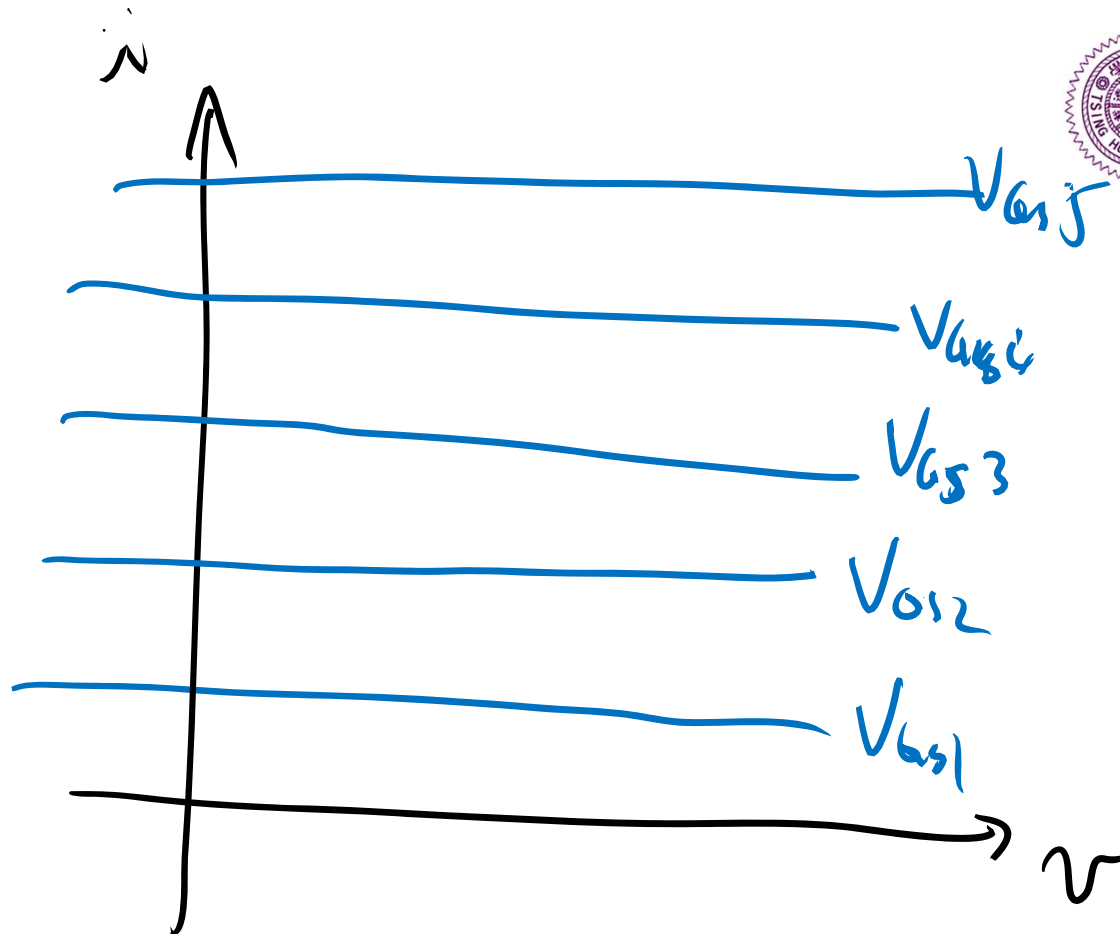


# Actual $i-v$ characteristics of the MOSFET

- Setup for observing MOSFET characteristics.

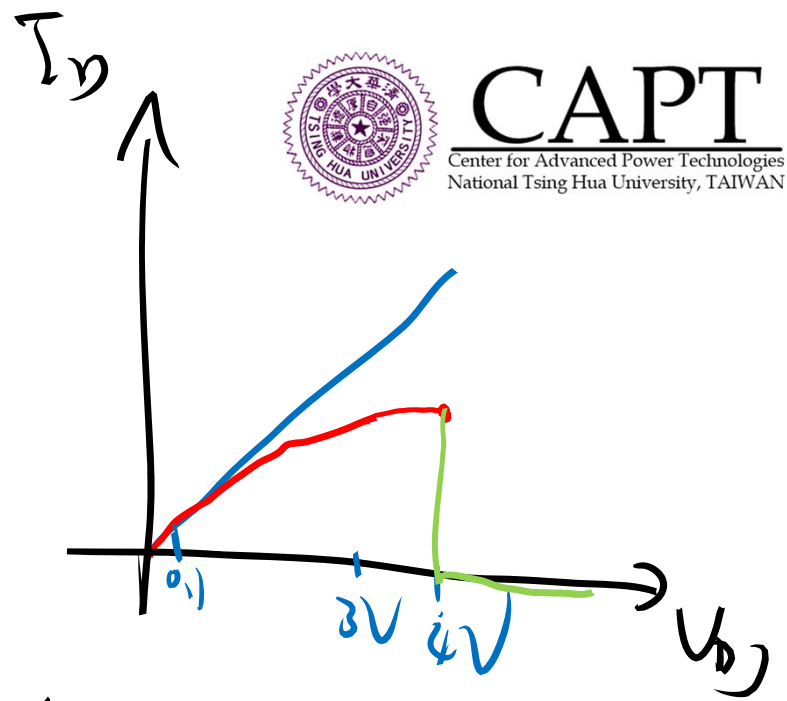
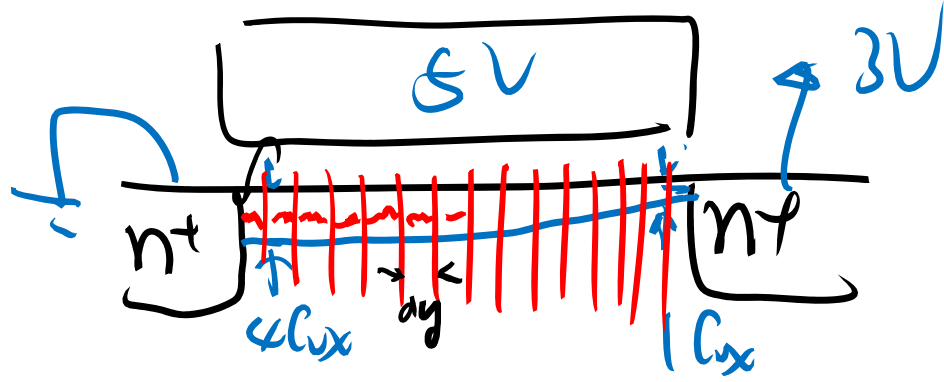


Actual  $i-v$  characteristics showing the *triode*, *saturation*, and *cutoff* regions



$$i = g_m V_{GS}$$

②  $V_{GS} = 5V$  ,  $V_{DS} = 3V$   
 $V_T = 1V$



$$R(y) = \frac{dy}{W \mu C_{ox} (V_{GS} - V_c(y) - V_T)}$$

$$dV_c(y) = I_D \cdot R(y)$$

$$dV_c(y) = \frac{I_D dy}{W \mu C_{ox} (V_{GS} - V_c(y) - V_T)}$$

$$= \int_0^L I_D dy$$



$$W\mu C_{ox} \left[ (V_{GS} - V_T)V_C - \frac{1}{2}V_C^2 \right] \Big|_0^{V_{DS}} = I_D \cdot L$$

$$I_D \cdot L = W\mu C_{ox} \left[ (V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

$$I_D = \frac{W}{L} \mu C_{ox} \left[ (V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

at  $V_{DS\text{sat}} = V_{GS} - V_T$

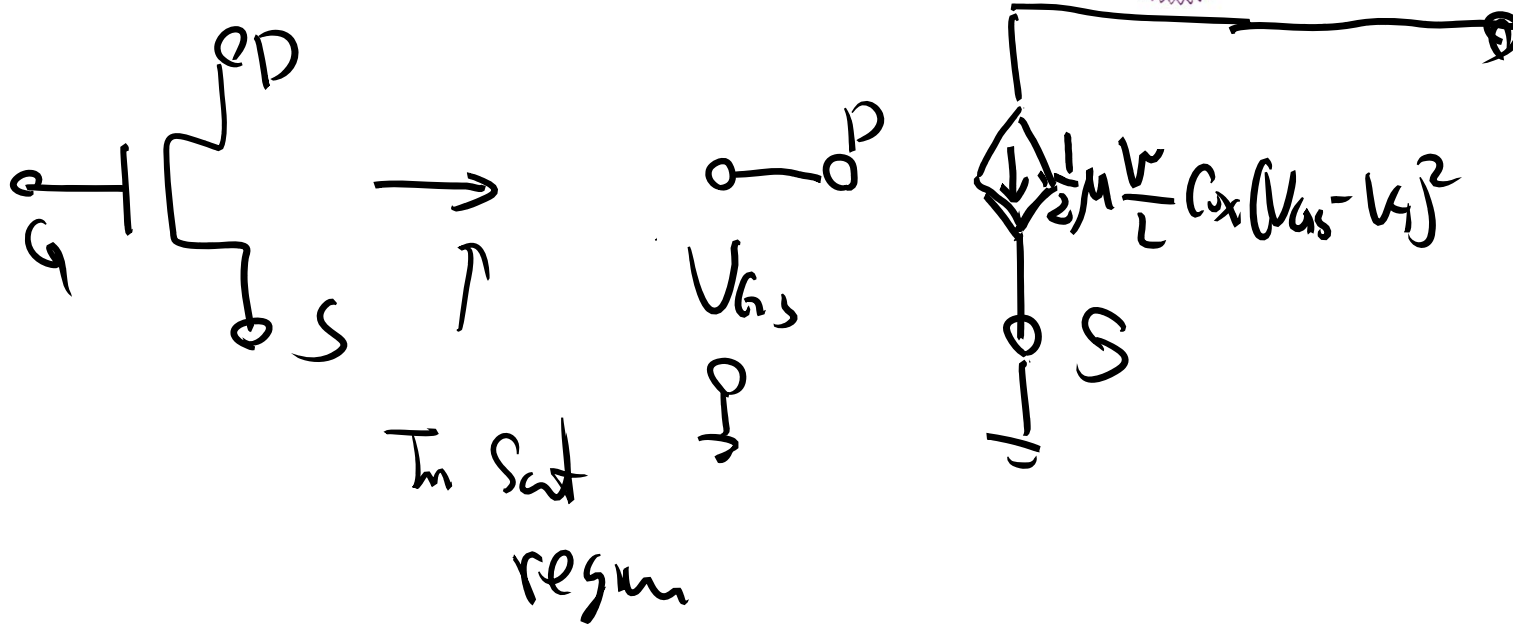
$$I_{D\text{sat}} = \frac{W}{L} \mu C_{ox} \left[ (V_{GS} - V_T)^2 - \frac{1}{2}(V_{GS} - V_T)^2 \right]$$





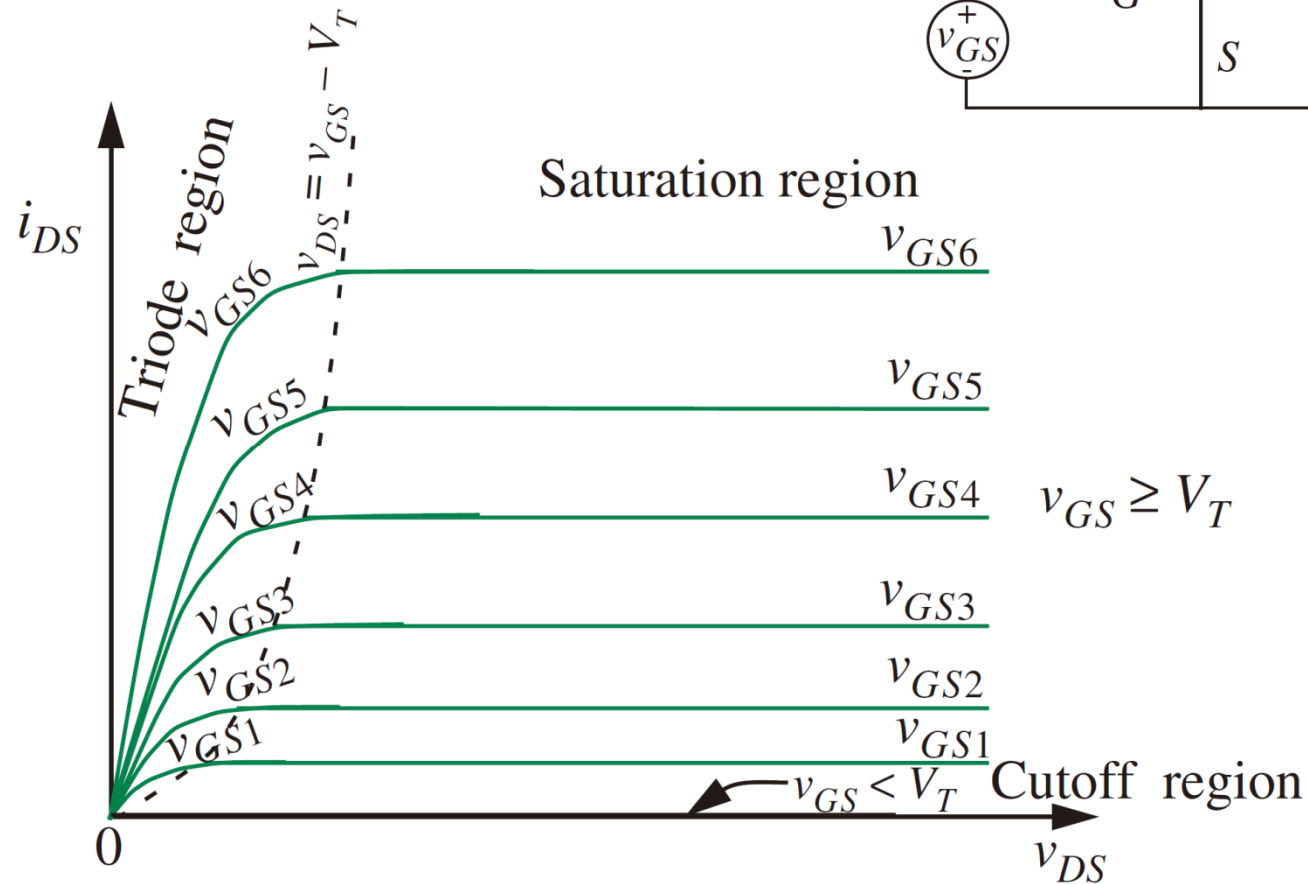
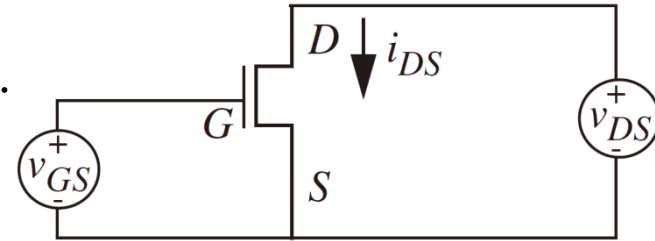


$$I_{Dsat} = \frac{W}{L} \mu C_{ox} \frac{1}{2} (V_{GS} - V_T)^2$$



# Actual $i$ - $v$ characteristics of the MOSFET

- Setup for observing MOSFET characteristics.

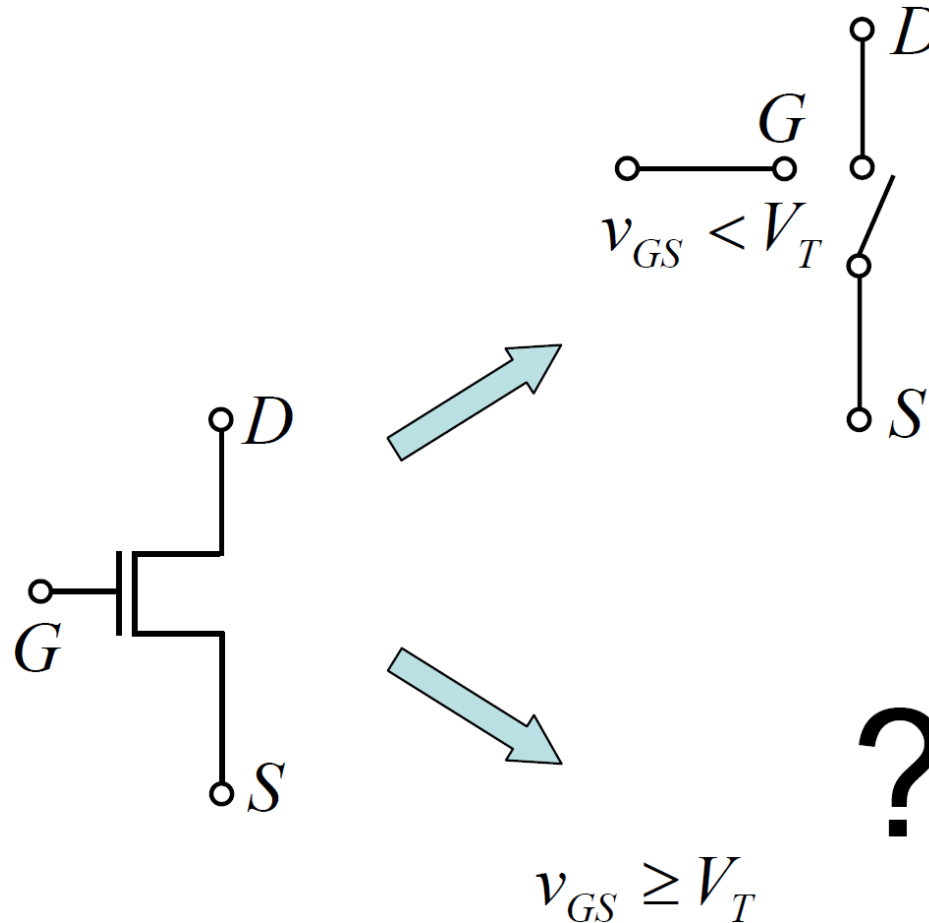


Actual  $i$ - $v$  characteristics showing the *triode*, *saturation*, and *cutoff* regions

# New Model Needed



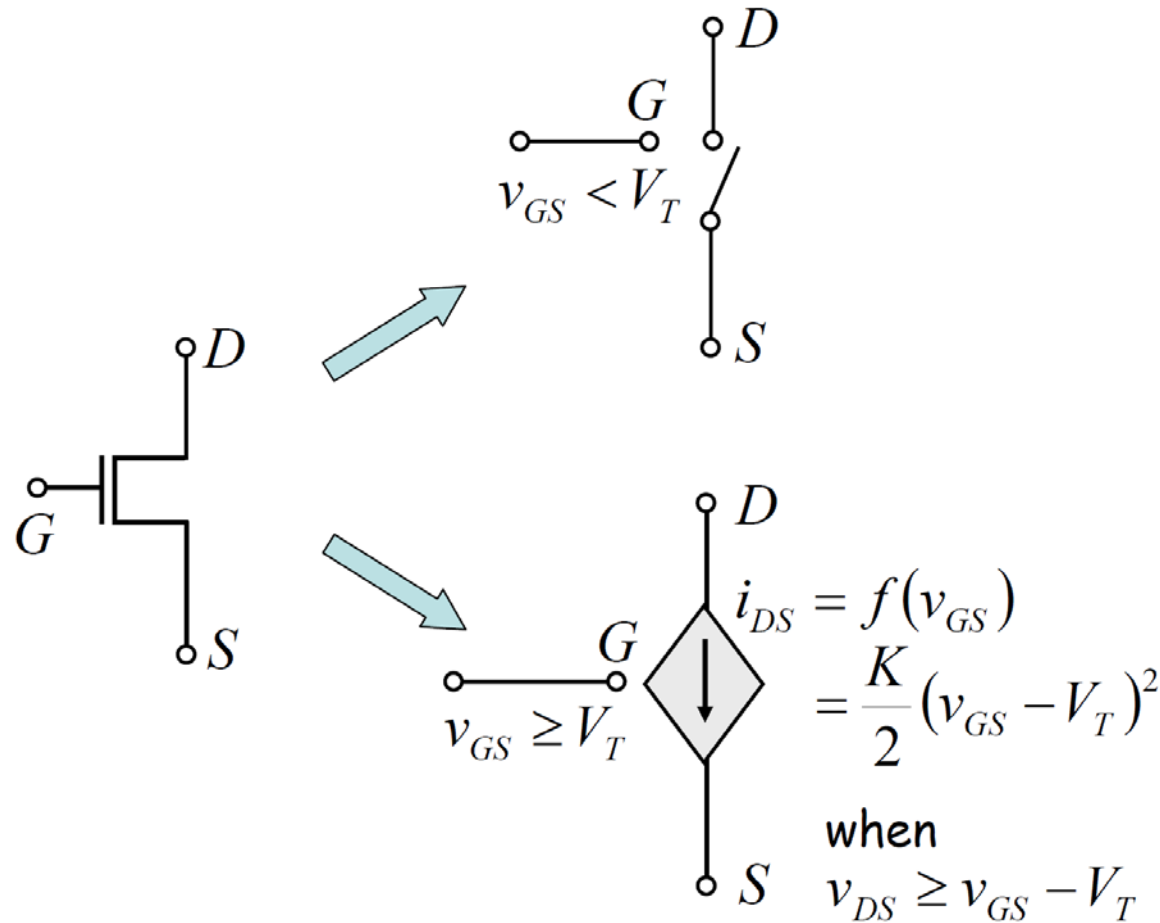
- First, we sort of lied. The on-state behavior of the MOSFET is quite a bit more complex than either the ideal switch or the resistor model would have you believe.



# SCS model of MOSFET



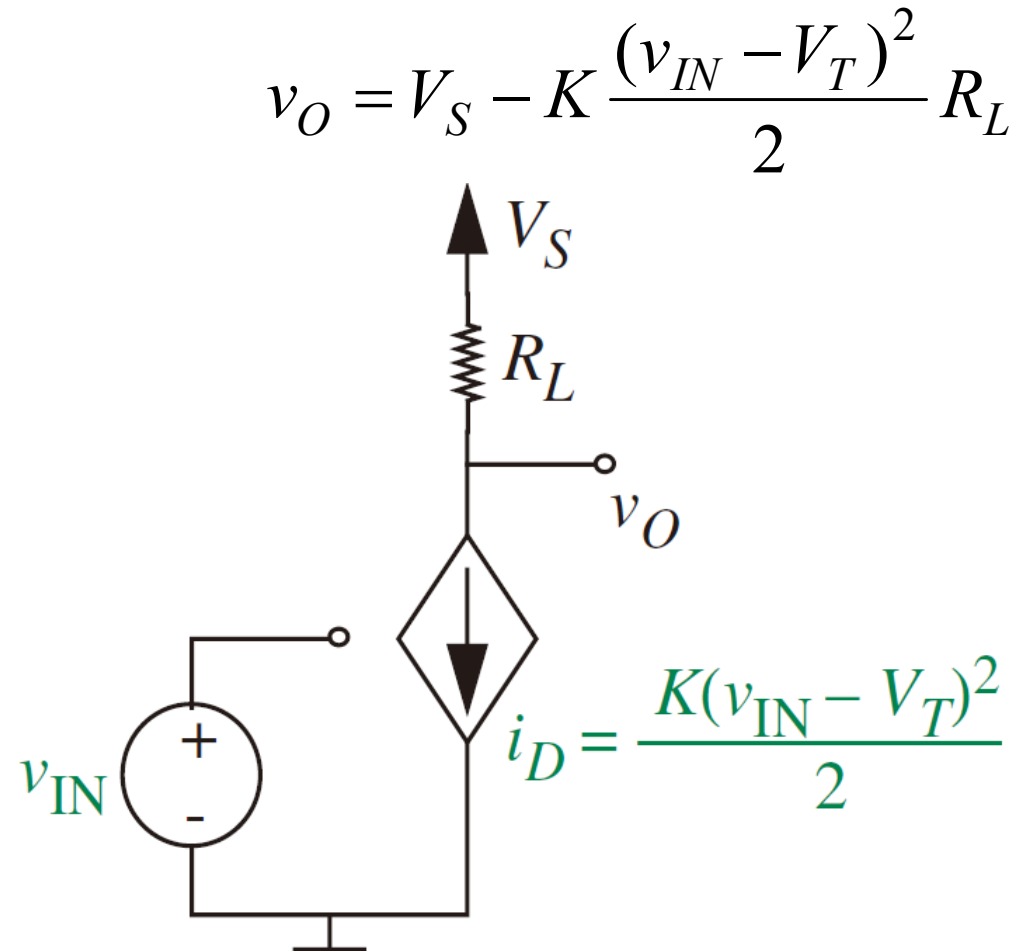
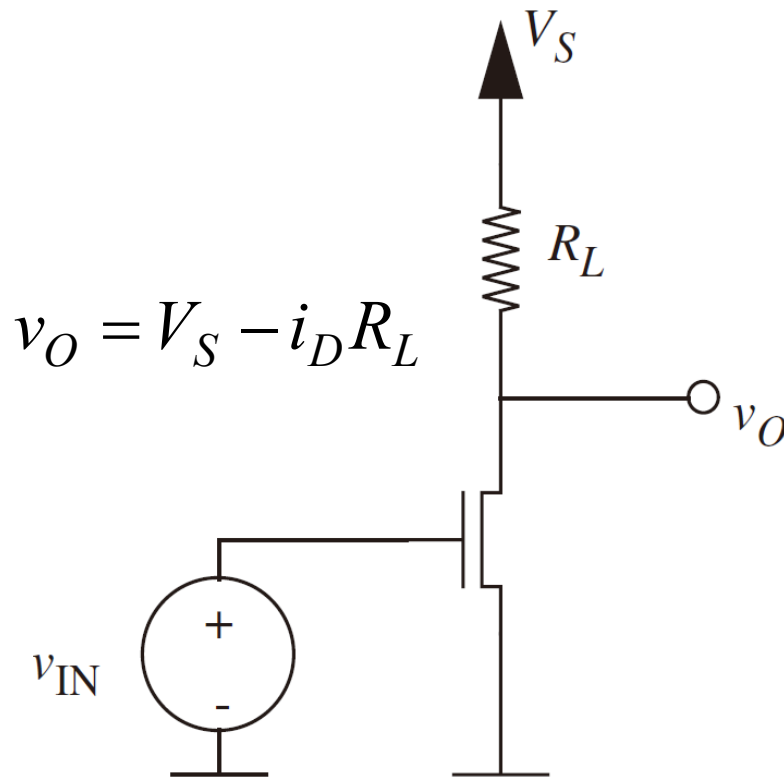
- The switch current source (SCS) model of the MOSFET
- This is more accurate than the S or SR model



# MOSFET amplifier



- Find the transfer function for the MOSFET amplifier if MOSFET operated in saturation region.

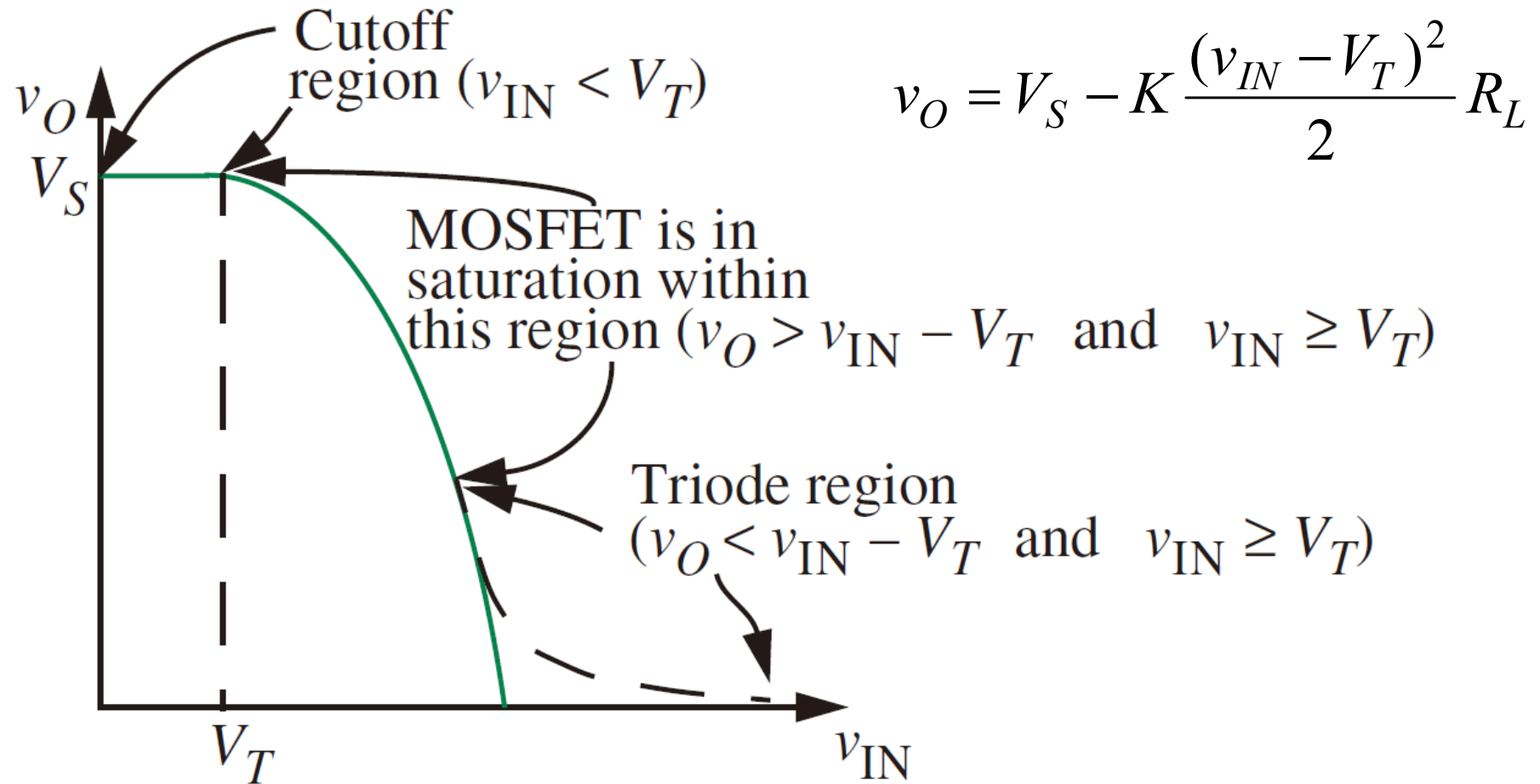


# Transfer Function with SCS Model



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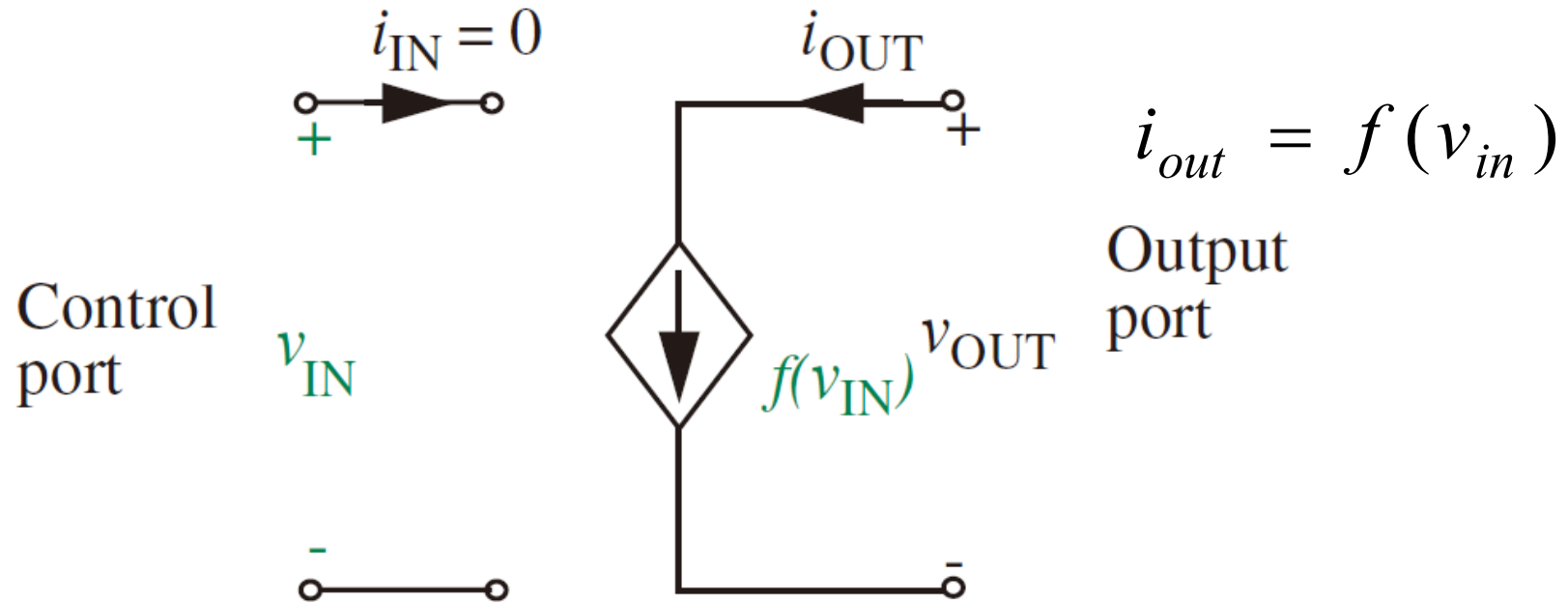
- Find the transfer function for the MOSFET amplifier if MOSFET operated in saturation region.



# Dependent Source



- New type of Element: *Dependent source*



For MOSFET

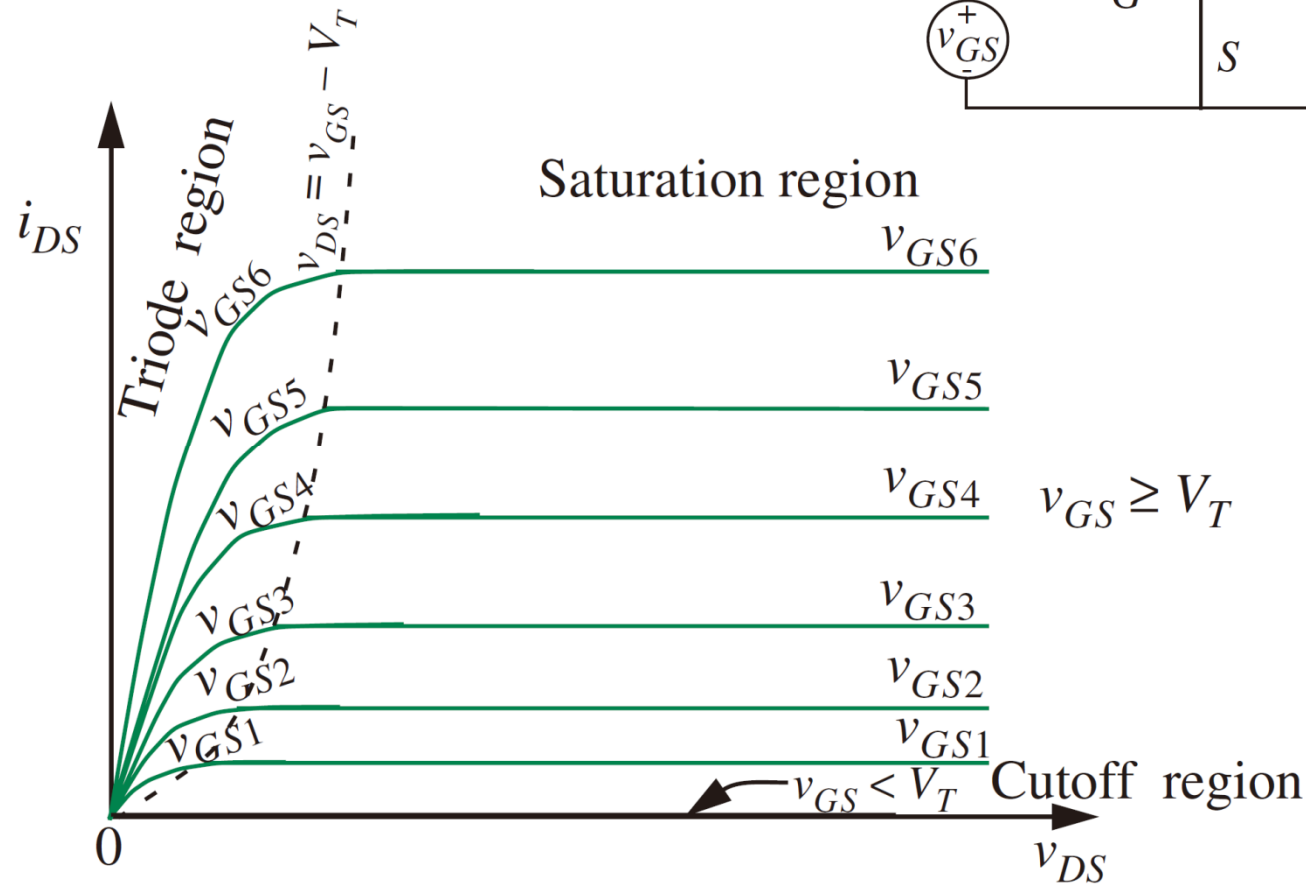
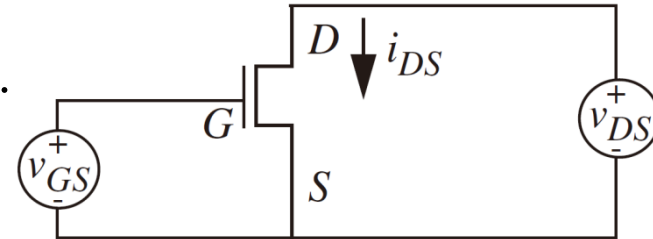
$$i_{out} = \frac{k}{2} (v_{in} - V_T)^2 \text{ for } v_{in} \geq V_T$$

$$i_{out} = 0 \text{ for } v_{in} < V_T$$

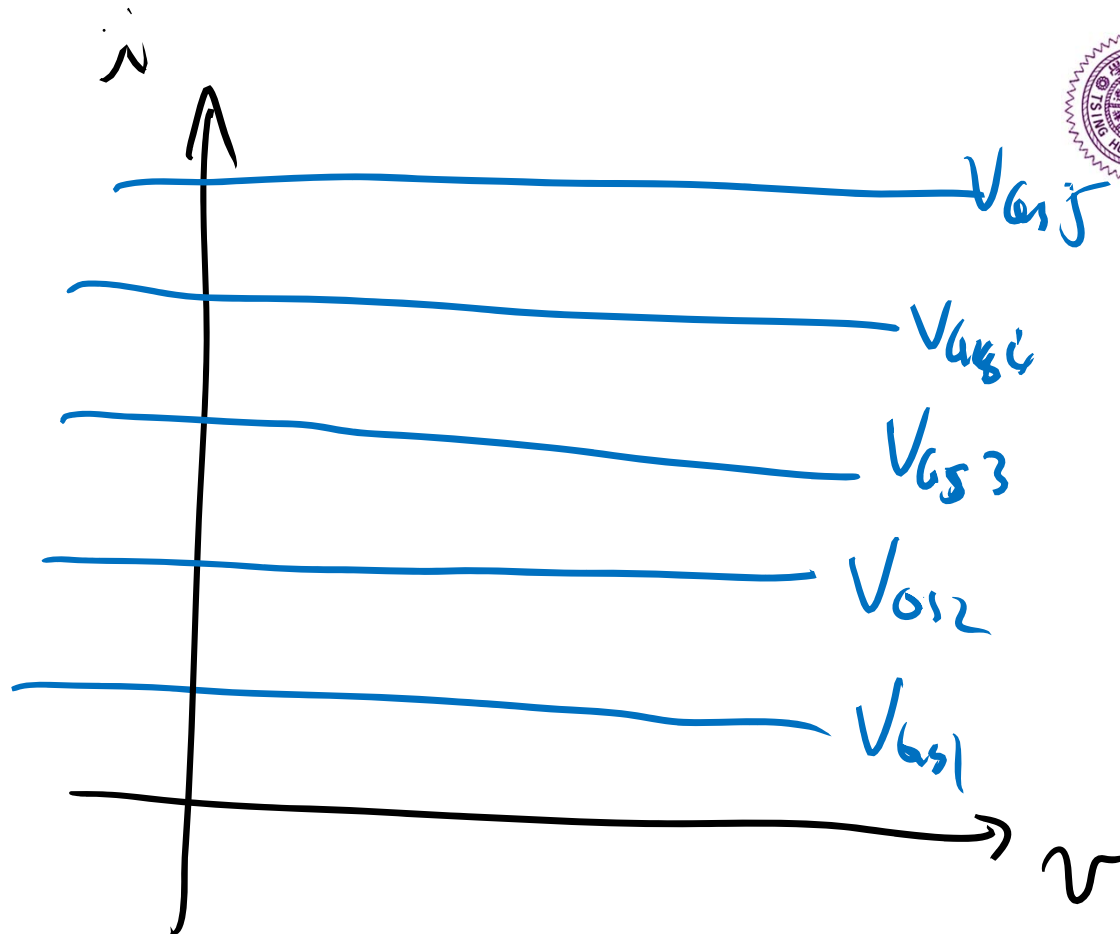


# Actual $i$ - $v$ characteristics of the MOSFET

- Setup for observing MOSFET characteristics.



Actual  $i$ - $v$  characteristics showing the *triode*, *saturation*, and *cutoff* regions



$$i = g_m V_{GS}$$

r



$$i_D = I_{D,DC} + i_d$$

DC      small signal

$$i_D = \frac{k}{2} (v_{GS} - V_T)^2$$

$$\underline{I_D} + \underline{i_d} = \frac{k}{2} (V_{GS} + v_{gs} - V_T)^2$$

$$= \frac{k}{2} (V_{GS} - V_T)^2 + \frac{k}{2} 2 (V_{GS} - V_T) v_{gs} + \frac{k}{2} v_{gs}^2$$

$$i_d = k (V_{GS} - V_T) v_{gs} + \frac{k}{2} v_{gs}^2$$

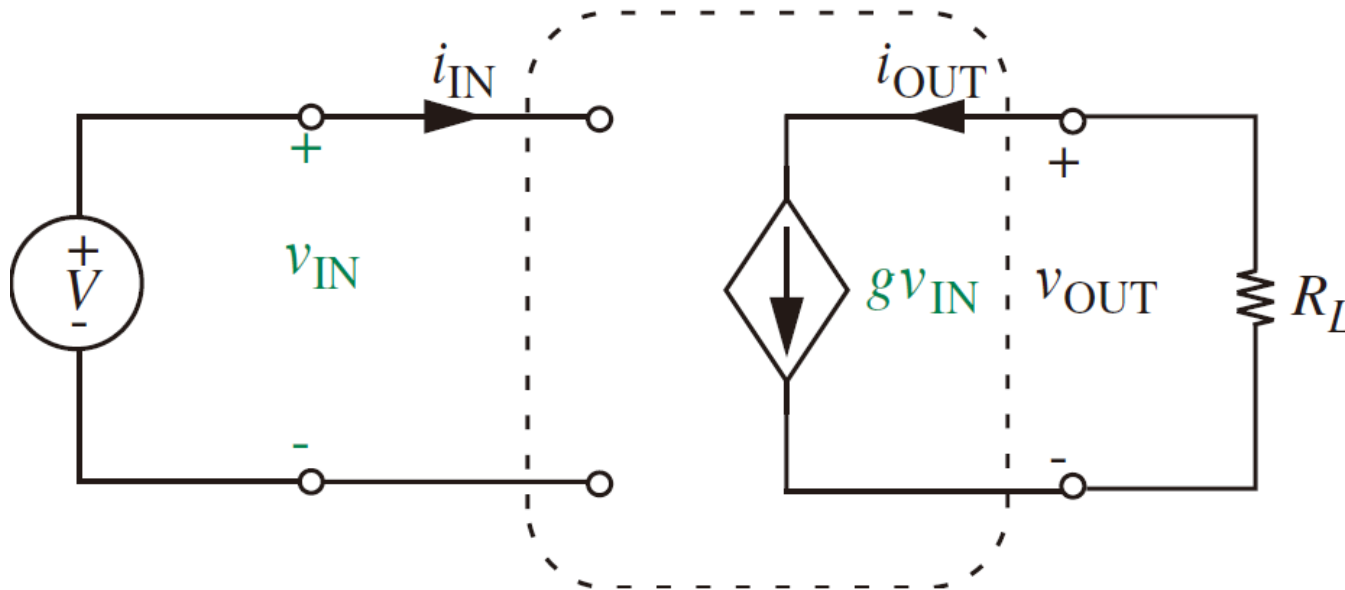
Small signal mode

$$i_d = k (V_{GS} - V_T) v_{gs} \quad \leftarrow \quad \rightarrow i_d$$

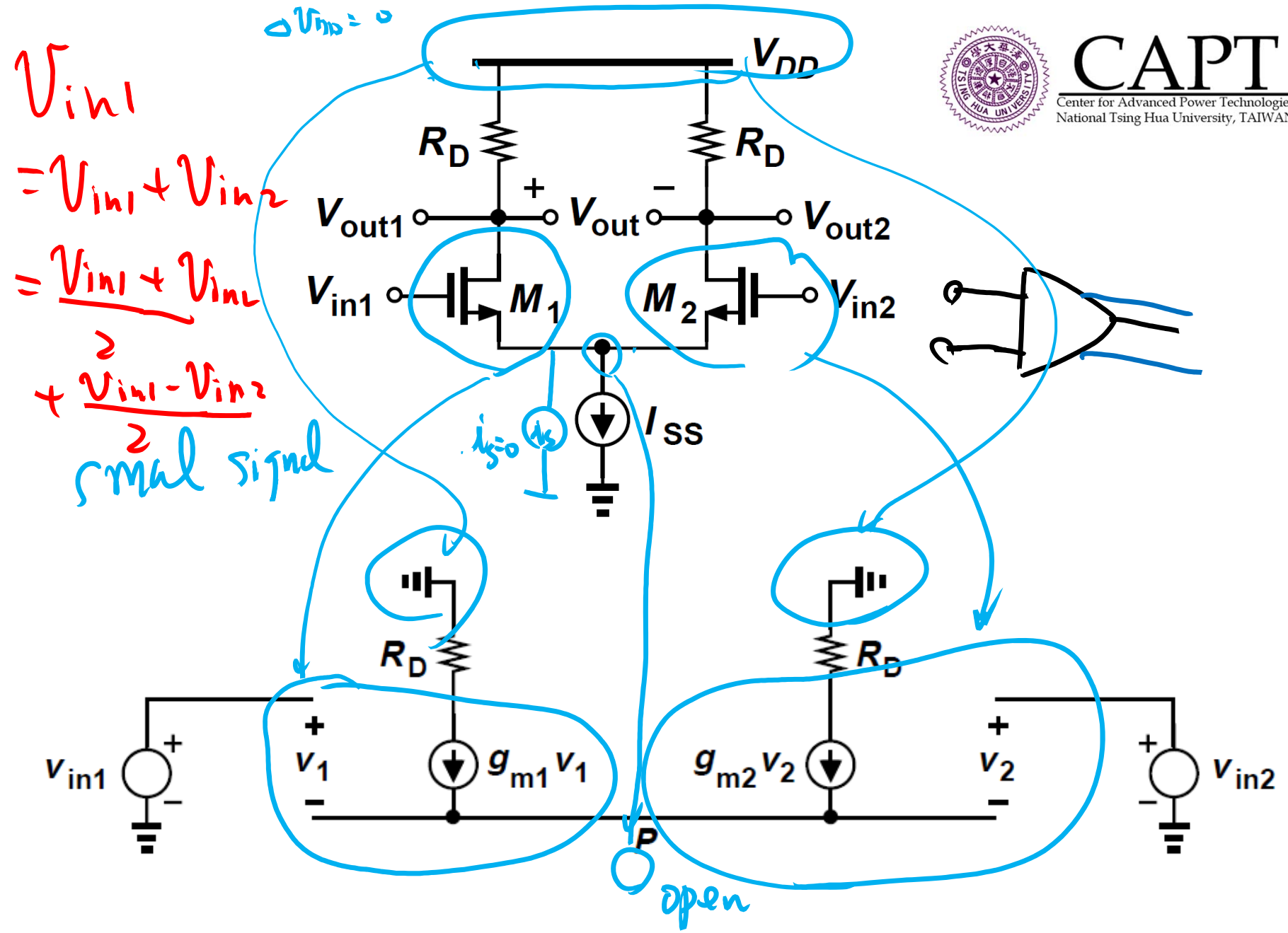
# Linear Dependent Source



- If the *Dependent source* is linear, say  $f(v_{in}) = gv_{in}$ .



- This type of dependent sources is called **voltage-controlled current source (VCCS)**. Current at output port is a function of voltage at the input port.  $g$  is called the **transconductance**.



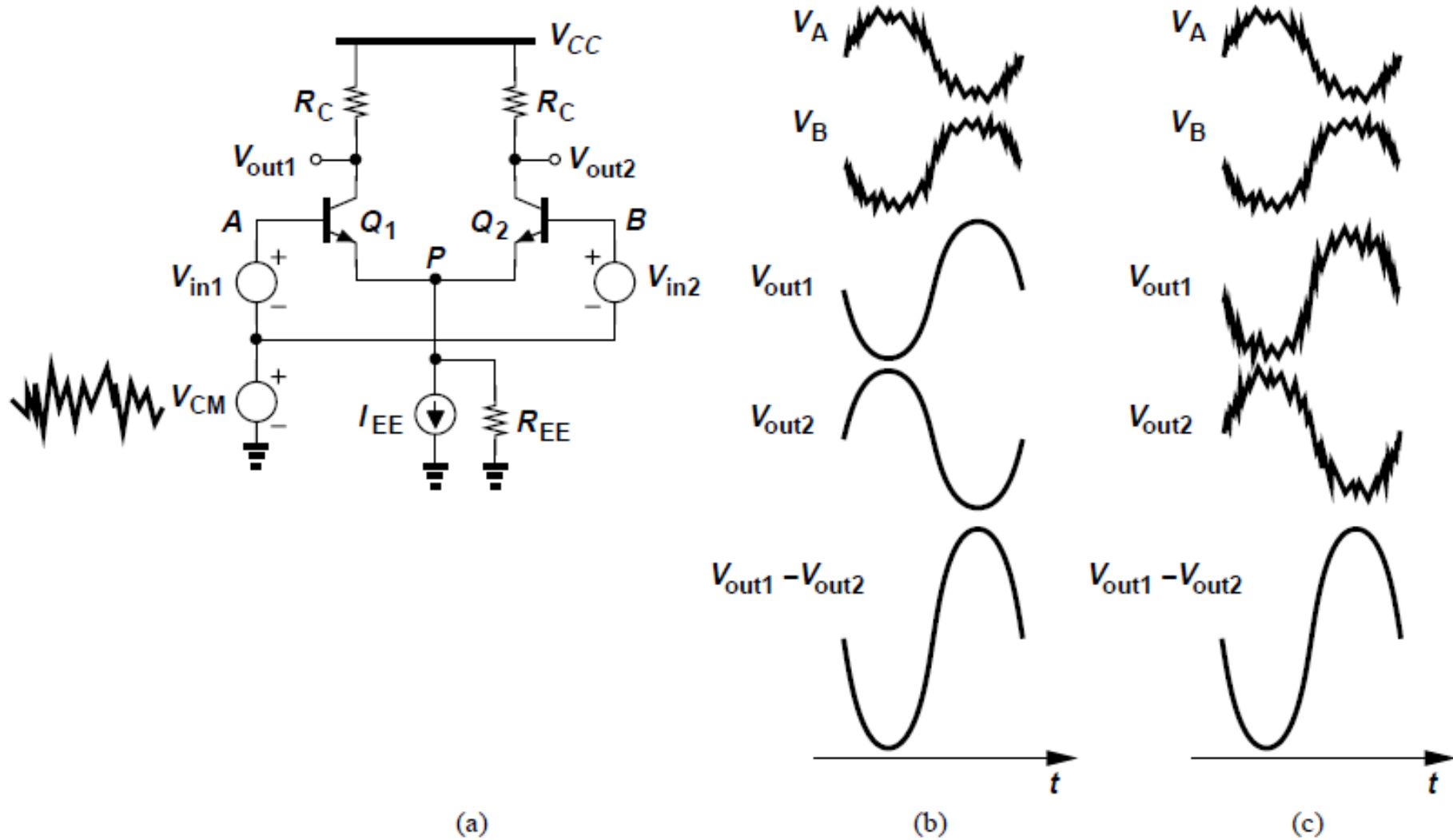


Figure 10.44 (a) Differential pair sensing input CM noise, (b) effect of CM noise at output with  $R_{EE} = \infty$ , (c) effect of CM noise at the output with  $R_{EE} \neq \infty$ .

# Noise Immunity of Diff. Amp.

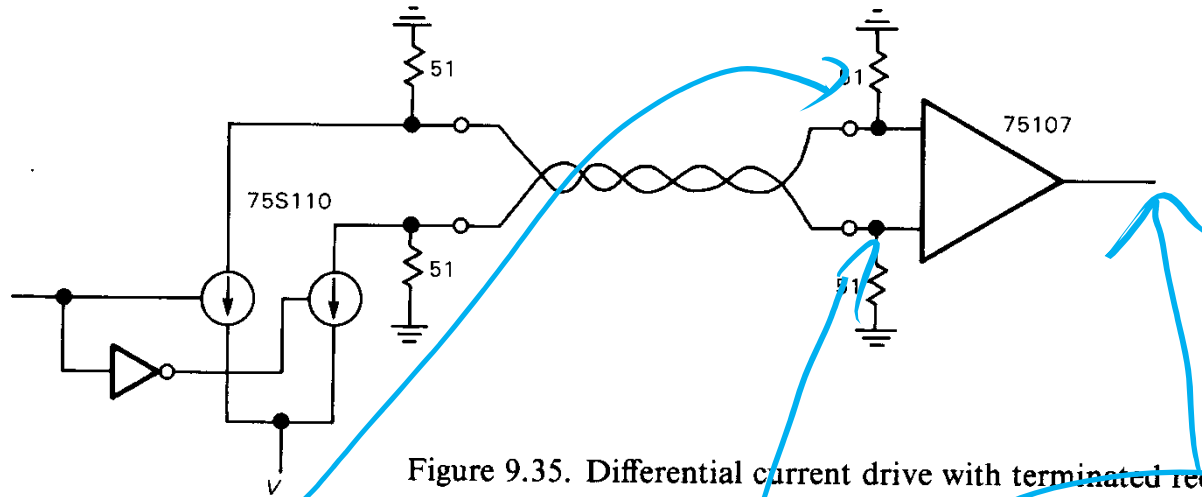


Figure 9.35. Differential current drive with terminated receiver

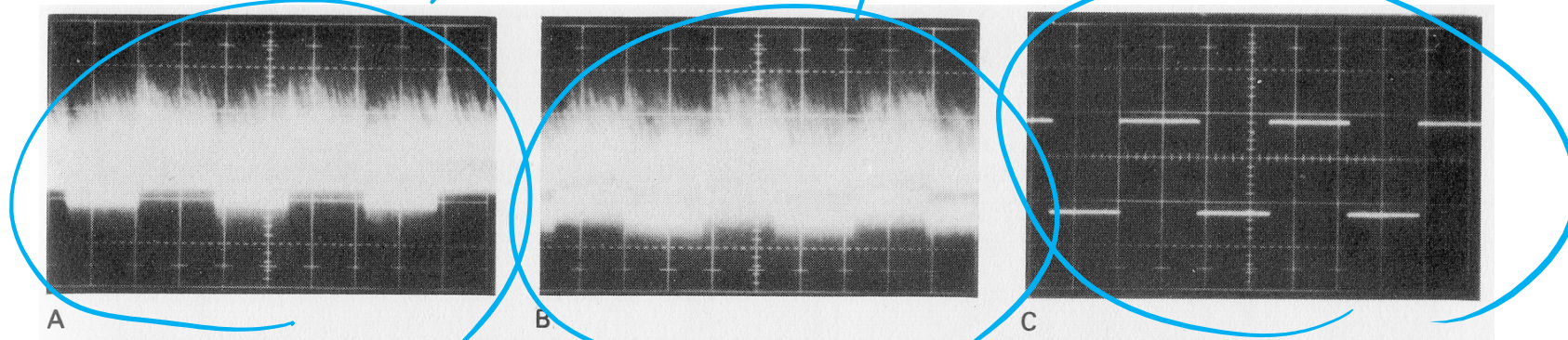
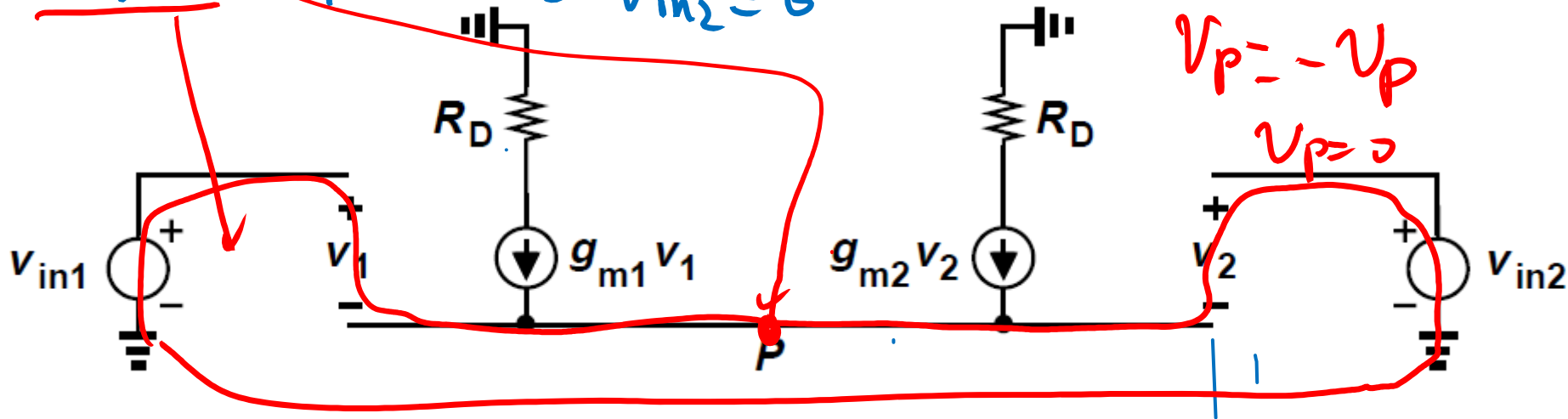


Figure 9.36. Scope photos showing excellent noise immunity of differential data transmission (75108 differential receiver). (Courtesy of Texas Instruments, Inc., Dallas, Texas.)

- A. (+) receiver input.
- B. (-) receiver input.
- C. Receiver output.



KCL:  $g_{m1}V_1 + g_{m2}V_2 = 0$   
 KVL:  $V_{in1} - V_1 + V_2 - V_{in2} = 0$   $v_p = 0$

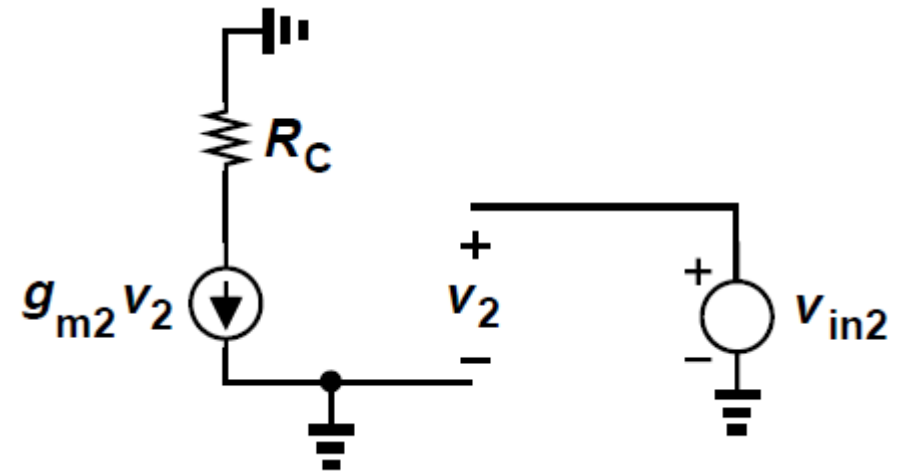
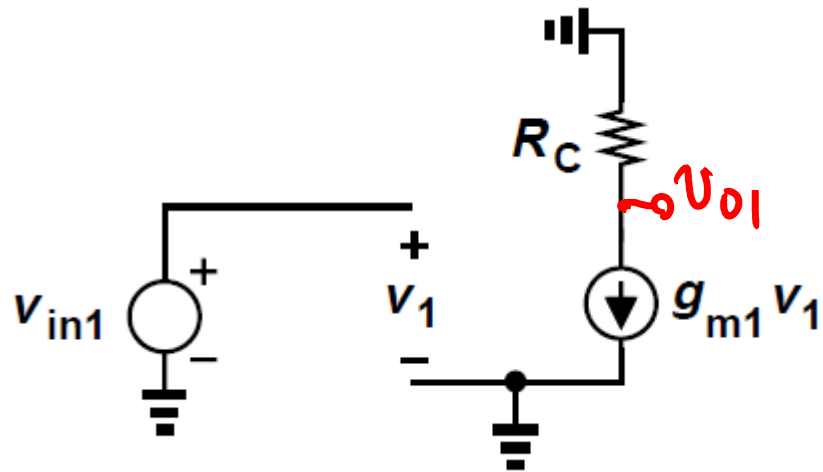


Assume  $g_{m1} = g_{m2} \Rightarrow$  from KCL  $\Rightarrow V_1 = -V_2$

$V_{in1}$  &  $V_{in2}$  are differential  $\Rightarrow V_{in1} = -V_{in2}$

KVL:  $V_{in1} - V_1 = V_{in2} - V_2 = -V_{in1} - (-V_1)$   
 $= -V_{in1} + V_1 = -(V_{in1} - V_1)$



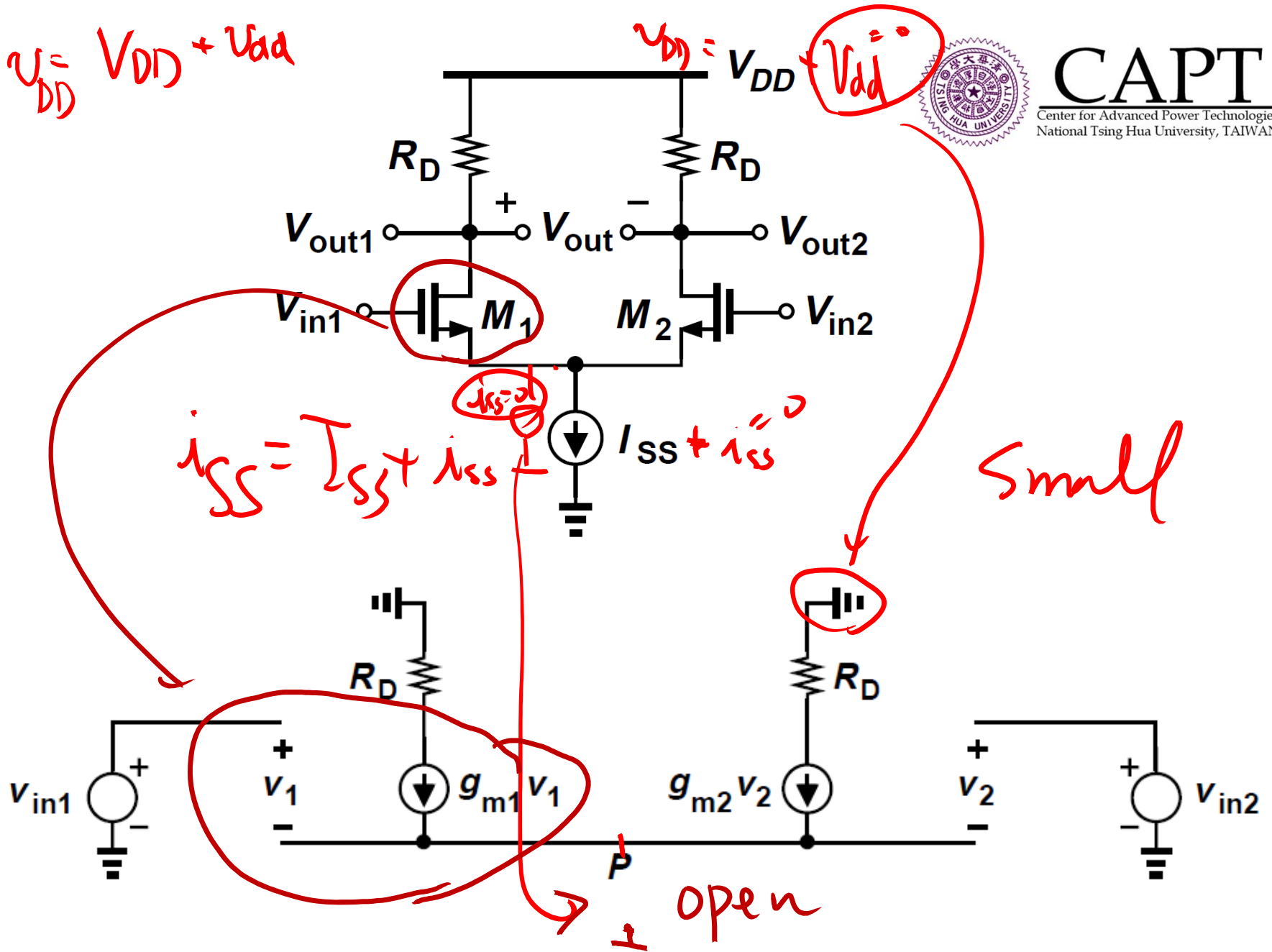


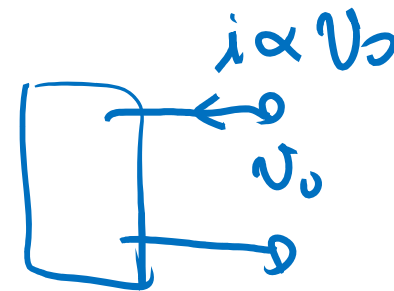
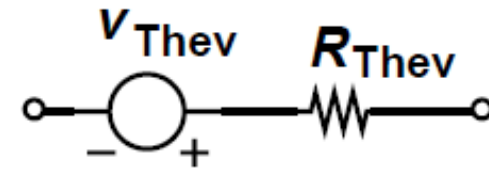
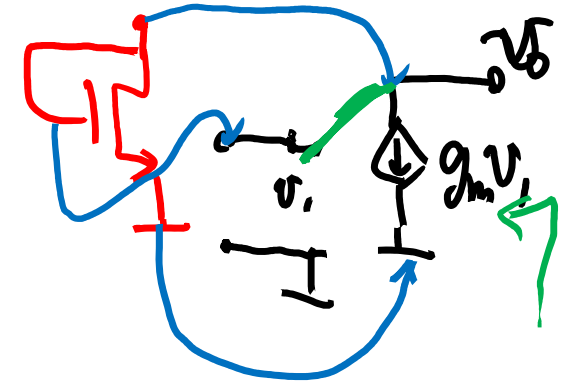
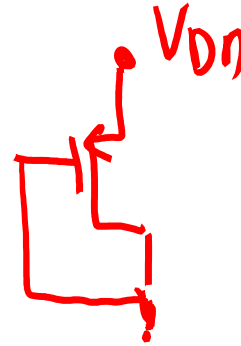
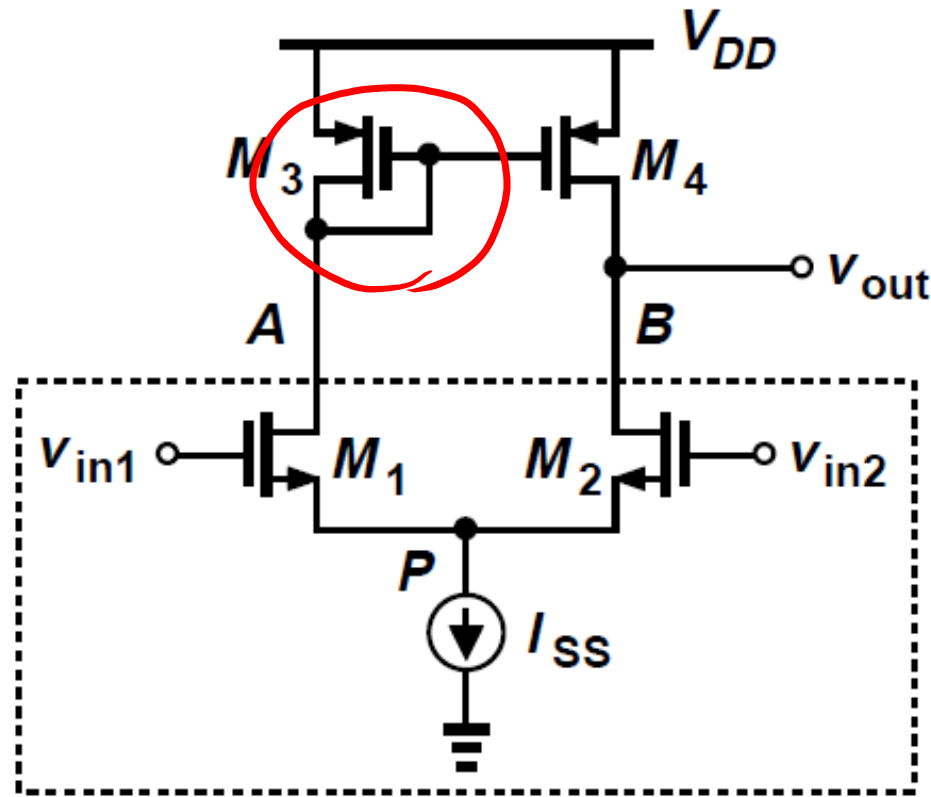
$$V_{O1} = -g_{m1} V_{in1} \cdot R_C$$

$$V_{O2} = -g_{m2} V_{in2} \cdot R_C$$

$V_{DD} = V_{DD} + V_{add}$

$V_{DD} = V_{DD} + V_{add}$





$$\equiv \frac{1}{r} = \frac{i_o}{v_o} = \frac{v_o}{g_m v_o} = \frac{1}{g_m}$$

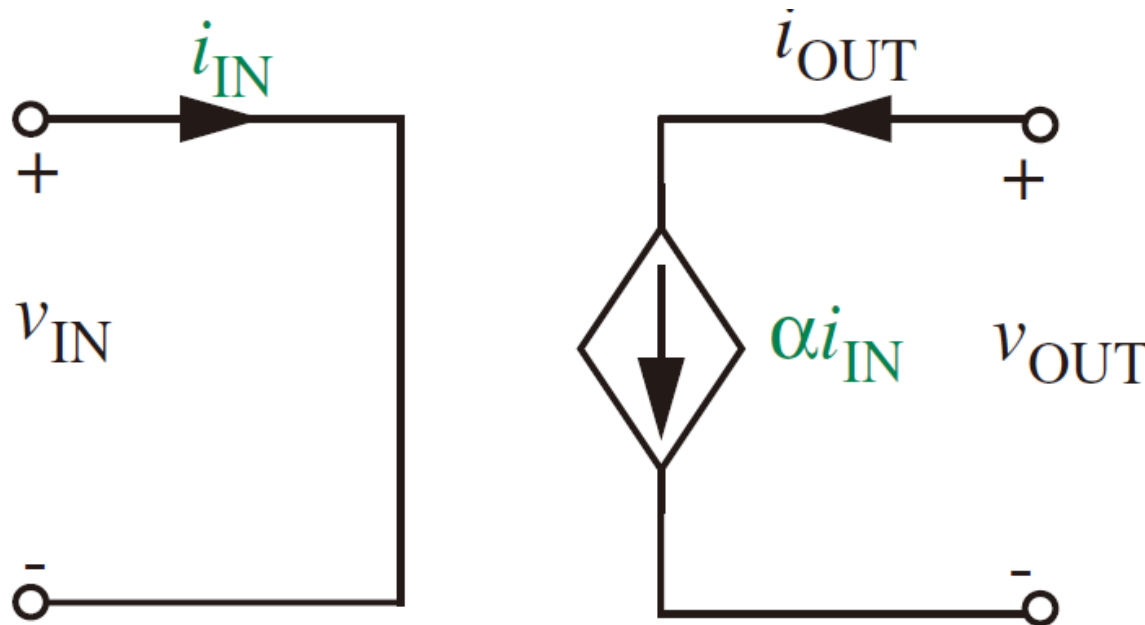
# Other Linear Dependent Source



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- There are 4 types of linear dependent sources : (a) *Voltage-controlled current source* (VCCS); (b) *Current-controlled current source* (CCCS); (c) *Voltage-controlled voltage source* (VCVS); (d) *Current-controlled voltage source* (CCVS).
- *Current-controlled current source* (CCCS) with  $\alpha$  referred as current transfer ratio.



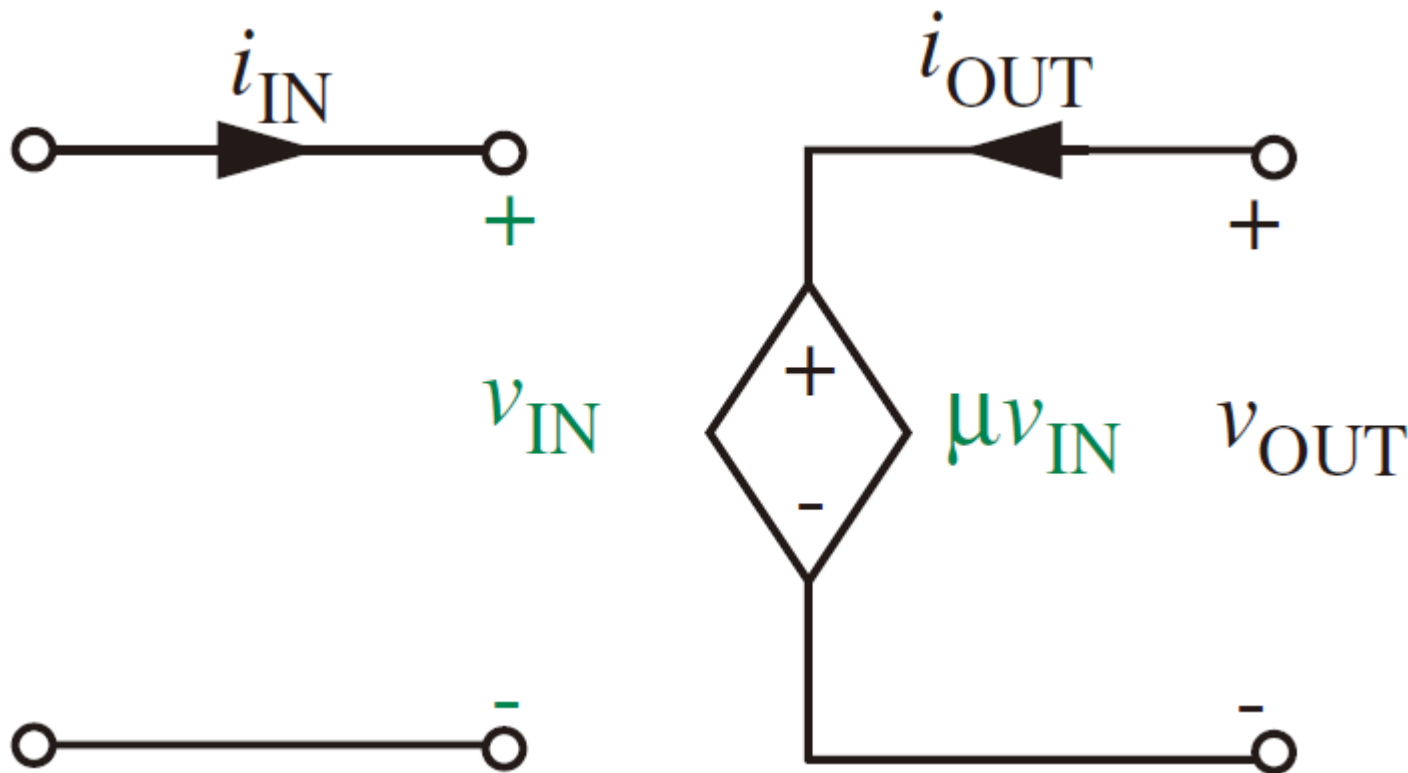
# Other Linear Dependent Source



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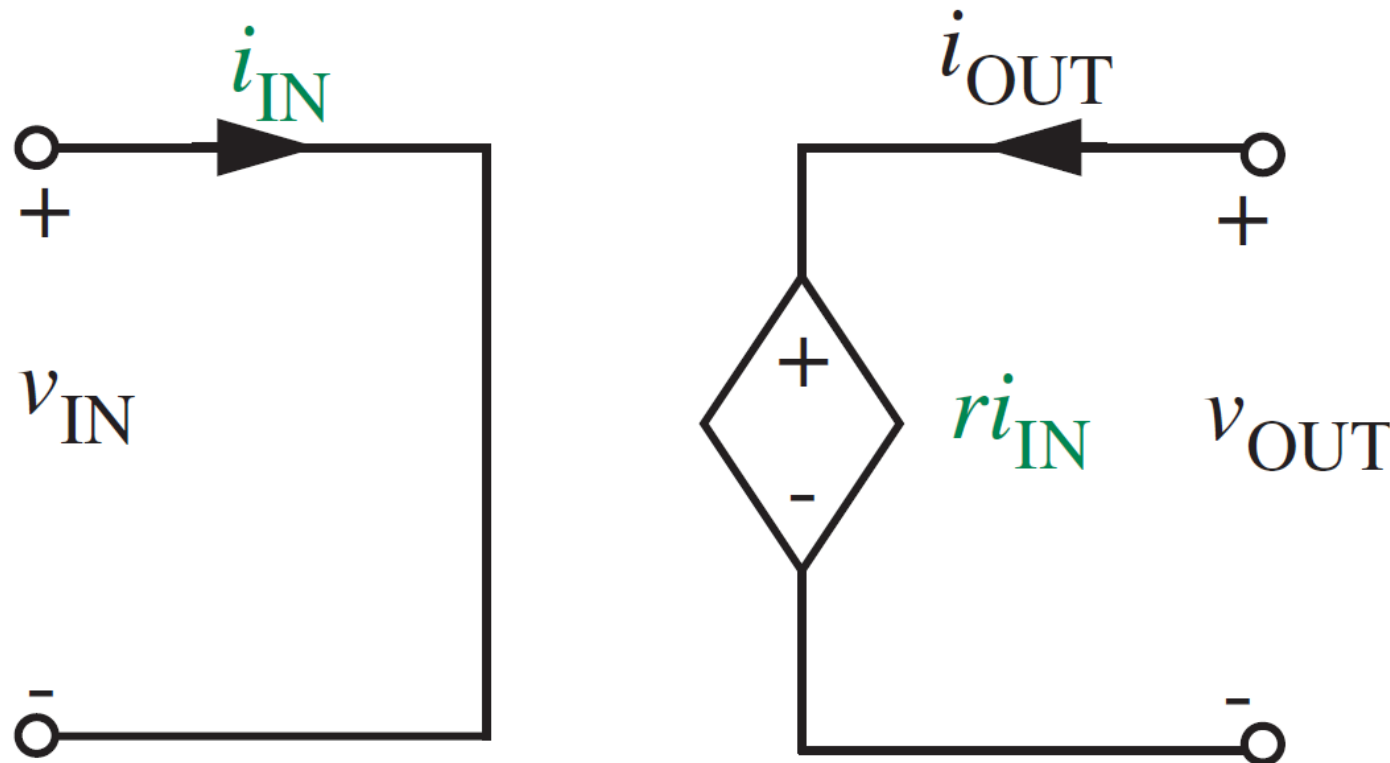
- *Voltage-controlled voltage source* (VCVS) with  $\mu$  is referred to as a voltage transfer ratio.



# Other Linear Dependent Source



- *Current-controlled voltage source* (CCVS) with  $r$  is referred to as a transresistance.



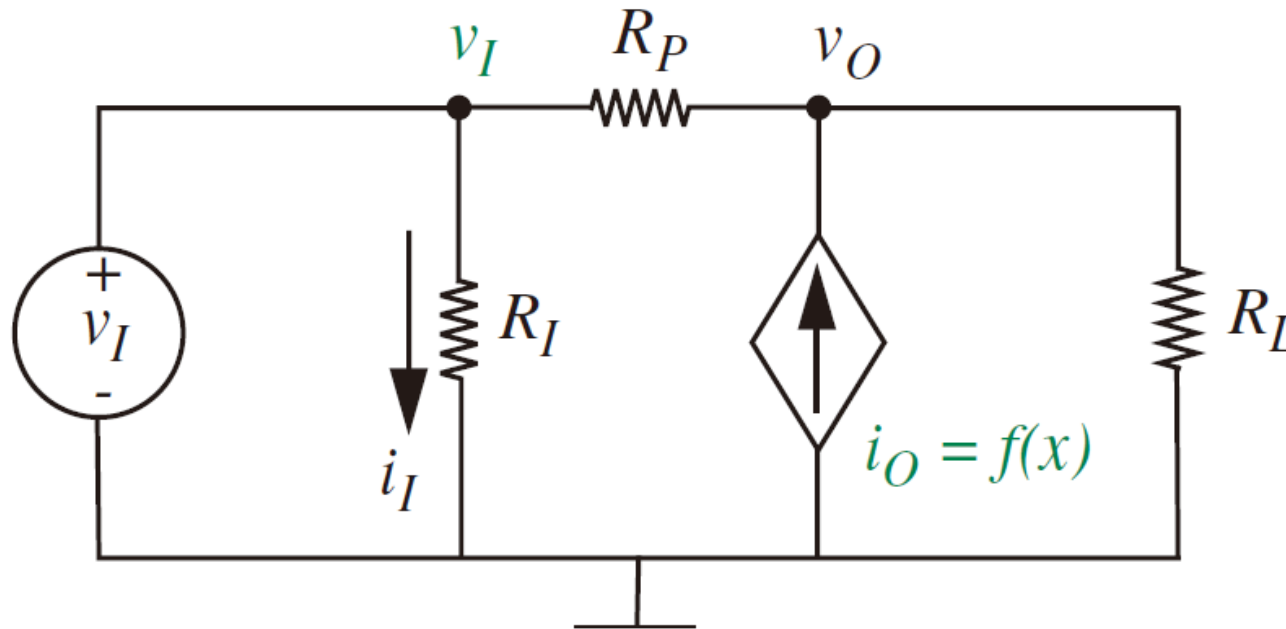
# Dependent Source and Node Eqs



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- Find  $v_O/v_I$  of the following circuit, for (1)  $i_O = -G_m v_I$  and (2)  $i_O = -\beta i_I$ .



$$\frac{v_I - v_O}{R_p} + i_O = \frac{v_O}{R_L}$$

$$i_O = -G_m v_I$$

$$\frac{v_I - v_O}{R_p} - G_m v_I = \frac{v_O}{R_L}$$

$$\frac{v_O}{v_I} = \frac{(1 - G_m R_p) R_L}{R_p + R_L}$$

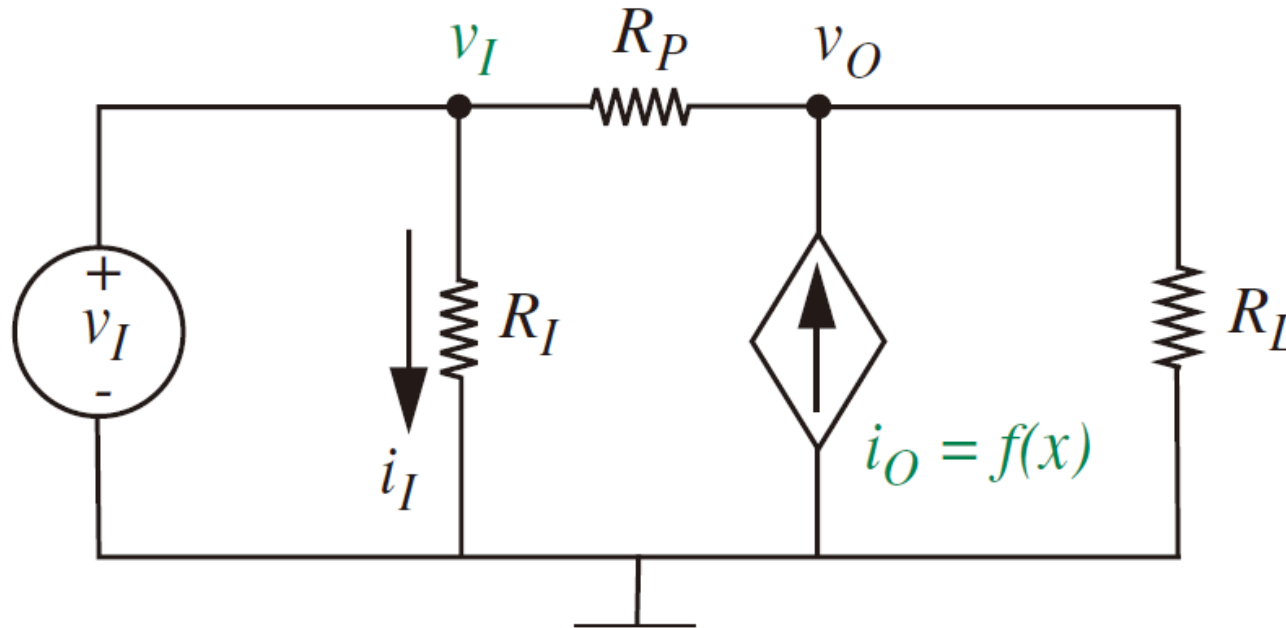
# Dependent Source and Node Eqs



CAPT

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$$\frac{v_I - v_O}{R_p} + i_O = \frac{v_O}{R_L}$$

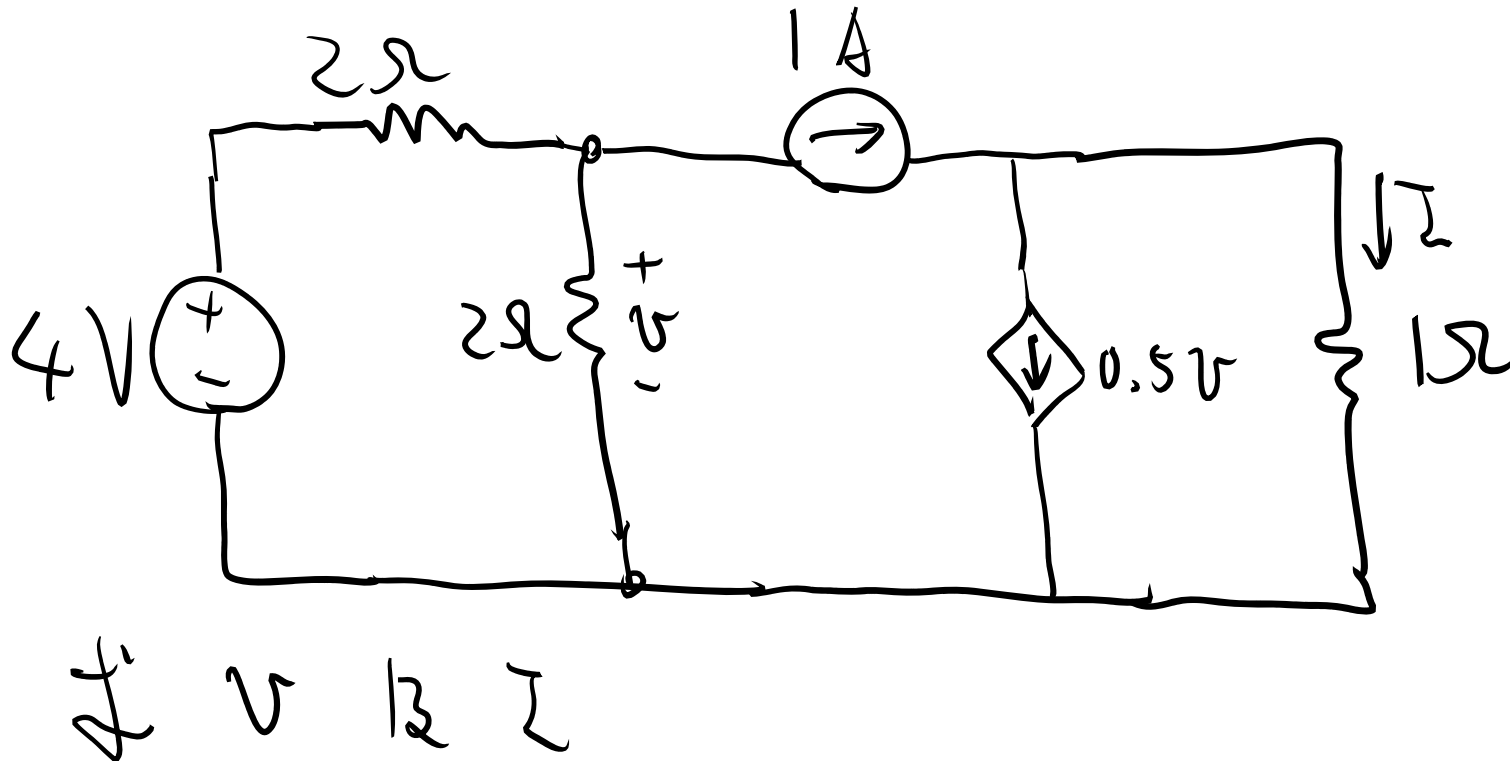
$$i_O = -\beta i_I = -\beta \frac{v_I}{R_I}$$

$$\frac{v_I - v_O}{R_p} - \beta \frac{v_I}{R_I} = \frac{v_O}{R_L}$$

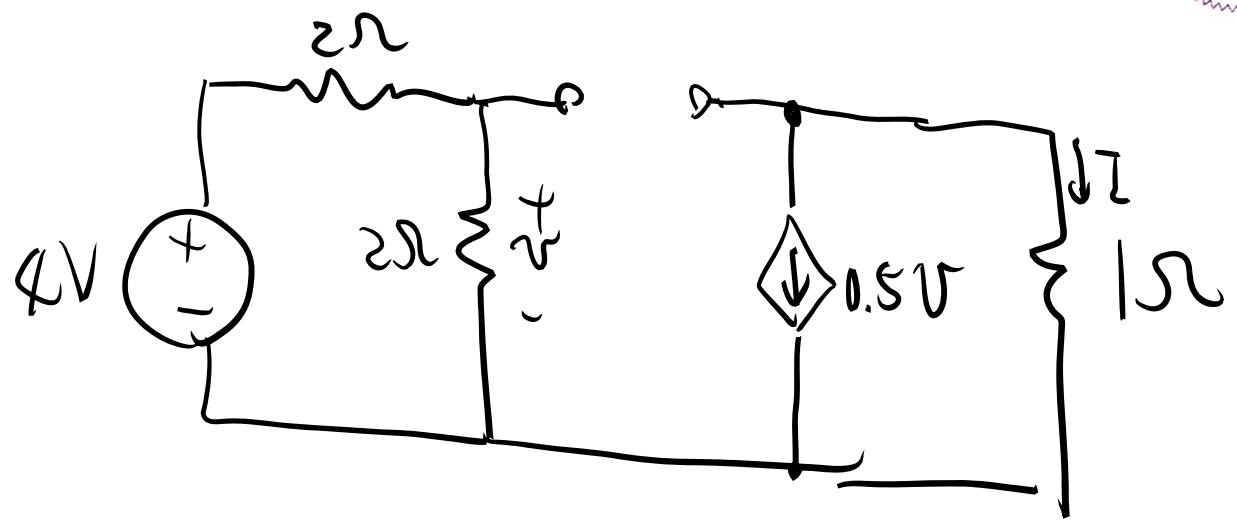
$$\frac{v_O}{v_I} = \frac{\left(1 - \beta \frac{R_p}{R_I}\right) R_L}{R_p + R_L}$$



# Superposition

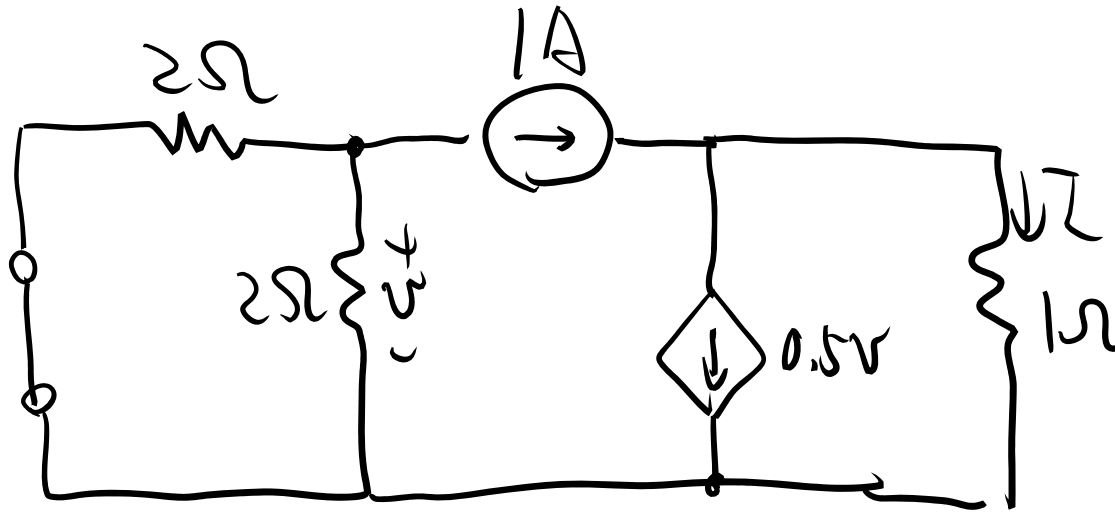


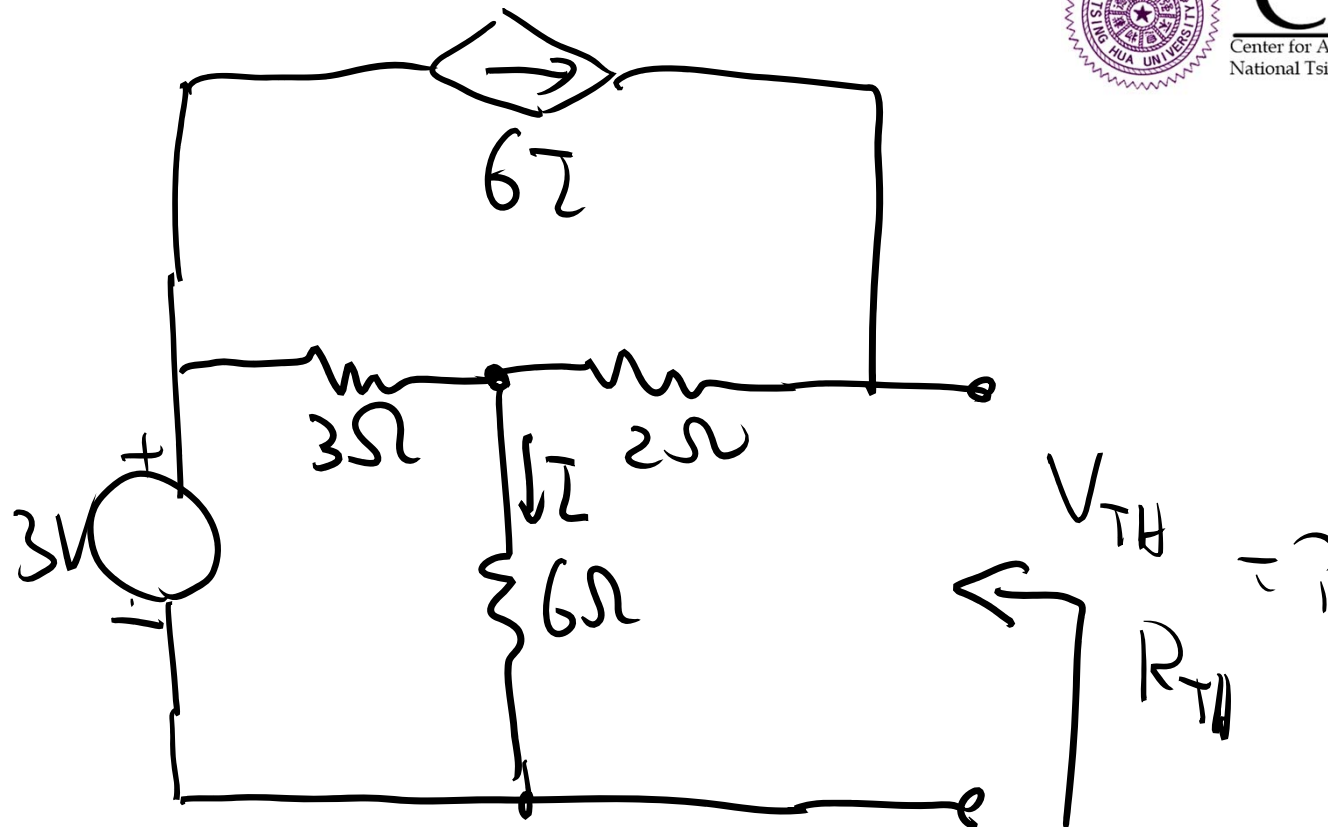
① 4V only

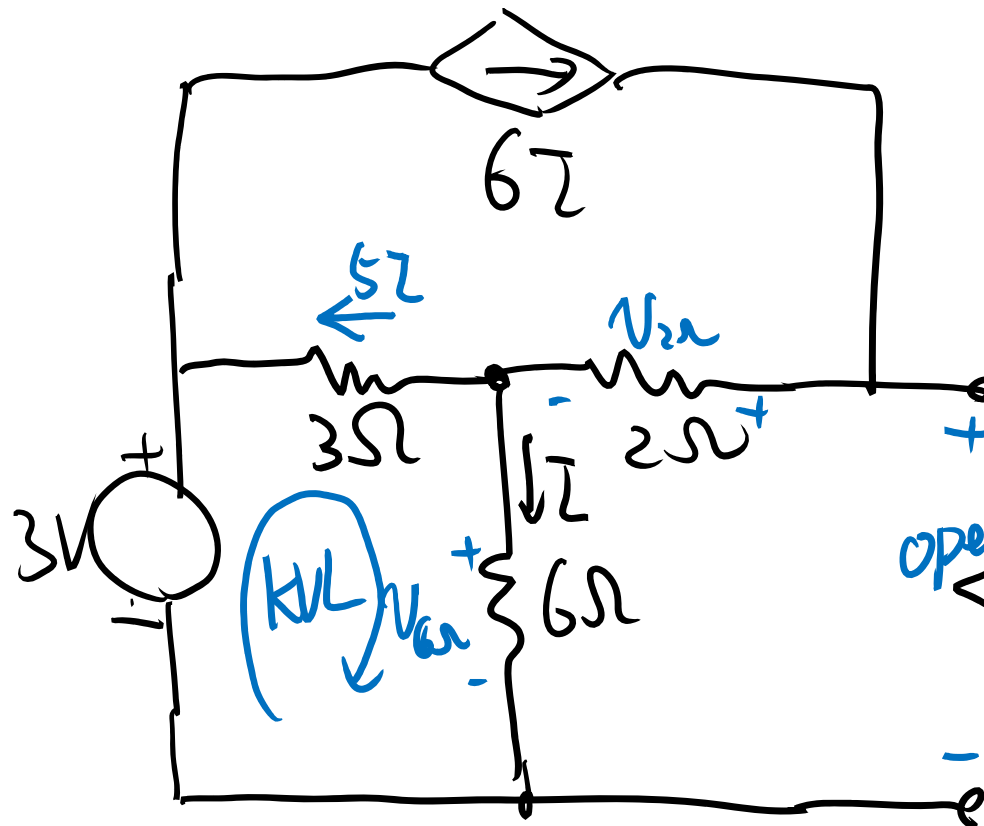


②

1A only







$$V_{TH} = -6V$$

$$V_{TH} = V_{oc}$$

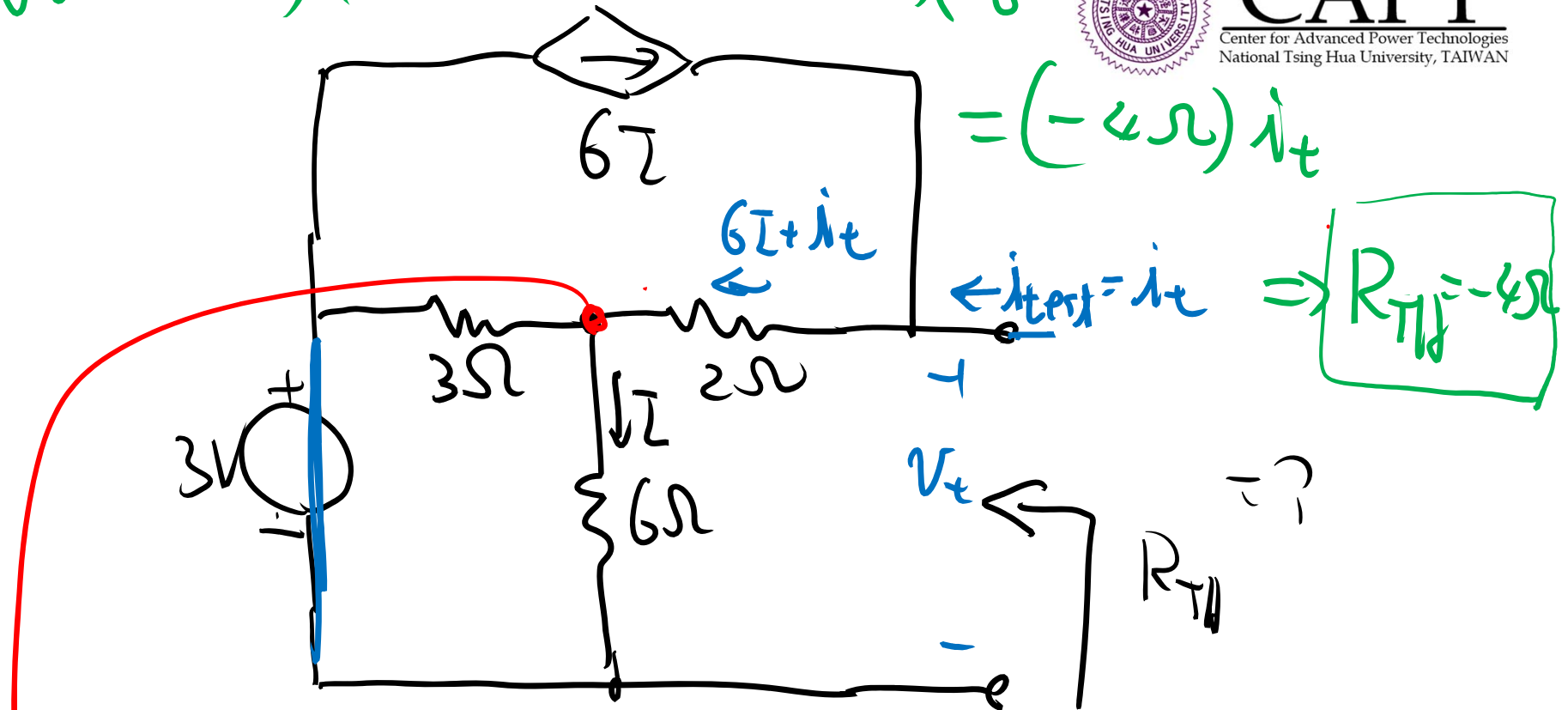
$$+(6\Omega)I - 3V - (3\Omega)(5A) = 0$$

$$-3V - 9I = 0$$

$$I = -\frac{1}{3}A$$

$$\begin{aligned} V_{TH} = V_{oc} &= (6\Omega)(2\Omega) \\ &+ (I)(6\Omega) \\ &= (18)(2) = 18 \left(-\frac{1}{3}A\right) \\ &= -6V \end{aligned}$$

$$V_t = (2\Omega) \left( 6 \cdot \left( -\frac{1}{3} i_t \right) + i_t \right) + (6\Omega) \left( -\frac{1}{3} i_t \right)$$



$$V_t = (2\Omega)(6I + i_t) + (6\Omega)I$$

$$\Rightarrow KCL \Rightarrow (6I + i_t) \cdot \frac{3\Omega}{3\Omega + 6\Omega} = I \Rightarrow I = -\frac{1}{3} i_t$$

# Conclusions



- The Three-terminal switch
- The Inverter
- The Logic Circuits and the Three-terminal switch
- BJT and MOSFET
- Switch Model (S Model) of the MOSFET
- MOSFET Inverter
- Switch -Resistor Model (SR Model) of the MOSFET
- The Switch Current Source (SCS) model of the MOSFET
- The Dependent Sources