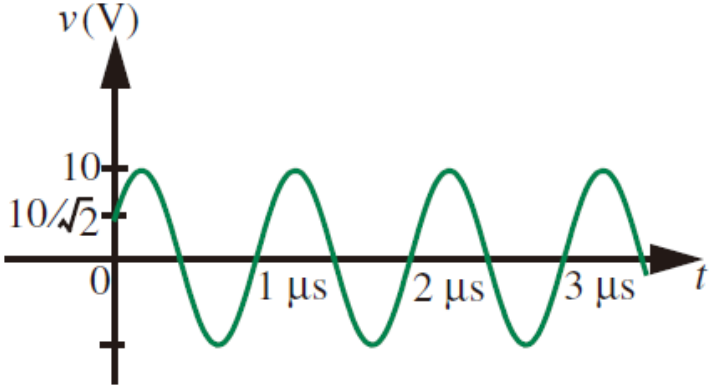
The Digital Abstraction

Chenhsin Lien and Po-Tai Cheng
CENTER FOR ADVANCED POWER TECHNOLOGIES
Dept. of Electrical Engineering
National Tsing Hua University
Hsinchu, TAIWAN

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

Signal Representation

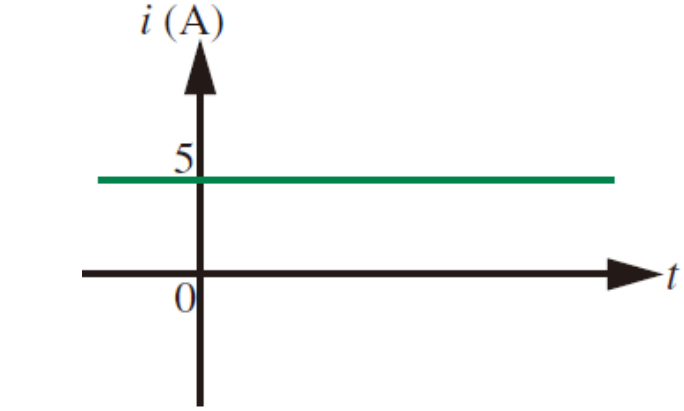
- One of the motivations for building circuits is to ***process information or energy***.
- iPod, iPad, and iPhone are examples of commonplace electronic systems for processing ***information***. Power supplies are example of electronic circuits that process ***energy***.
- Either the ***information or the energy***, is represented in the circuit by an ***electrical signal***, namely a ***current i(t)***or a ***voltage v(t)***, and ***circuit*** networks are used to process these signals.
- An analog Signal: a 1-MHz sinusoidal signal with amplitude 10 V and a phase offset of $\pi/4$

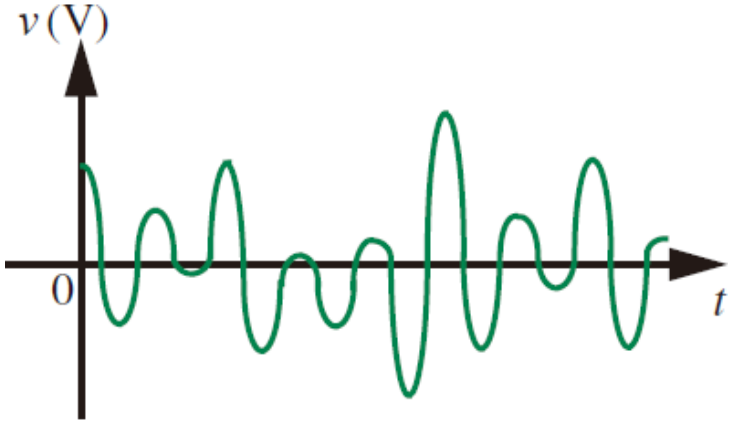


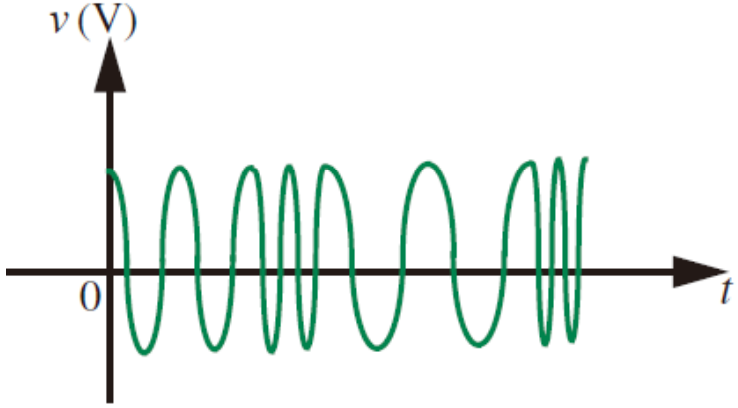
(a) $v = 10 \sin\left(2\pi \times 10^6 t + \frac{\pi}{4}\right)$

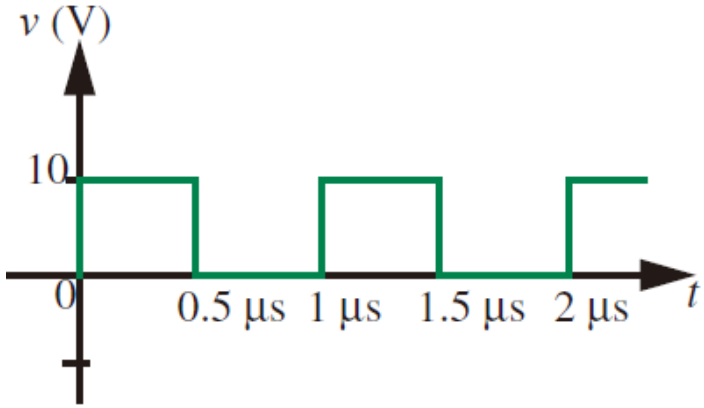
Analog Signals

- A 5-A DC signal.
- A signal carrying information in its amplitude.
- A signal carrying information in its frequency.
- A 1-MHz square wave signal with a 5-V offset



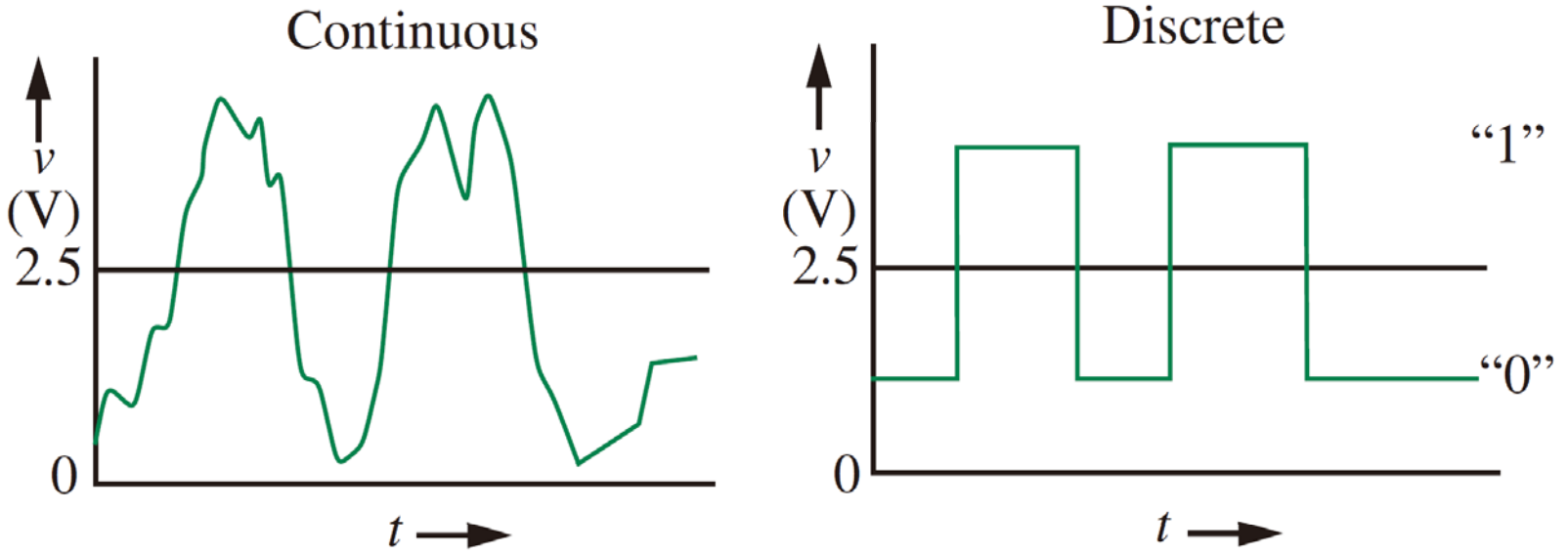






The Digital Abstraction

- Digital abstraction is ***the signal value discretization***.
- Continuous Signal

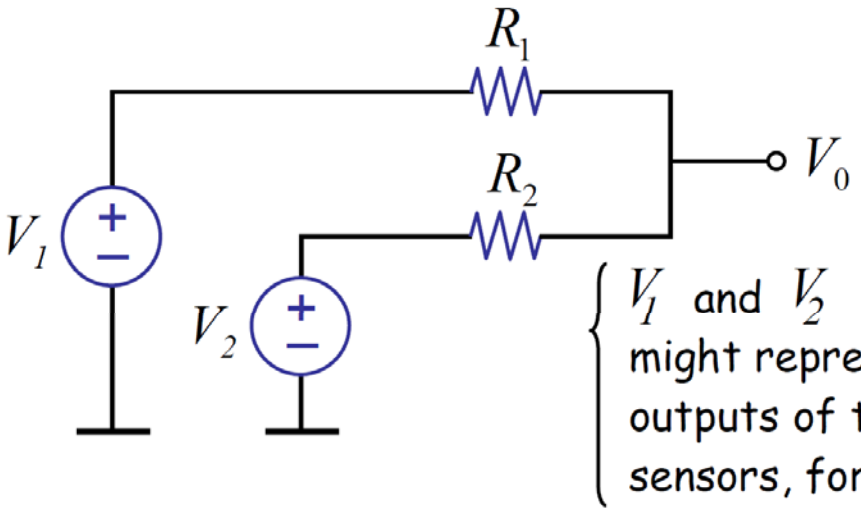


- Discrete Signal (or Digital Signal)
- Interestingly, we will see shortly that the tools learned in the previous three chapters are sufficient to analyze simple digital circuits.

Why digital Signal?

- Here is a signal averager (an analog signal processing circuit).

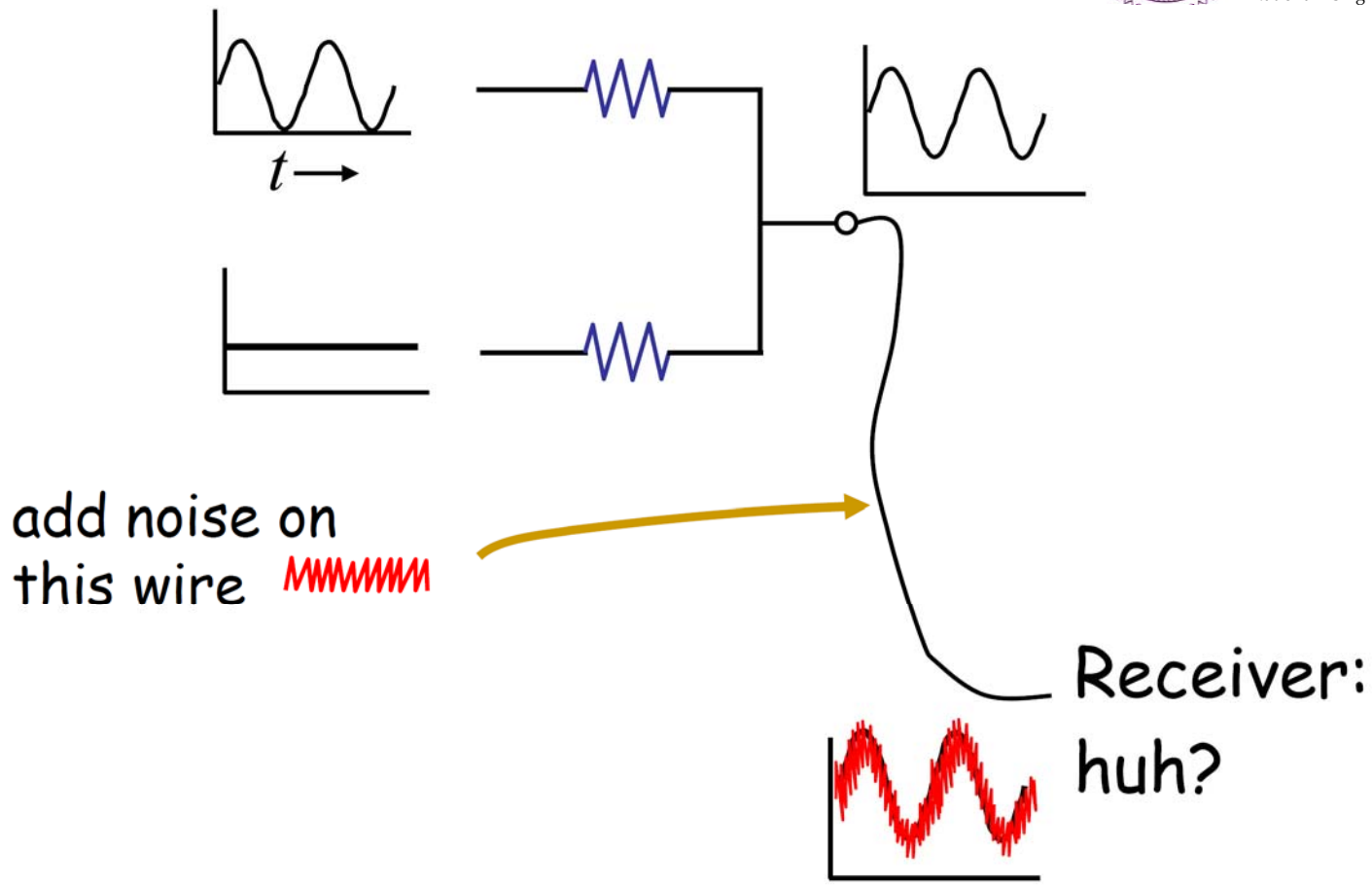
Analog signal processing



$$V_0 = \frac{R_2}{R_1 + R_2} V_1 + \frac{R_1}{R_1 + R_2} V_2$$

If $R_1 = R_2$, $V_0 = \dfrac{V_1 + V_2}{2}$ This is an ***Averager*** Circuit.

Noise Problem



Noise hampers our ability to distinguish between small differences in value, for example, between 3.1V and 3.2V.

Value Discretization

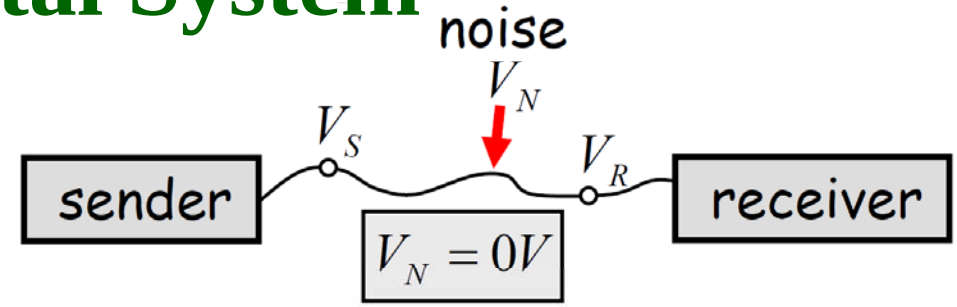
- Let's restrict values to be one of following two values.

High	***Low***
5V	0V
True	***False***
1	**0**

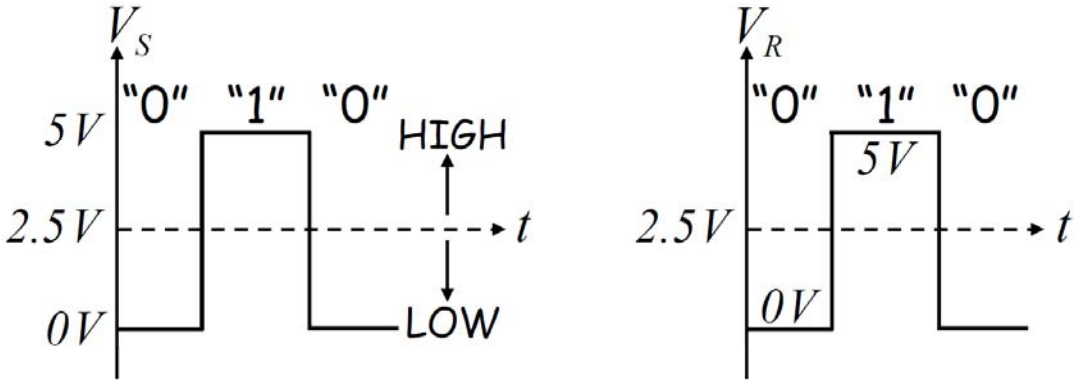
- This is just like two digits 0 and 1
- (Remember, numbers larger than 1 can be represented using multiple binary digits and coding, much like using multiple decimal digits to represent numbers greater than 9. E.g., the binary number 101 has decimal value 5.)

- ***Why is this discretization useful?***

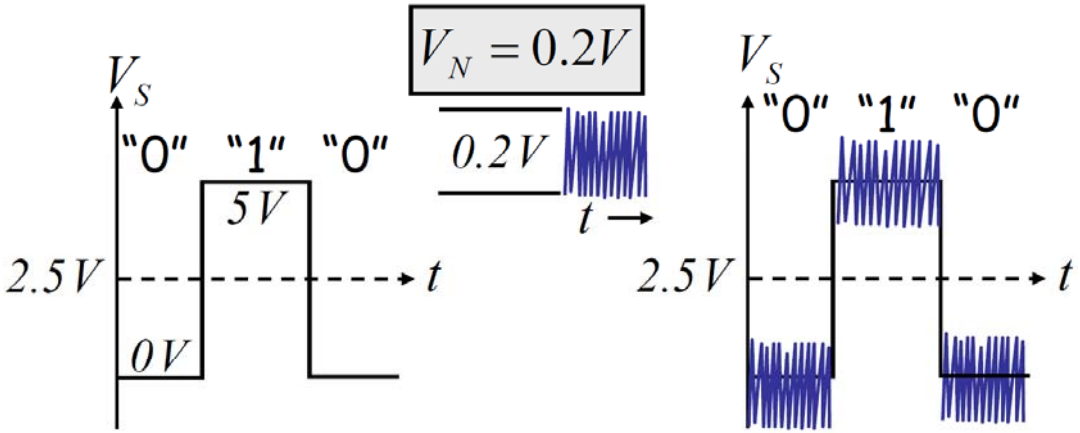
Digital System



Without noise



With noise



Digital System

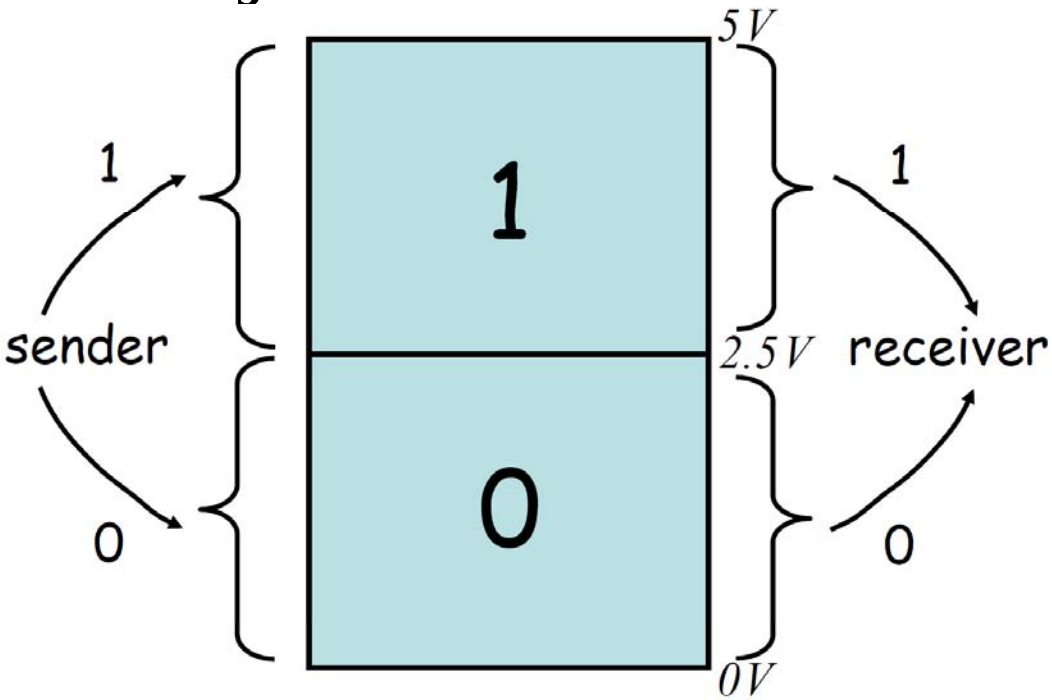
- Better noise immunity

  Lots of "noise margin "

Logic value for "1" : $2.5\ \mathrm{V} \le V \le 5\ \mathrm{V}$ ***noise margin*** 5V to 2.5V = 2.5V.

Logic value for "0" : $0\ \mathrm{V} \le V < 2.5\ \mathrm{V}$ ***noise margin*** 0V to 2.5V = 2.5V.

- 2.5V is called the ***voltage threshold***.

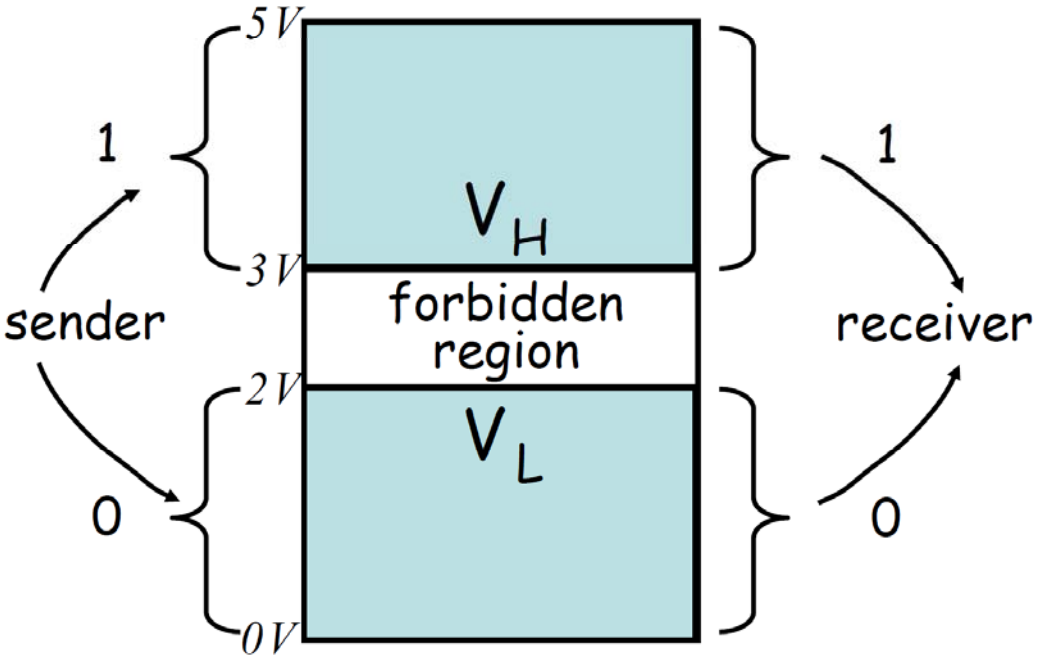


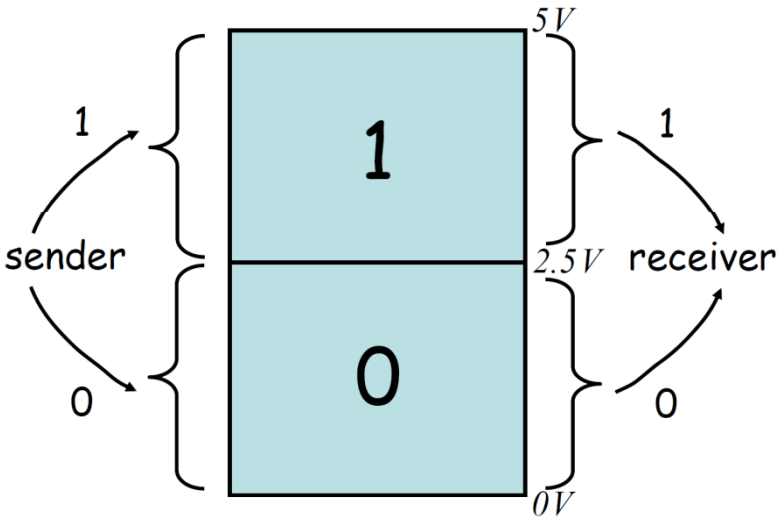
Issue with Voltage threshold 2.5V

- What if the receiver receive a 2.5 V signal? How to interpret this signal? 0 or 1?
- How about create a "forbidden region“ to overcome this problem?

logic value for "1" : $V_H \equiv 3\,\mathrm{V} \le V \le 5\,\mathrm{V}$

logic value for "0" : $0\,\mathrm{V} \le V \le 2\,\mathrm{V} \equiv V_L$



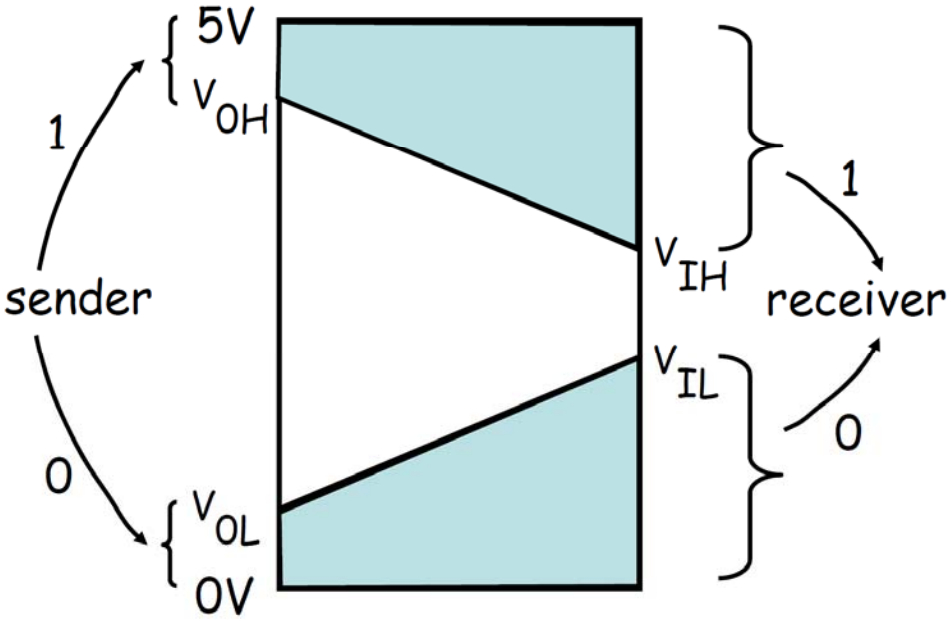


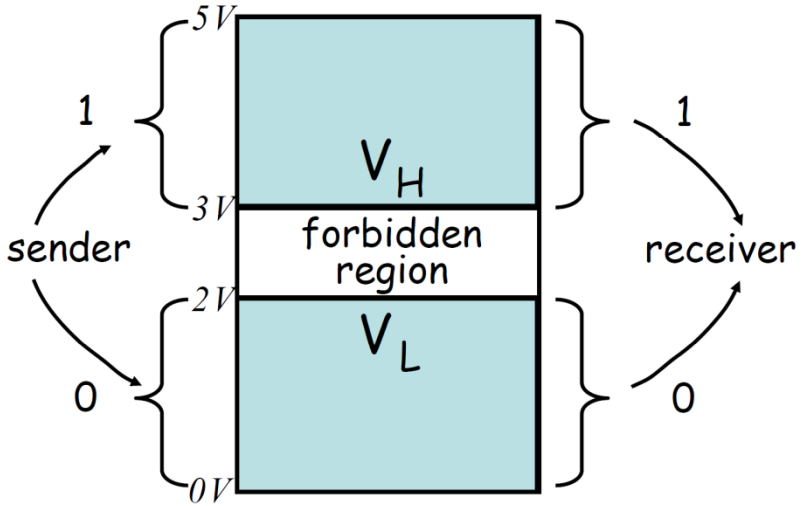
Noise Margin

- If the sender sent $V_H = 3\text{V}$ as logic "1“, then where’s the noise margin?
- How to resolve this zero noise-margin issue?
- Hold the sender to tougher standards!

"1" for sender: $V_{OH} \equiv 4\text{ V} \le V \le 5\text{ V}$ for receiver: $V_{IH} \equiv 3\text{ V} \le V \le 5\text{ V}$

"0" for sender: $0\text{ V} \le V \le 1\text{ V} \equiv V_{OL}$ for receiver: $0\text{ V} \le V \le 2\text{ V} \equiv V_{IL}$



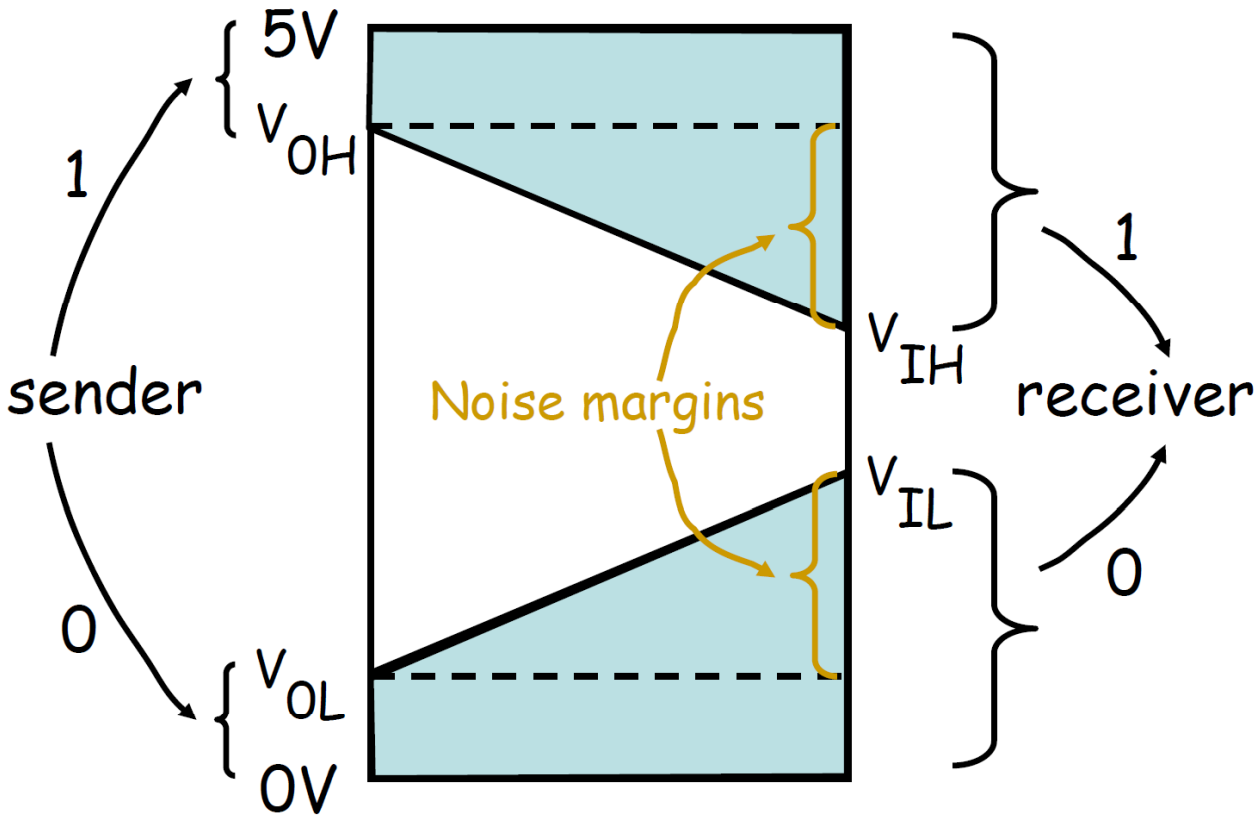


The Noise Margin

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

"1" noise margin: $\mathrm{NM}_1 = V_{OH} - V_{IH}$

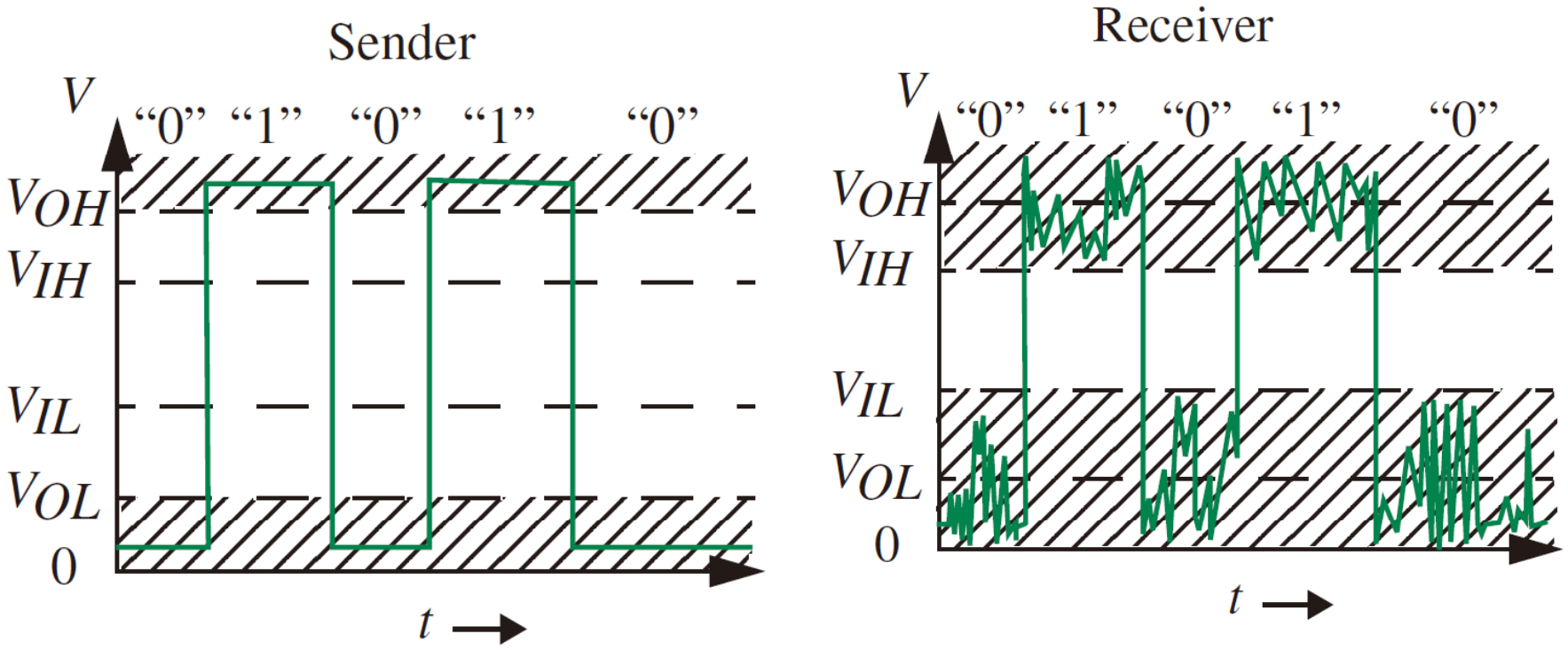
"0" noise margin: $\mathrm{NM}_0 = V_{IL} - V_{OL}$



The Static Discipline

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

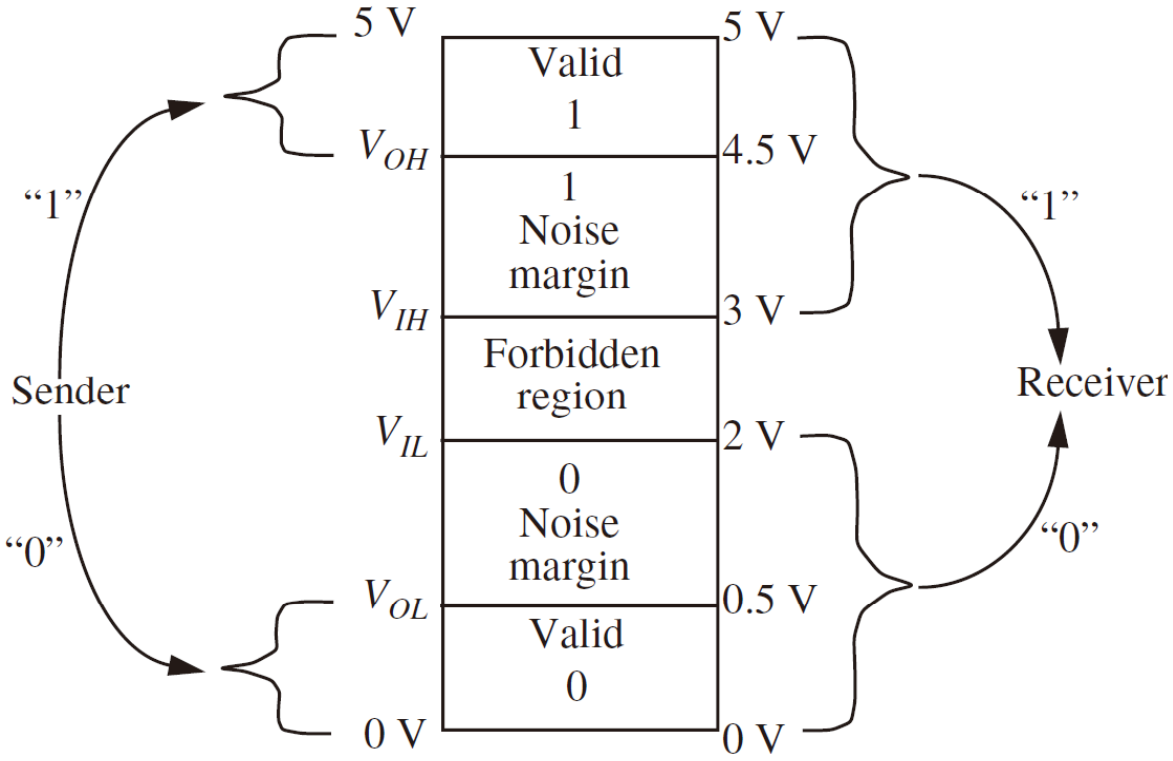
- Digital systems follow static discipline: if inputs to the digital system meet valid input thresholds, then the system guarantees its outputs will meet valid output thresholds.



The Static discipline

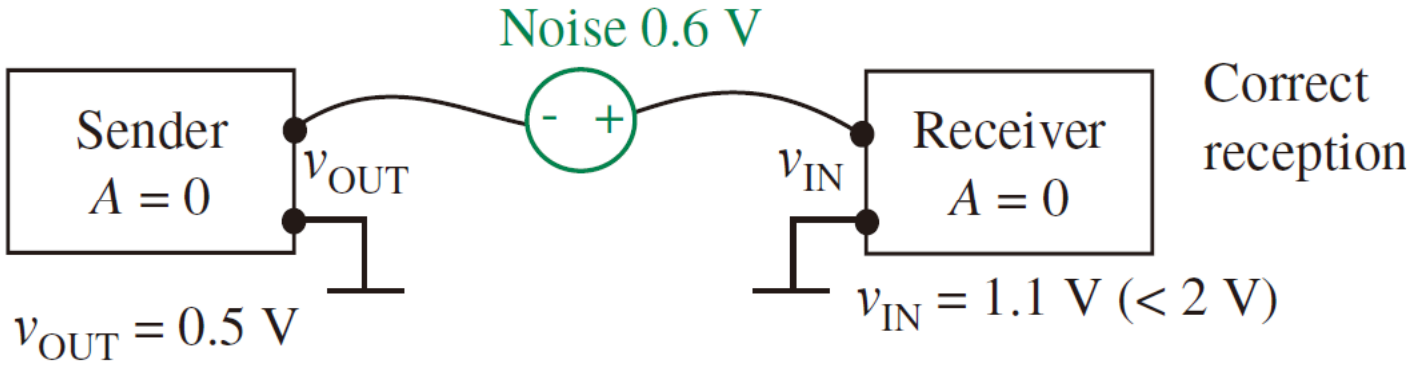
CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

- The static discipline is a specification for digital devices.
- The static discipline requires devices to interpret correctly voltages that fall within the input thresholds (V_{IL} and V_{IH}).
- As long as valid inputs are provided to the devices, the discipline also requires the devices to produce valid output voltages that satisfy the output thresholds (V_{OL} and V_{OH}).

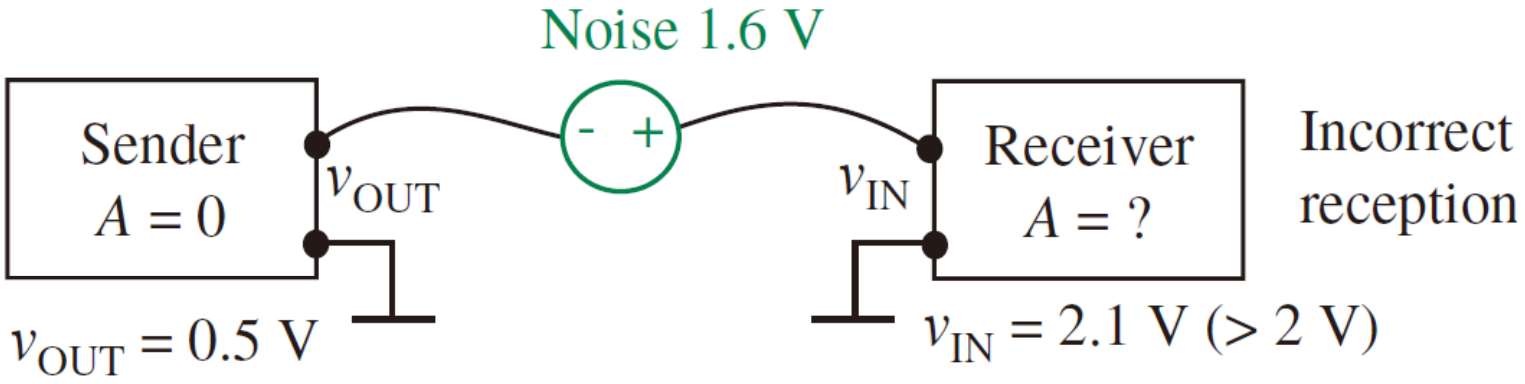


Noise Margin

- The sender sends a 0 by placing $v_{OUT} = 0.5$ V on the wire. The receiver is able to interpret the value as a 0 because the received value is within the low input voltage threshold of 2 V.

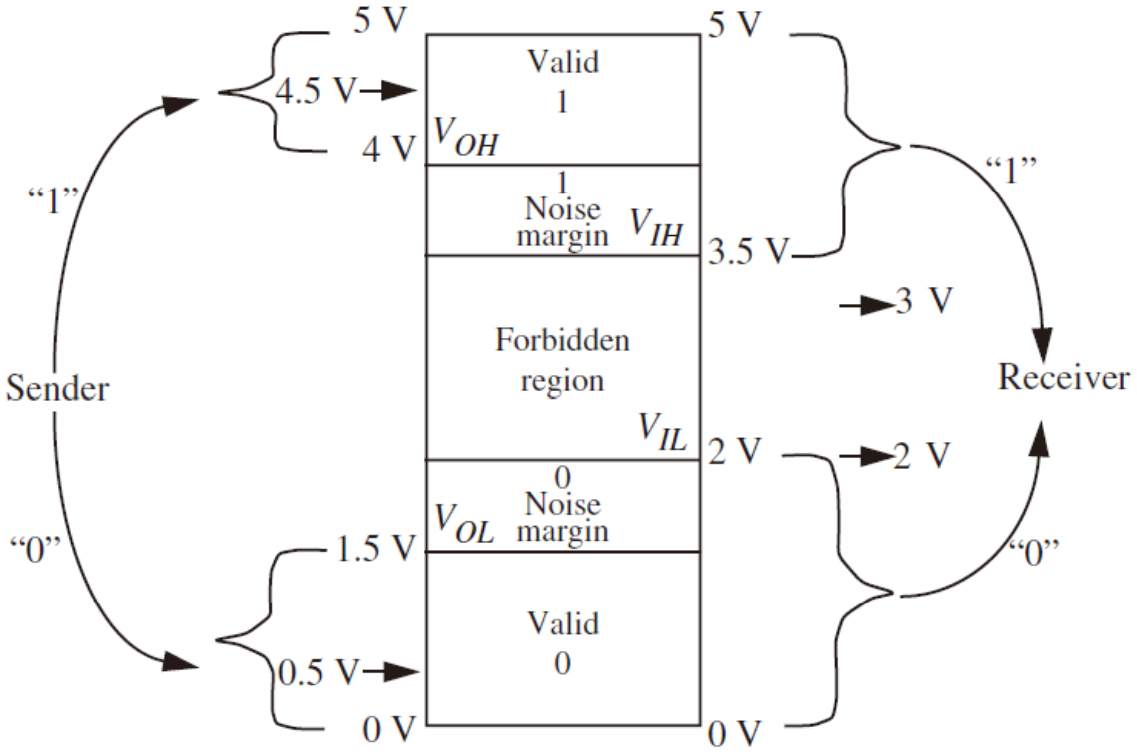


- The receiver is unable to interpret the signal correctly because the noise level of 1.6 V is higher than the noise margin of 1.5 V.



Example

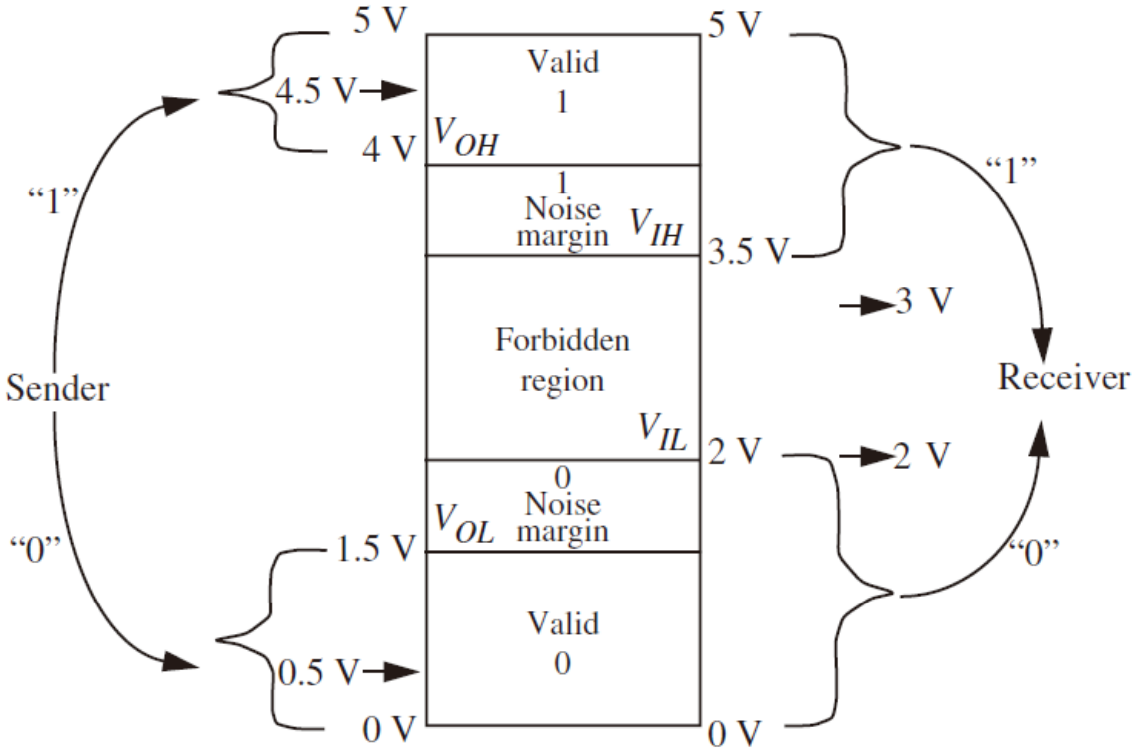
- Disco's static discipline: V_{IL} = 2 V, V_{IH} = 3.5 V, V_{OL} = 1.5 V and V_{OH} = 4 V.
- Yehaa adders can interpret all signals between 0 V and 2 V at their inputs as a logical 0, and all signals between 3 V and 5 V as a logical 1.
- For a logical 0, their adders produce a voltage level of 0.5 V at their outputs. For logical 1, their adders produce the voltage level of 4.5 V.
- Yehaa's adders satisfy Disco's static discipline



Example

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

- Disco's static discipline: V_{IL} = 2 V, V_{IH} = 3.5 V, V_{OL} = 1.5 V and V_{OH} = 4 V.
- Yikes's adders can interpret all signals between 0 V and 1.2 V at their inputs as a logical 0, and all signals between 4 V and 5 V as a logical 1.
- For a logical 0, their adders produce a voltage level of 1.7 V at their outputs. For logical 1, their adders produce the voltage level of 4.5 V.
- Yikes's adders DO NOT satisfy Disco's static discipline.



Processing digital signals

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

- Recall, we have only two values.
- Map naturally to logic: T, F.
- Can also represent numbers: 1, 0.
- An Example- Boolean Logic: AND gate
- The statement

If **X** is true and **Y** is true
Then **Z** is true else **Z** is false.

Truth table representation:

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

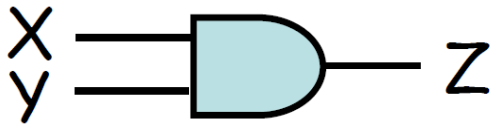
- Boolean Eq. ⇨ Z = X AND Y

Z = X • Y

Boolean equation

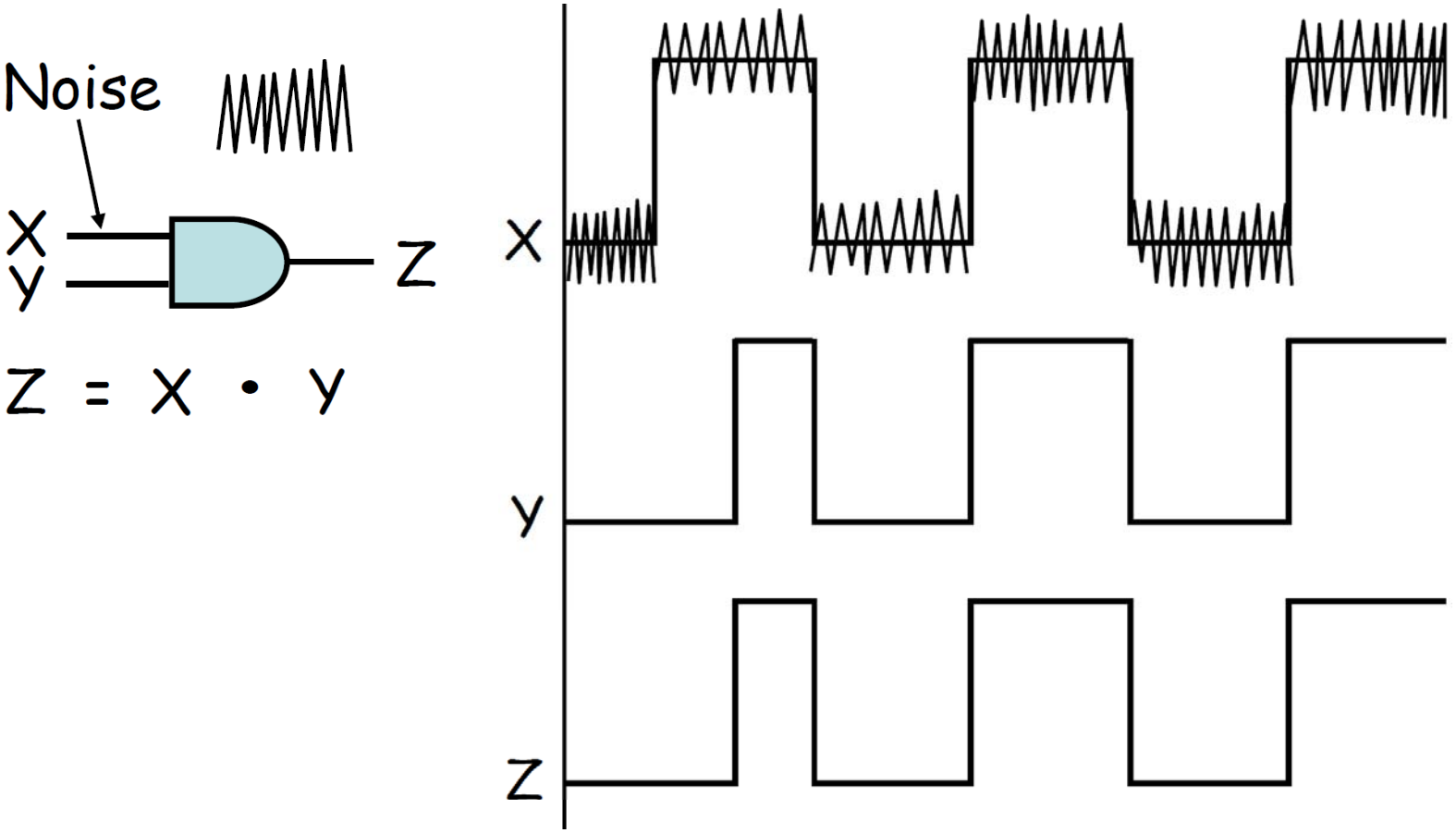
X, Y, Z are digital signals "0" , "1"

- AND Gate



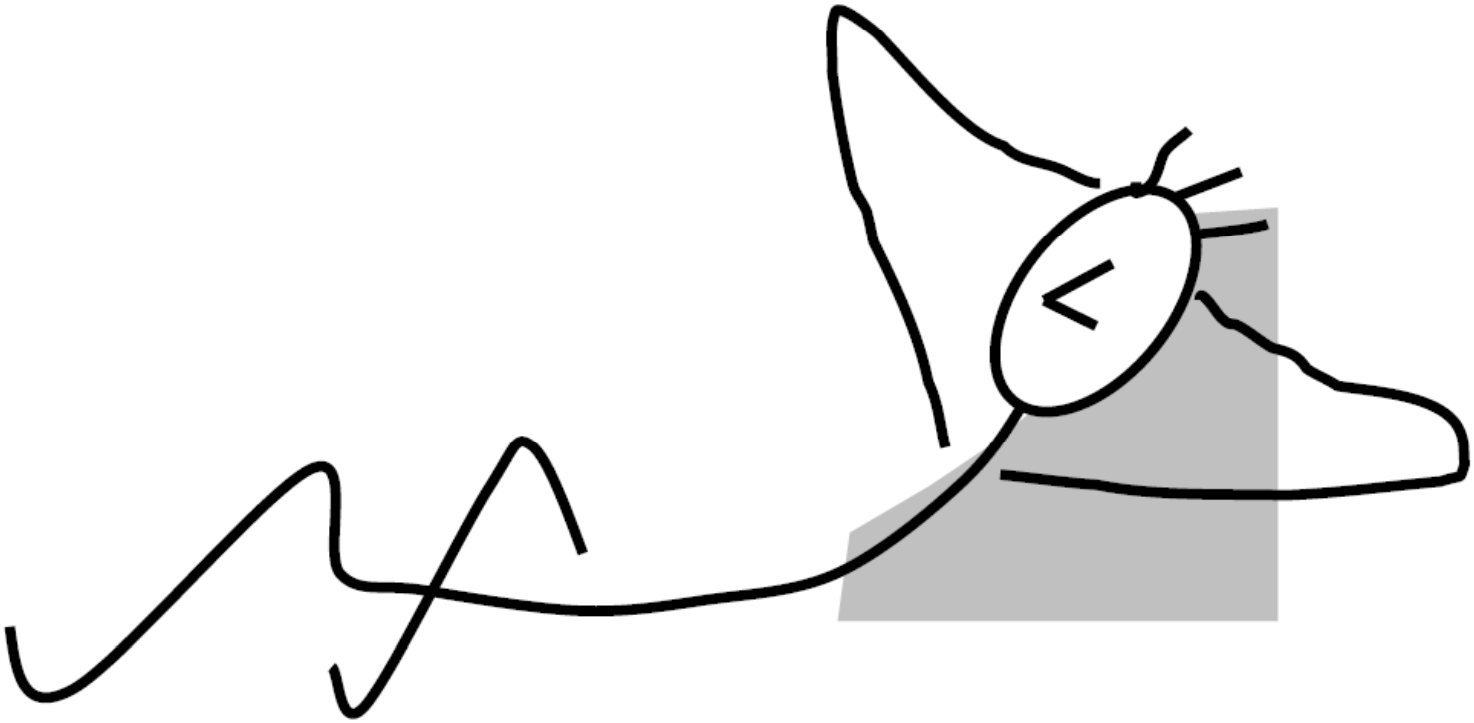
- Truth Table Representation

Noise Immunity



Combinational gate abstraction

- Adheres to static discipline.
- Outputs are a function of inputs alone.
- Digital logic designers do not have to care about what is inside a gate.



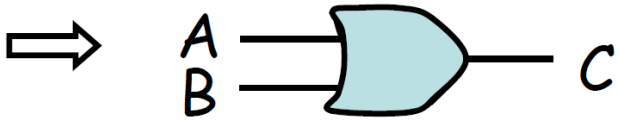
More Gates

- An OR gate.

If (**A** is true) OR (**B** is true)
then **C** is true
else **C** is false

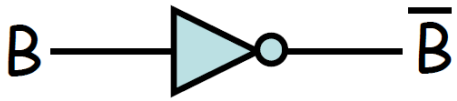
$\Rightarrow C = A + B$ Boolean equation

OR



OR gate

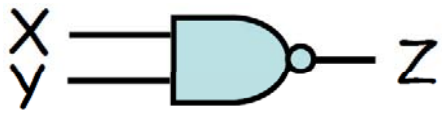
- NOT gate (or called Inverter)



Inverter

Digital Circuits

- An NAND gate.

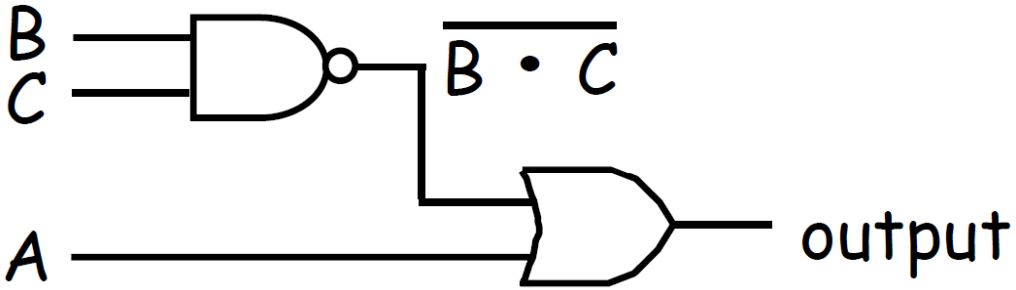


NAND

$$Z = \overline{X \cdot Y}$$

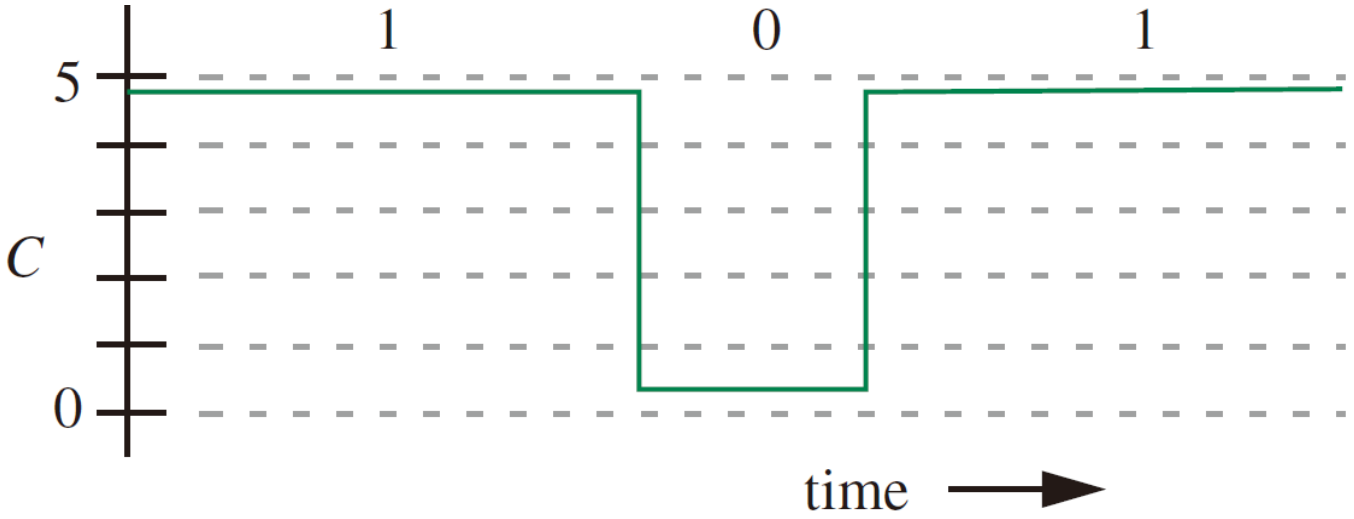
- Digital Circuits

Implement: $output = A + \overline{B \cdot C}$



What if we receive the following?

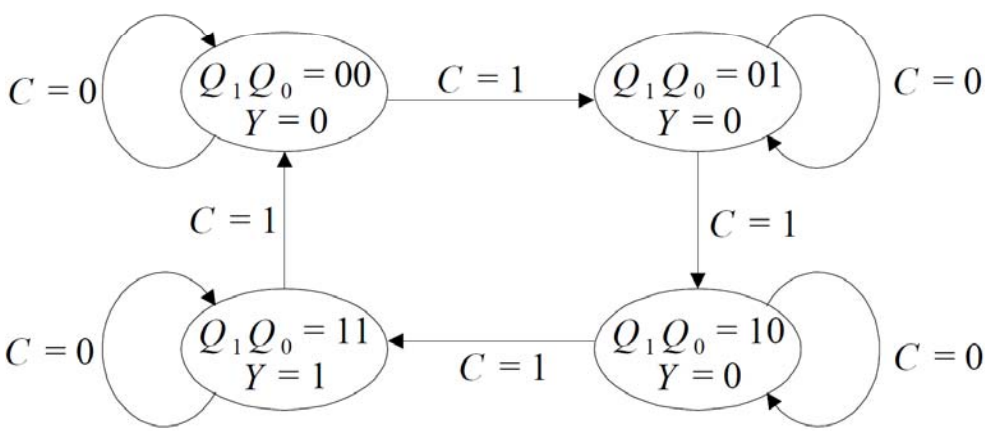
- What if we receive the following signal?

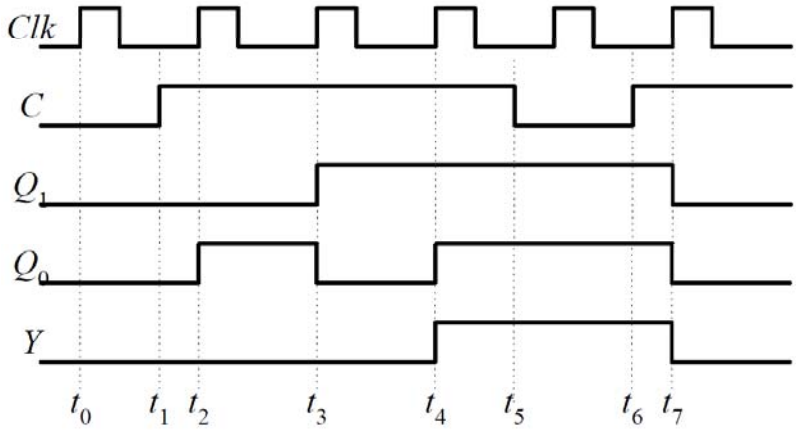


- Is C 11011?
- May be C is 111110011111. May be ……
- How to make sure we get (or interpret) the correct signal send by the sender?

Clocked Digital Systems

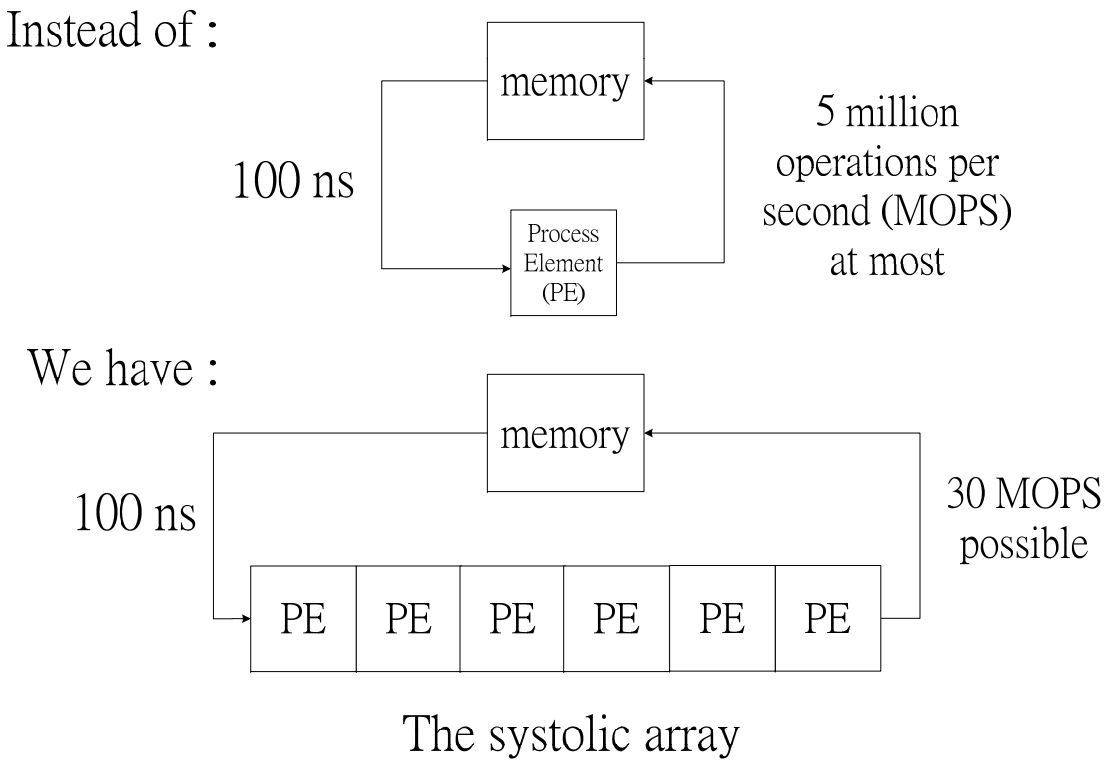
- ***Lumped circuit abstraction*** that is fundamental to electrical engineering is based on lumping or ***discretizing matter***.
- ***Digital systems*** use the digital abstraction, which is based on ***discretizing signal values***.
- ***Clocked digital systems*** are based ***on discretizing both signals and time***.





Digital Systolic Arrays

- ***Digital systolic arrays*** are based on ***discretizing signals, time and space***.
- Systolic system works like an automobile assembly line.



Conclusions

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

- Digital signal is to discretize signal value

  High and Low

  True or False

  0 and 1

- Static discipline

  V_{OH}, V_{IH}, V_{OL} and V_{IL}

- Noise Margin

  NM_1 and NM_0

- Clocked digital systems and Digital systolic arrays

My PC Hardware monitor

CAPT
Center for Advanced Power Technologies
National Tsing Hua University, TAIWAN

- Winbond W83627DHG hardware monitor
- Voltage sensor 0 1.32 Volts [0xA5] (CPU VCORE)
- Voltage sensor 1 12.04 Volts [0xD8] (+12V)
- Voltage sensor 2 3.23 Volts [0xCA] (AVCC)
- Voltage sensor 3 3.23 Volts [0xCA] (+3.3V)
- Voltage sensor 5 5.14 Volts [0xD6] (+5V)
- Note that the voltage for CPU core is much less than voltage for PC mother board. Why?