Energy and Power

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Why worry about energy?

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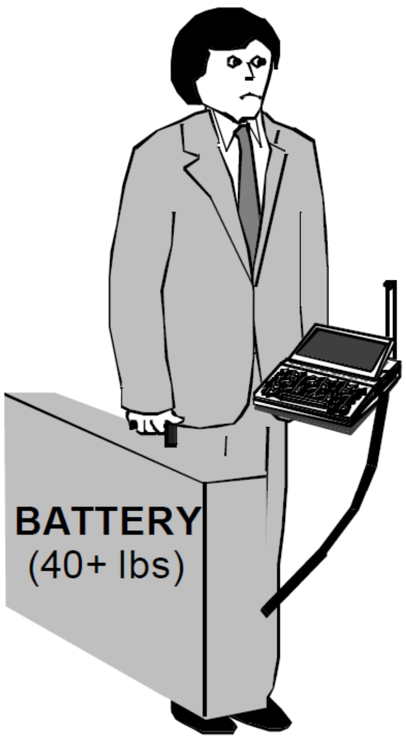
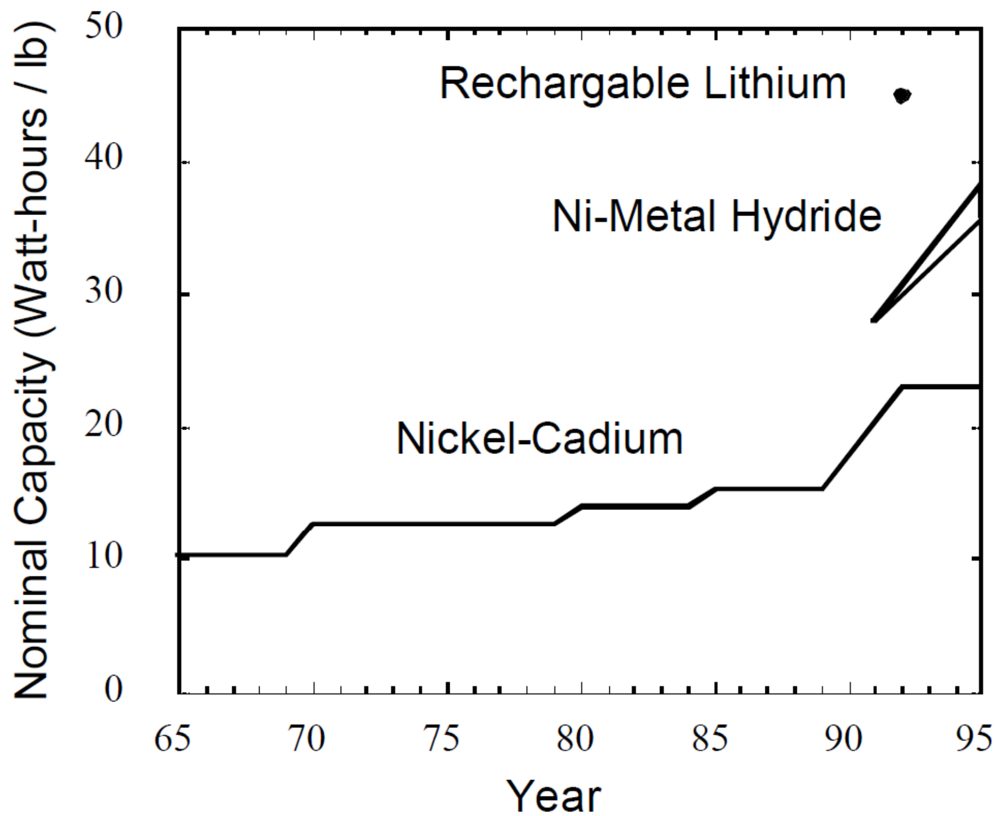
- Portability





- Want to learn about.
  - How long will the battery last? (1) in stand-by mode. (2) in active use.
  - Will the chip overheat and self-destruct?

Energy Dissipation in MOSFET Gates

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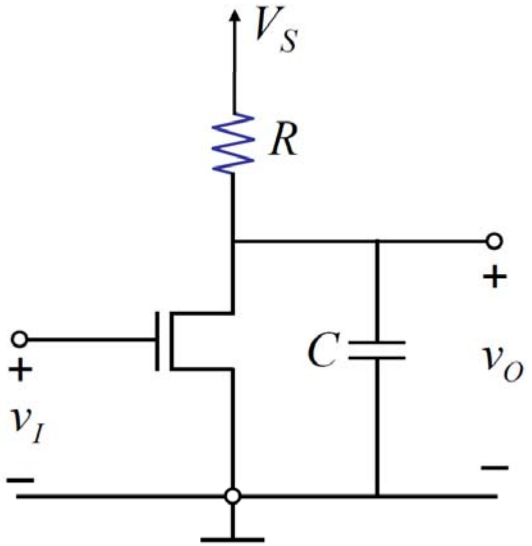
- For the logic gate below:



$$C = C_{Wire} + C_{GS}$$

- Let us determine ***standby power*** and ***active use power***.
- Let's work out a few related examples first.

Example #1

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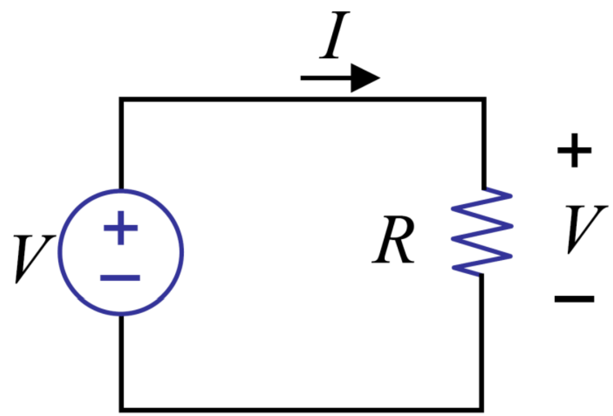
- The Circuit #1



- **Power** P**.**

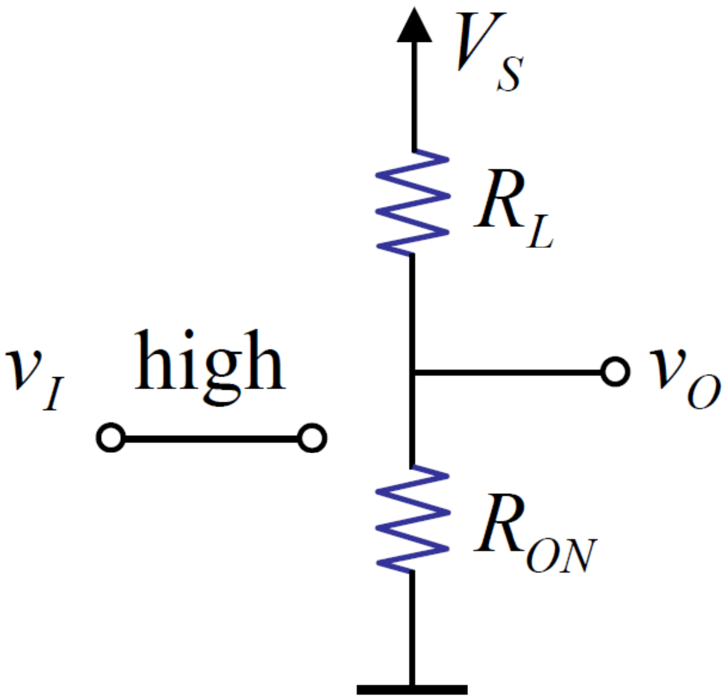
$$P = VI = \frac{V^2}{R}$$

- **Energy dissipated in time** T.

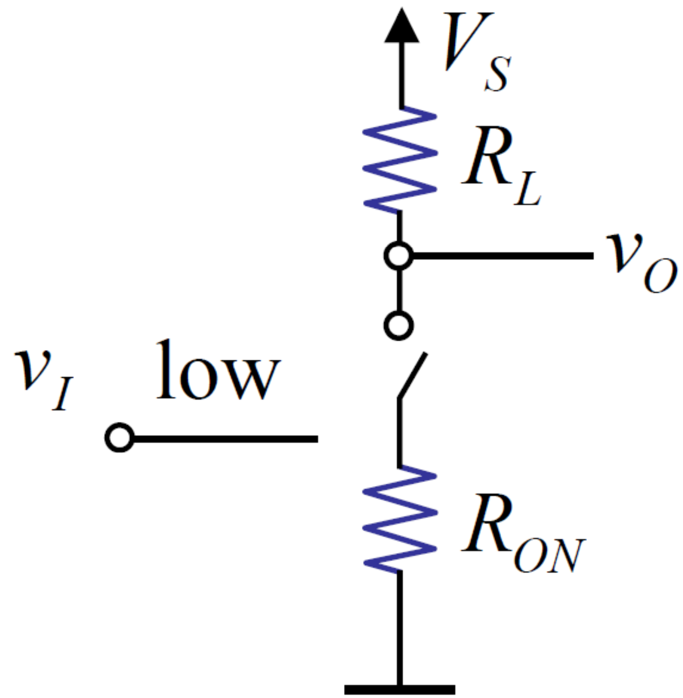
$$E = VIT = \frac{V^2}{R} T$$

Example #1

- Applying to our gate



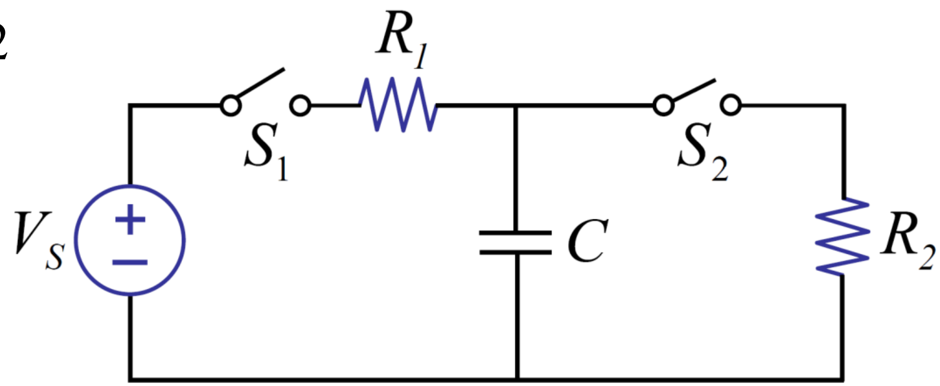
$$P = \frac{V_S^2}{R_L + R_{ON}}$$

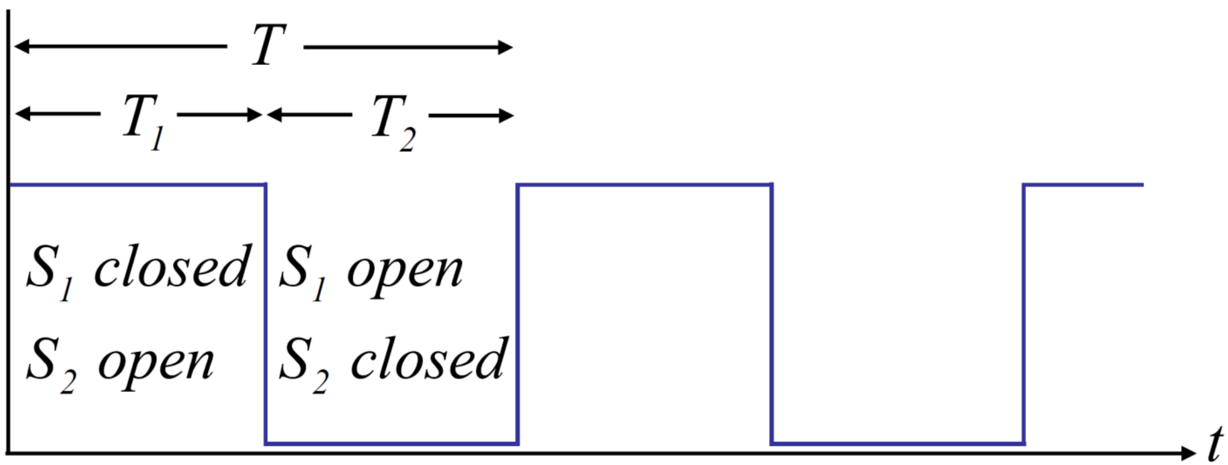


$$P = 0$$

Example #2

- The Circuit #2





- Find energy dissipated in each cycle.
- Find average power $\overline{P}$.

Example #2

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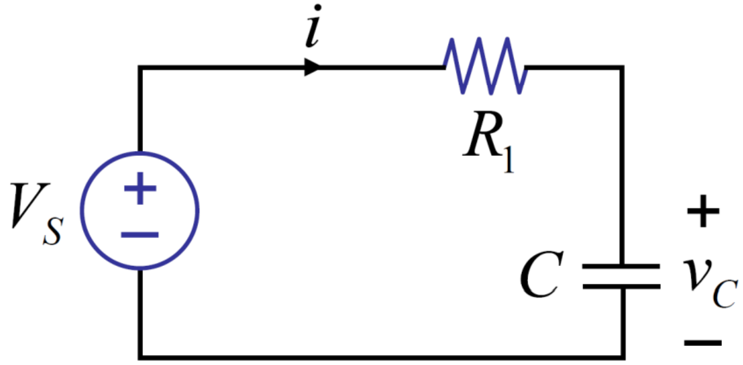
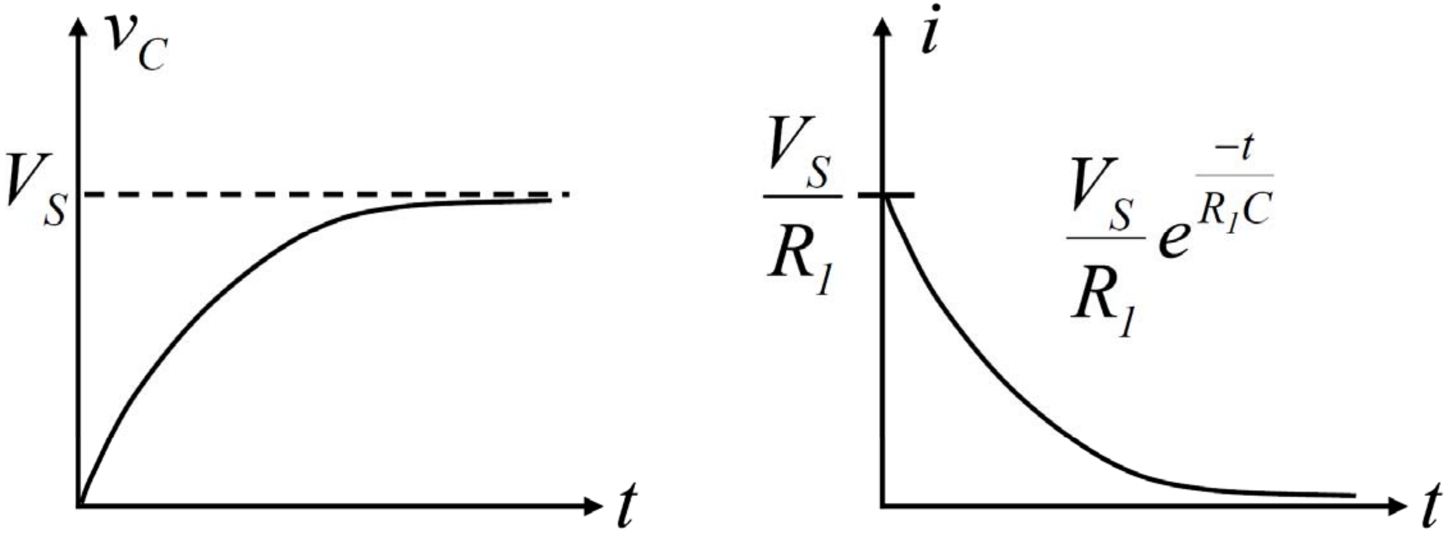
- During T_1: S_1 closed, S_2 open.



- Assume $v_C = 0$ at $t = 0$.



Total energy

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- Total energy provided by source during T_1:

$$E = \int_0^{T_1} V_S i dt = \int_0^{T_1} \frac{V_S^2}{R_1} e^{-\frac{t}{R_1 C}} dt = -\frac{V_S^2}{R_1} R_1 C e^{-\frac{t}{R_1 C}} \Big|_0^{T_1}$$

$$E = CV_S^2 \left(1 - e^{-\frac{T_1}{R_1 C}} \right)$$

$$E \approx CV_S^2$$

If $T_1 >> R_1C$, i.e. if we wait long enough

- $\frac{1}{2} CV_S^2$ stored in capacitor.
- $E_1 = CV_S^2 - \frac{1}{2} CV_S^2 = \frac{1}{2} CV_S^2$ dissipated in R_1.

Independent of R!!

Example #2

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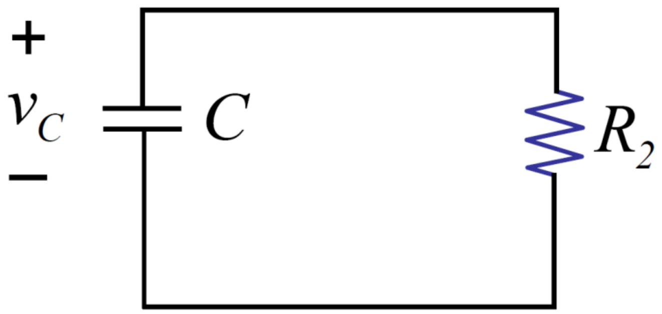
- During T_2: S_2 closed, S_1 open.



- Initially, $v_C = V_S$. (Recall $T_1 >> R_1C$).
- So, initially, energy stored in capacitor is $\frac{1}{2}CV_S^2$.
- Assume $T_2 >> R_1C$.
- Thus, capacitor discharges about fully in T_2.
- Thus, energy dissipated in R_2 during T_2 is $E_2 = \frac{1}{2}CV_S^2$.
- Both E_1 and E_2 are independent of R_1 and R_2!

Example #2

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- Putting the two periods, T_1 and T_2, together.
- We have energy dissipated in each cycle

$$E = E_1 + E_2 = \frac{1}{2} C V_S^2 + \frac{1}{2} C V_S^2$$

$$E = C V_S^2$$

- E is the energy dissipated in charging and discharging capacitor C. Assumes C charges and discharges fully.
- The average power is :

$$\overline{P} = \frac{E}{T} = \frac{C V_S^2}{T} = C V_S^2 f$$

- Where $f = \frac{1}{T}$ is the frequency.

Back to our inverter

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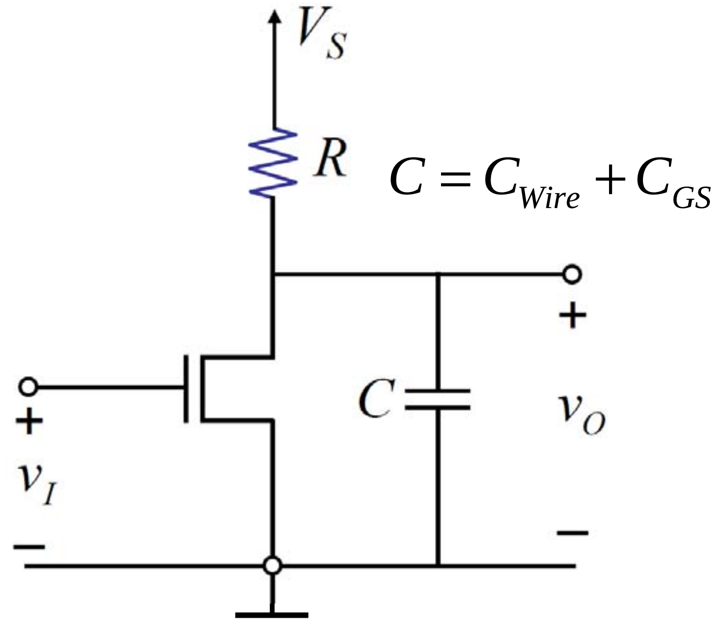
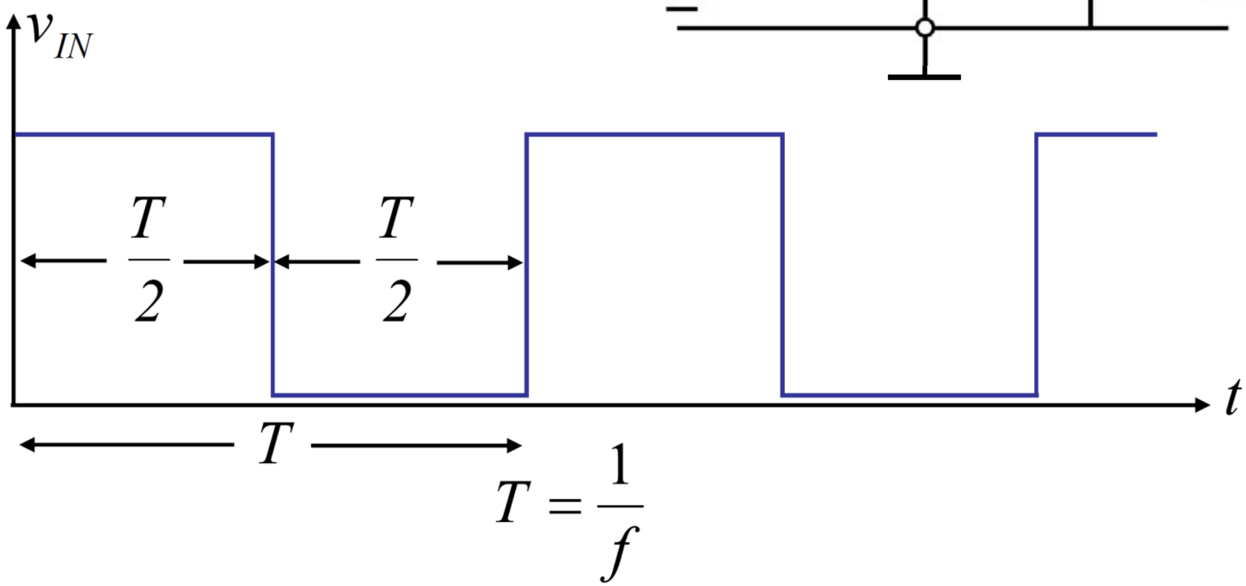


- What is $\overline{P}$ for the following input?



Equivalent Circuit

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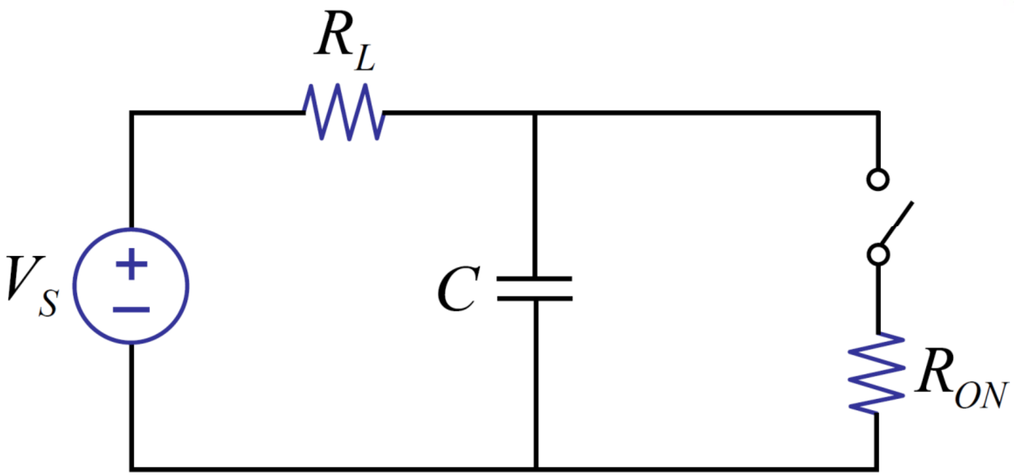
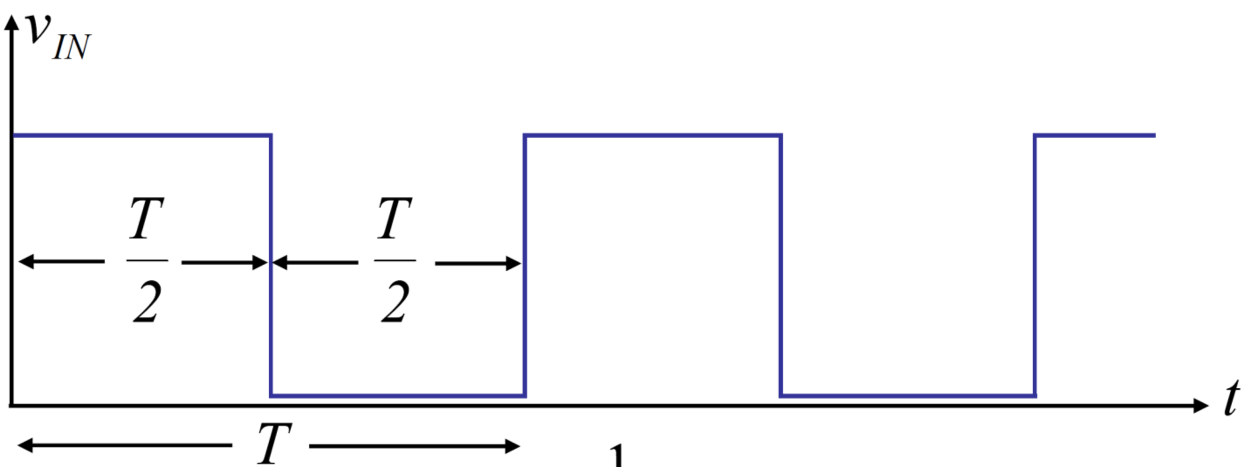


- What is $\overline{P}$ for the following input?



$$T = \frac{1}{f}$$

S Closed

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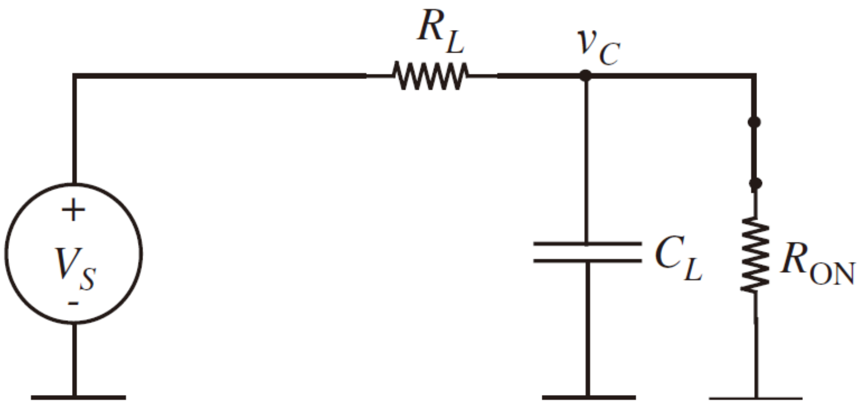


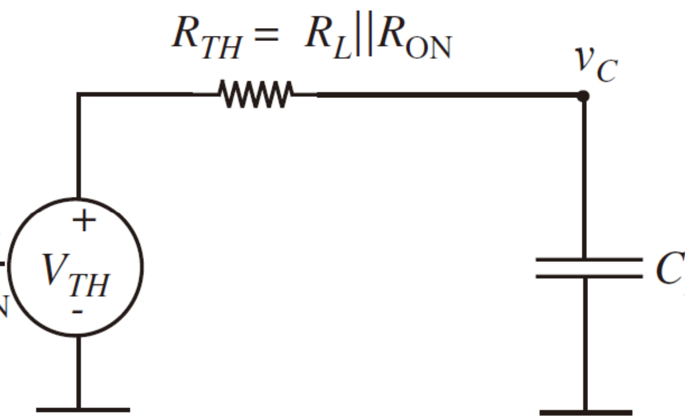
$$p(t) = \frac{(V_S - v_c(t))^2}{R_L} + \frac{v_c^2(t)}{R_{on}}$$

$$w_1 = \int_0^{T_1} p(t)dt$$

$$w_1 = \frac{V_S^2}{R_L + R_{ON}} T_1 + CV_S^2 \frac{R_L^2}{2(R_L + R_{ON})^2}$$

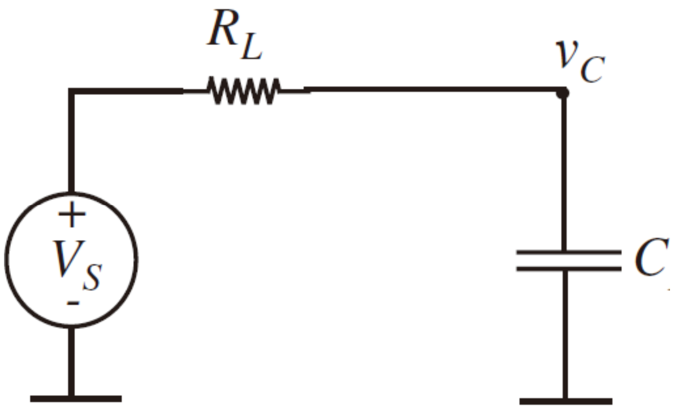
- Thévenin equivalent circuit

$$V_{TH} = \frac{V_S R_{ON}}{R_L + R_{ON}}$$



$$v_c = V_{TH} + (V_s - V_{TH})e^{-\frac{t}{R_{TH}C}}$$

S Opened



- Energy dissipated in R_L.

$$v_c = V_{TH} + (V_s - V_{TH})(1 - e^{-\frac{t}{R_L C}})$$

$$w_2 = CV_S^2 \frac{R_L^2}{2(R_L + R_{ON})^2}$$

$$p(t) = \frac{(V_S - v_c(t))^2}{R_L}$$

What is $\overline{P}$ for gate?

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- $\overline{P}$ for gate is:

$$\overline{P} = \frac{w_1 + w_2}{T} = \frac{V_S^2}{2(R_L + R_{ON})} + CV_S^2 f \frac{R_L^2}{(R_L + R_{ON})^2}$$

- When $R_L >> R_{ON}$

$$\overline{P} = \frac{V_S^2}{2R_L} + CV_S^2 f$$

- The first term $\overline{P}_{Statics} = \frac{V_S^2}{2R_L}$ is called static power dissipation (independent of *f*). The MOSFET is ON half of the time.
- The second term $\overline{P}_{Dynamic} = CV_S^2 f$ is called dynamic power dissipation (proportional to *f* and *C*).

Standby Mode

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- When $R_L >> R_{ON}$

$$\overline{P} = \frac{V_S^2}{2R_L} + CV_S^2 f$$

- In standby mode, $f \rightarrow 0$ and dynamic power is 0.

- Thus, $\overline{P}_{\text{Standby}} = \frac{V_S^2}{2R_L}$

- From above, in standby mode, half the gates in a chip can be assumed as be on.

- Standby power and active power

$$\overline{P} = \overline{P}_{\text{Standby}} + \overline{P}_{\text{Active}} = \frac{V_S^2}{2R_L} + CV_S^2 f$$

Some numbers

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- A chip with 10^6 gates clocking at 100 MHz.
- Assume C = 1 fF, R_L = 10 kΩ, and V_S = 5 V.

$$\overline{P} = 10^6 \times \left(\frac{V_S^2}{2R_L} + CV_S^2 f \right)$$

$$\overline{P} = 10^6 \times \left(\frac{5^2}{2\times10^4} + 10^{-15} \times 5^2 \times 10^8 \right)$$

$$\overline{P} = 10^6 \times (1.25\,\text{mW} + 2.5\,\mu\text{W})$$

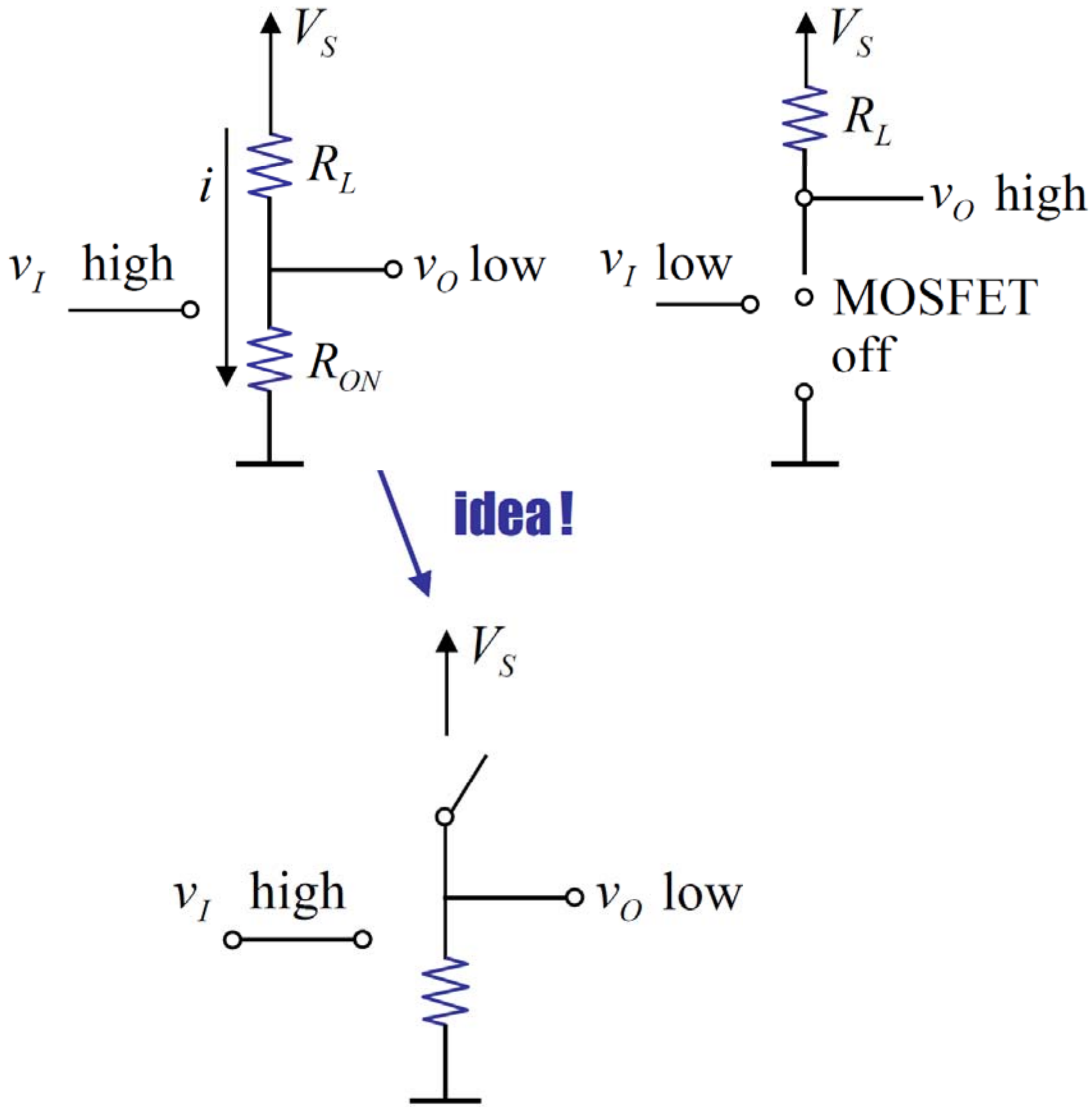
$$\overline{P} = \overline{P}_{\text{Standby}} + \overline{P}_{\text{Active}} = 1.25\,\text{KW} + 2.5\,\text{W}$$

Not bad, Reducing V_S From 5 to 1V Become 150 mW

Problem

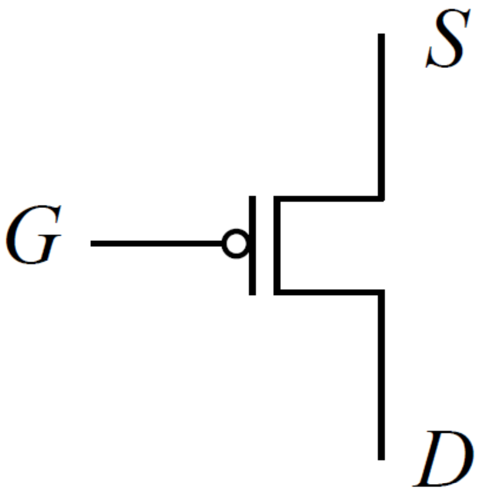
How to get rid of static power?

- Intuition:



PMOS

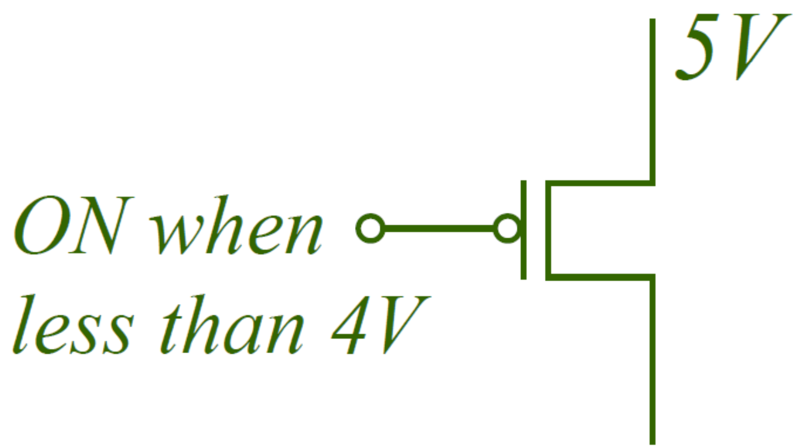
- P-channel MOSFET (PMOS)



on when $v_{GS} \leq V_{TP}$

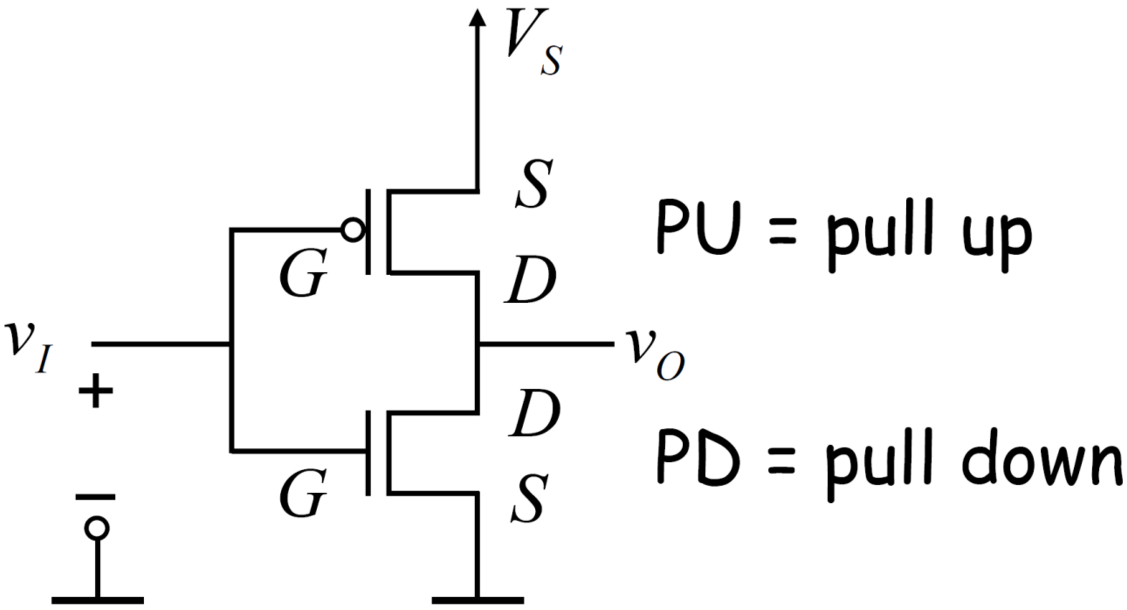
off when $v_{GS} > V_{TP}$

e.g. $V_{TP} = -1V$

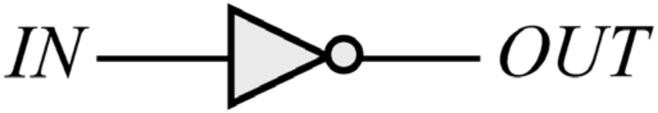


CMOS

- Consider this circuit:

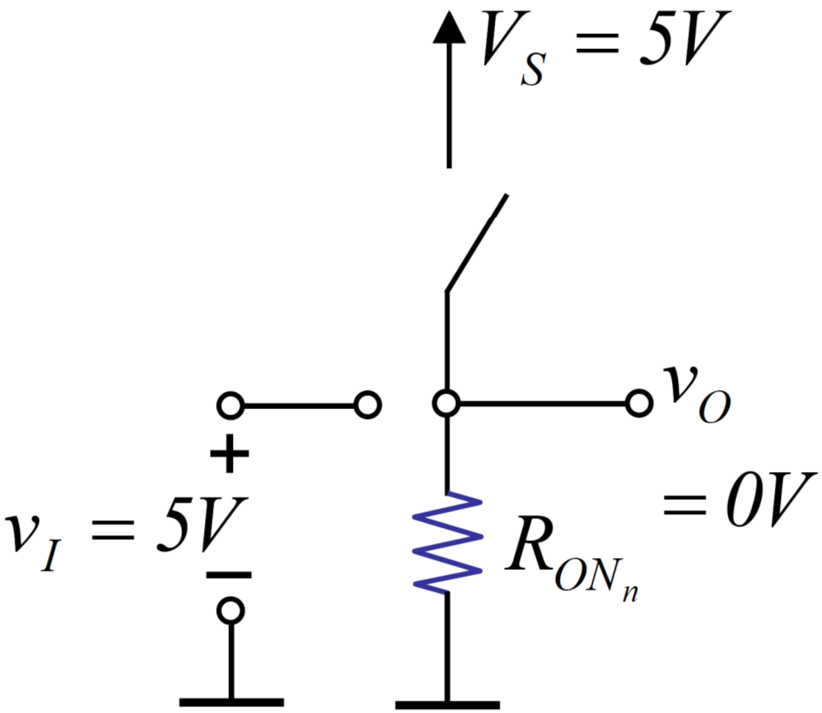


- Works like an inverter!

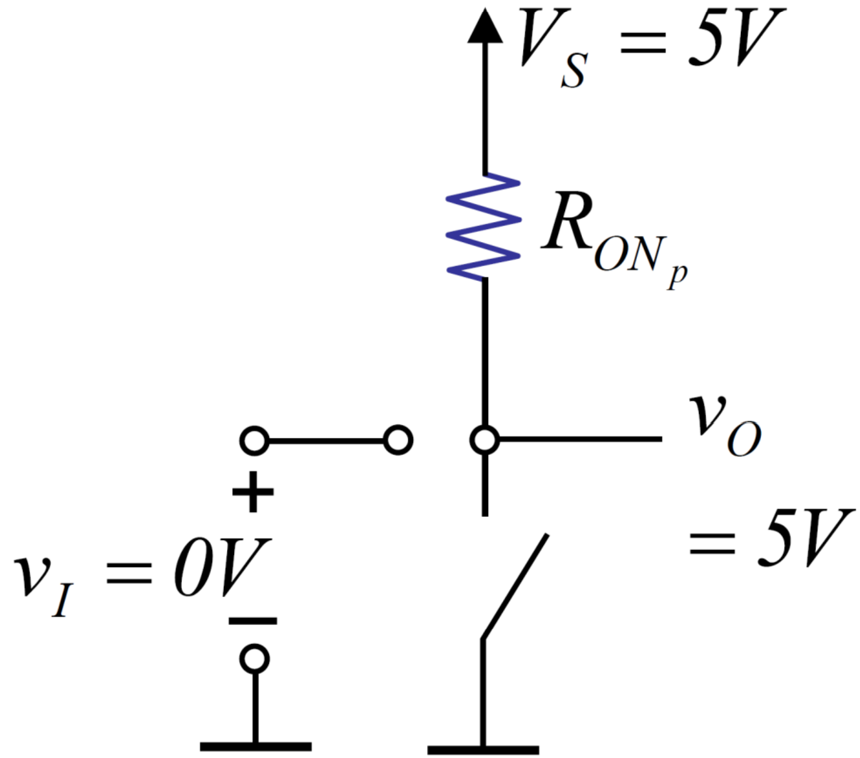


CMOS

- Called "CMOS logic" or Complementary MOS logic. (Our previous logic was called "NMOS")



$v_I = 5V$ (input high)



$v_I = 0V$ (input low)

Power of CMOS Logic

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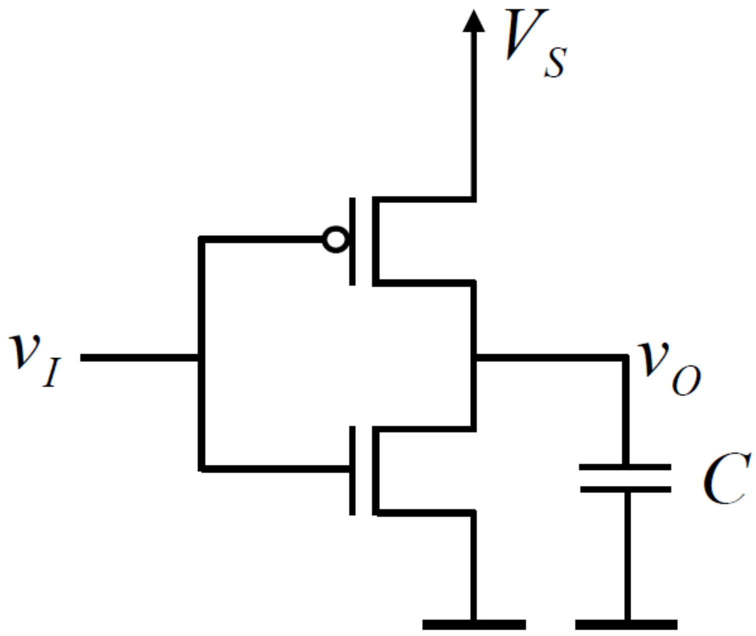
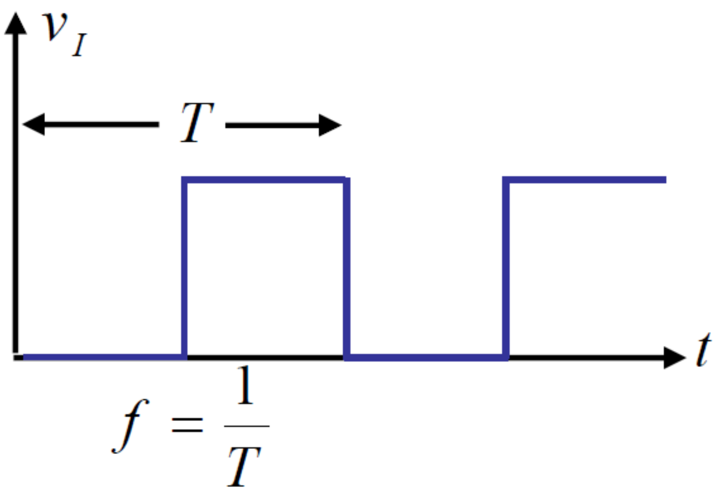
- Since there are no path from VS to GND! Thus, there are no static power dissipation!
- Let's compute $\overline{P}_{\text{Active}}$ or $\overline{P}_{\text{Dynamic}}$.





Power of CMOS Logic

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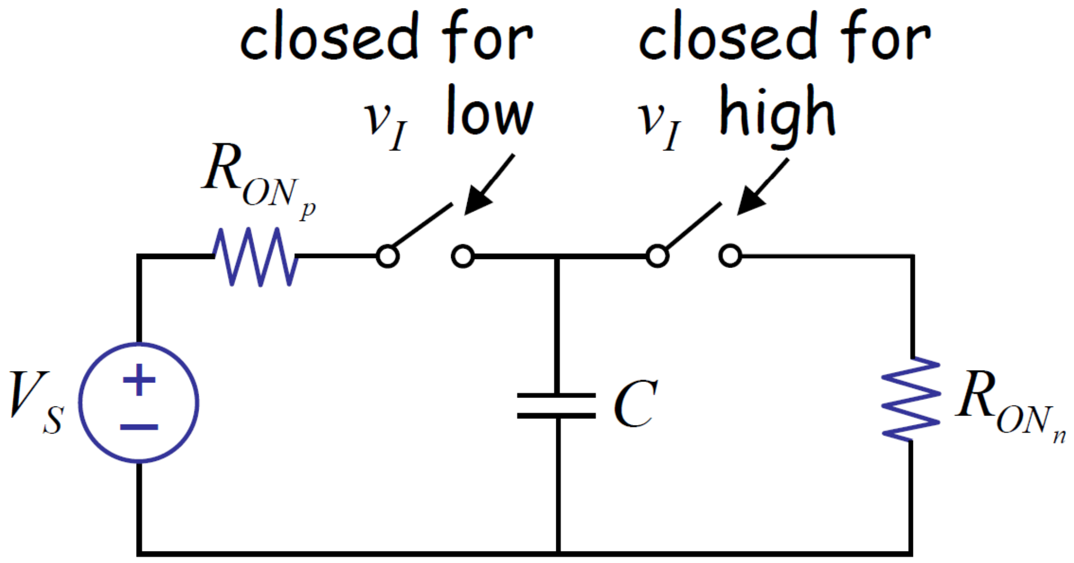

- From previous discussion, we have $\overline{P}_{\text{Dynamic}}$ as:

$$\overline{P}_{\text{Dynamic}} = CV_S^2 f$$

For our previous example

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- A chip with 10^6 gates clocking at 100 MHz.
- Assume C = 1 fF, R_L = 10 kΩ, and V_S = 5 V.

Gates	*f*	*P*
10^6	100 MHz	2.5 W
2×10^6	300 MHz	15 W
2×10^6	600 MHz	30 W
8×10^6	1.2 GHz	240 W
25×10^6	3 GHz	1875 W

How to reduce power?

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- Reduce V_S.
- Turn off circuit when not in use (Sleep mode).
- Change V_S depending on need.
- Use multicore to reduce *f* without sacrificing speed of the circuits.

Power Trends in Intel's Microprocessors