電路學(EE2210)第四次隨堂考

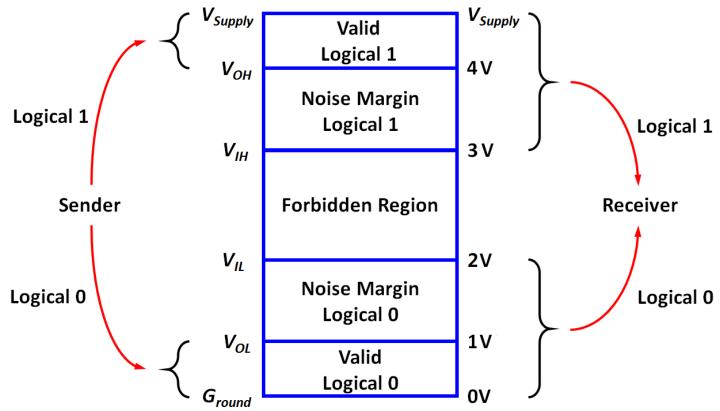
Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{IL} = 2 \text{ V}$, $V_{OL} = 1 \text{ V}$, $V_{IH} = 3 \text{ V}$, and $V_{OH} = 4 \text{ V}$.

| (a) What is the highest voltage that must be interpreted by a receiver as a logical 0? | (12.5%) |
|--|---------|
| (b) What is the lowest voltage that must be interpreted by a receiver as a logical 1? | (12.5%) |
| (c) What is the highest voltage that can be output by an inverter for a logical 0 output? | (12.5%) |
| (d) What is the lowest voltage that can be output by an inverter for a logical 1 output? | (12.5%) |
| (e) What range of voltages will be treated as invalid under this discipline? | (12.5%) |
| (f) What are its noise margins (NM_0, NM_1) ? | (25%) |
| (g) Will this logic gate family drive the input of another logic gate family characterized by the | |
| voltage thresholds: $V_{IL} = 1.5 \text{ V}$, $V_{OL} = 0.5 \text{ V}$, $V_{IH} = 3.5 \text{ V}$, and $V_{OH} = 4.4 \text{ V}$ correctly? | (12.5%) |
| | |

Solutions:

(a) & (b)

The valid voltage ranges for logical input signal can be found from the following figure under this static discipline.



Therefore

(a) the highest voltage that must be interpreted by a receiver as a logical 0 is $V_{IL} = 2V$, and (b)the lowest voltage that must be interpreted by a receiver as a logical 1 is $V_{IH} = 3V$.

(c) & (d)

The valid voltage ranges for logical output signal can be found from the figure of last page under this static discipline.

Therefore,

(b) the highest voltage that can be a logical 0 output is $V_{OL} = 1$ V, and

(c) the lowest voltage that can be a logical 1 output is $V_{OH} = 4$ V.

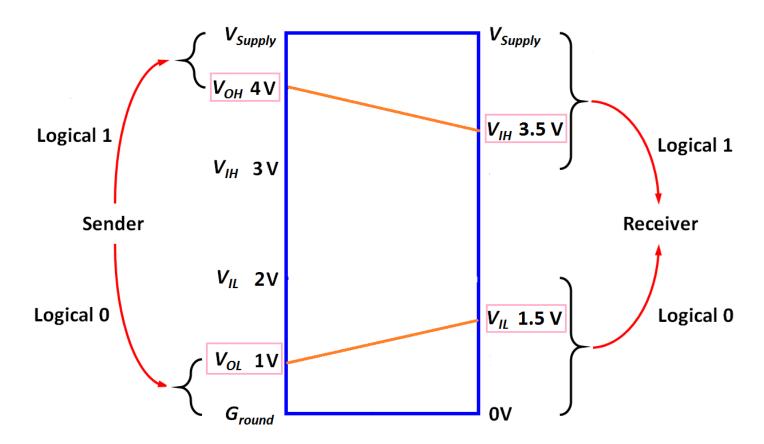
(e)

The range of voltages 2V < v < 3V will be treated as invalid under this discipline.

(f)

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NM_0 = V_{IL} - V_{OL} = 1VNM_1 = V_{OH} - V_{IH} = 1V
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(g)



Ans: Yes, because all valid outputs of the this family of logic gates are valid inputs for the other gate family as shown above.

