電路學(EE2210)第四次隨堂考

Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{IL} = 1.5 \text{ V}$, $V_{OL} = 0.5 \text{ V}$, $V_{IH} = 3.5 \text{ V}$, and $V_{OH} = 4.4 \text{ V}$.

(a) What is the highest voltage that can be output by an inverter for a logical 0 output?	(14%)
(b) What is the lowest voltage that can be output by an inverter for a logical 1 output?	(14%)
(c) What is the highest voltage that must be interpreted by a receiver as a logical 0?	(14%)
(d) What is the lowest voltage that must be interpreted by a receiver as a logical 1?	(14%)
(e) What range of voltages will be treated as invalid under this discipline?	(14%)
(f) What are its noise margins (NM ₀ , NM ₁)?	(28%)

Solutions:

(a) & (b)

The valid voltage ranges for logical output signal can be found from the following figure under this static discipline.



Therefore,

the highest voltage that can be a logical 0 output is $V_{OL} = 0.5$ V, and the lowest voltage that can be a logical 1 output is $V_{OH} = 4.4$ V.

(c) & (d)

The valid voltage ranges for logical input signal can be found from the following figure under this static discipline.



Therefore,

the highest voltage that must be interpreted by a receiver as a logical 0 is $V_{IL} = 1.5$ V, and the lowest voltage that must be interpreted by a receiver as a logical 1 is $V_{IH} = 3.5$ V.

(e)

The range of voltages 1.5V < v < 3.5V will be treated as invalid under this discipline.

(f)

$$\begin{split} \mathbf{N}\mathbf{M}_0 &= V_{IL} - V_{OL} = 1\mathbf{V}\\ \mathbf{N}\mathbf{M}_1 &= V_{OH} - V_{IH} = \mathbf{0.9V} \end{split}$$

(a) $V_{OL} = 0.5 \text{ V}$	_, (b) <u>V_{OH} = 4.4 V</u>	, (c) <u>V_{IL} = 1.5 V</u>	, (d) <u>V_{IH} = 3.5 V</u>	,
(e) $1.5V < v < 3.5V$, (f) $NM_0 = V_I$	$L - V_{OL} = 1V$, $NM_1 = V_{OH} - V_{IH} = 0.9V$	·

