Part I. Design and characterization of single-stage amplifier

A. Design of a common-source amplifier

5.6 ~ 10 V/V

1. According to Fig. 2, please build a common-source amplifier on your breadboard with the power supply voltage and the gate voltage fixed at 5.0 V (the power supply has a fixed 5-V output) and 2.0 V, respectively (make sure that COM1 and COM2 are connected together). You should use the NMOS transistor without body effect (node 6-7-8). Please add bias resistors of 5 kΩ and a coupling capacitor of 0.1 μF to apply the input signal to the gate. With simple hand calculation, please determine the load resistor necessary to achieve a small-signal gain in the range between **15 dB to 20 dB** at the mid-band. Please explain your design process.

Set $A_V = 7.5$

$\Rightarrow g_m(R_D \parallel r_o) = 7.5$

$\Rightarrow R_D = 11927\,\Omega$

$(v_o/v_i)_{calc.} = -7.5$

$I = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_{th})^2 = 2.296 \times 10^{-4}$

$\lambda = 0.00758$ $W/L = 7$

$V_{th} = 1.2846$

$K_n = 2.99 \times 10^{-4}$

$r_o = \frac{1}{\lambda I} = 574629\,\Omega$

$g_m = \frac{I}{V_{GS}} = 0.00064$

Based on your design, measure the drain current I_D (DC), the voltage across drain and source (DC), and the mid-band small-signal gain v_o/v_i. Compare the measured data with your analysis in the space provided below.

Measured values: V_{GS} = 1.996 V; I_D = 233.6μ A; V_{DS} = 2.407 V; v_o/v_i = -7.69

Comment:

As $A_V = g_m \times (R_D \parallel r_o)$, $g_m = \frac{2I}{V_{od}}$, measured current is larger and V_{GS} < 2V ⇒ V_{od} is lower than expected. Therefore, measured V_o/V_i is higher.

2. Perform HSPICE simulation based on the transistor parameters extracted in Lab 6. Compare the measured results (DC values and gain) with HSPICE simulation, and comment on what you observe.

Comment:

V_{GS} = 2V, I_D = 234.24u, V_{DS} = 2.2359V, V_o/V_i = -7.58

As simulation is usually very precise, which will not affected by individual elements (ex: resistors, voltage source's finite impedance...) So it's more close to hand calculation result.

3. Based on your design, measure the output swing under a few different input signal levels (v_i) and record these in the data sheet provided below. What is the maximum linear output swing of your design?

v_i (V_{pp})	v_o (V_{pp})
104m	800 mV
200m	1.3 V
456m	2.88 V
648m	3.6 V

Maximum output swing (in terms of linear amplification): $v_{o,\text{peak-to-peak}}$ = 3.6 V

4. Plot the load line of your design together with the simulated I_D-V_{DS} curves obtained from Lab 6. Is your design optimized for maximum output swing? Please explain.
If not, adjust the gate voltage to achieve the maximum output swing under the same load resistor. Also, measure the drain current I_D, the voltage across drain and source, and the mid-band small-signal gain v_o/v_i under the optimized V_{GS}. How does the gain change? Give a brief comment.

Measured values: $V_{GS(optimal)}$ = 1.9962 V; I_D = 243.7μ A; V_{DS} = 2.2752 V; v_o/v_i = 5.632

Comment:

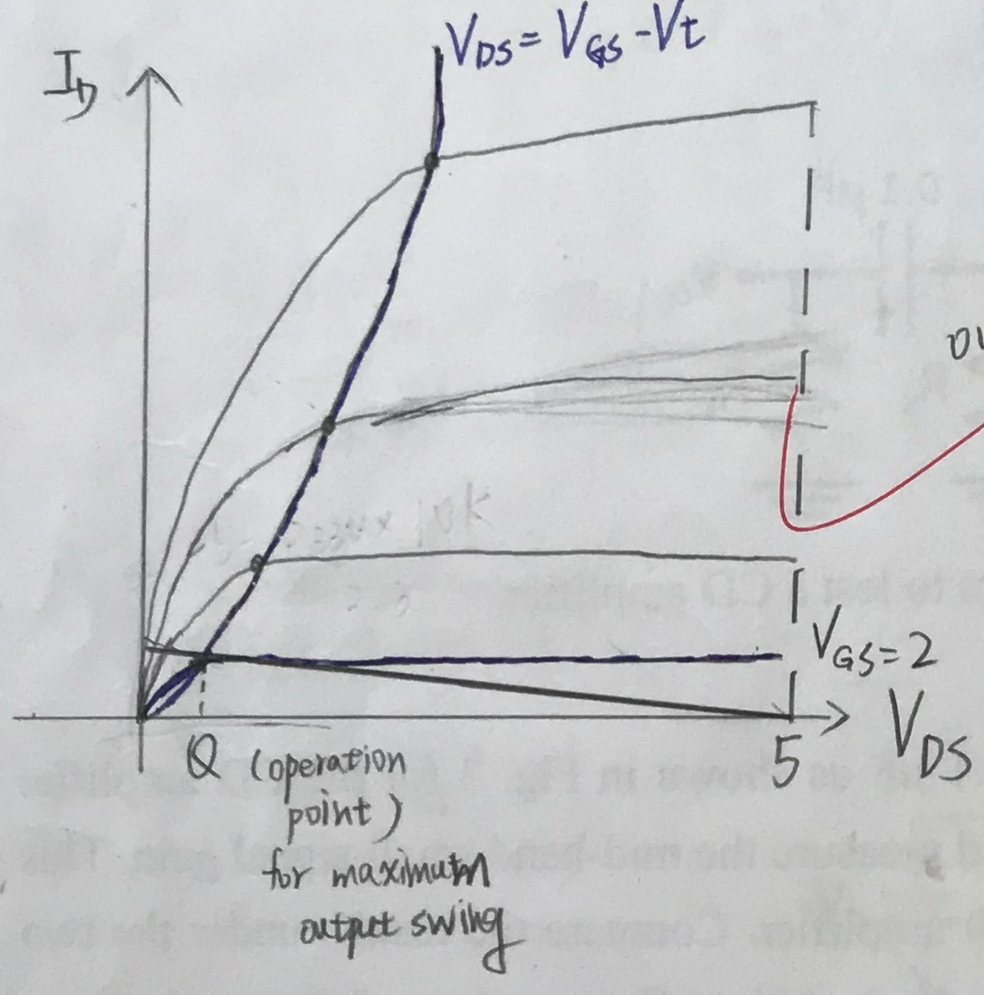
$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2 = \frac{V_{DD} - V_{DS}}{R_D} = \frac{V_{DD} - (V_{GS} - V_{th})}{R_D}$

$\Rightarrow \frac{1}{2} \times 299\mu \times 3 \times (V_{GS} - 1.28)^2 = \frac{5 - (V_{GS} - 1.28)}{11.8k}$

$\Rightarrow V_{GS} = 2.16$ (operation point)

So, we increase V_{GS} to 2.16V to maxmize output swing. But at the same time, gain decreased from -7.69 to -5.632!

Vi = 696mV
Vo = 3.92V



5. Add a source degeneration resistor of 1 kΩ in the CS amplifier. Adjust the gate voltage to achieve the same drain current as in Step 1. Measure the mid-band small-signal gain and maximum linear output swing. How does the gain compare to your hand calculation?

$(v_o/v_i)_{measured}$ = -1.66 ; $(v_o/v_i)_{calc.}$ = -2 ; maximum output swing = 1.84 V

Comment:

$V_G = 4.19$
$V_S = 0.598$
$g_m = \frac{2I_D}{V_{GS} - V_{th}} = 2.0196 \times 10^{-4}$

$A_v = \frac{g_m R_D}{1 + g_m R_S} = 2$

measured value is less calculated value. I think it's because I ignore channel length modulation (r_o) when hand calculating!

B. Design of a common-drain amplifier (source follower)

1. Design the common-drain amplifier with the transistor of nodes 6-7-8 to achieve a small-signal gain larger than 0.8 by selecting R_S, where R_S is connected to the source of the transistor directly (please refer to Fig. 3, but do not connect R_L and 0.1 μF for now). Set V_{DD}= 5.0 V and V_G= 3.0 V. Please explain your design process.

Calculation: $(v_o/v_i)_{calc.}$ = 0.82

$\lambda = 0.005356$, $V_{th} = 1.2816$, $\frac{W}{L} = 3$

$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_{th})^2$

$\Rightarrow 2230\, I_D = (3 - V_S - 1.28)^2$

$\Rightarrow 2230\, I_D = (1.72 - I_D R_S)^2$ - ①

$\Rightarrow I_D = \frac{(1.72 - I_D R_S)^2}{2230}$

$A_V = \frac{g_m (R_S // r_o)}{1 + g_m (R_S // r_o)} \geq 0.8$

$\Rightarrow g_m (R_S // r_o) \geq 4$

$\Rightarrow \frac{2I_D}{V_{od}} \times \frac{R_S \times \frac{1}{\lambda I_D}}{R_S + \frac{1}{\lambda I_D}} \geq 4$

$\Rightarrow \frac{2(1.72 - I_D R_S)}{2230} \times \frac{I_D R_S \times \frac{1}{\lambda I_D}}{I_D R_S + \frac{1}{\lambda}} \geq 4$

$\therefore 8920 (I_D R_S) + 2488604 - 2854400 \geq 0$

$\Rightarrow I_D R_S > 1.14$

$\because \lambda \neq 0 \quad I_D \geq 1.5 \times 10^{-4}$

$\Rightarrow R_S \geq 5700$ (assume $I_D = 0.2$ mA)

$\therefore$ 取 R_S = 16 kΩ

Measure the DC drain current I_D, the voltage across drain and source, and the mid-band small-signal gain v_o/v_i.

$\Rightarrow \frac{V_o}{V_i} = 0.82$

Measured values: I_D = 150u A; V_{DS} = 4.1 V; v_o/v_i = 0.83

$V_S = 1.17$ V

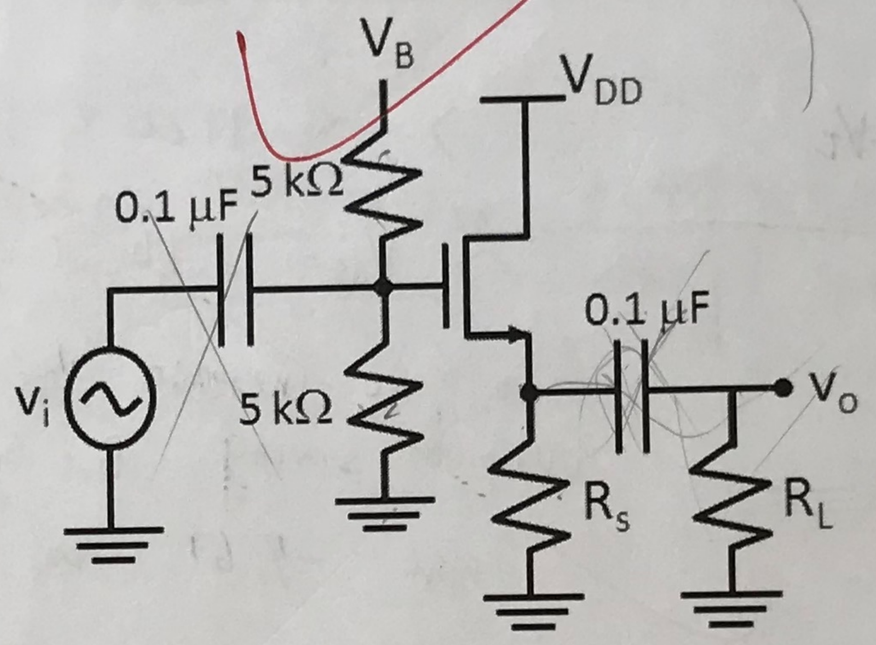


Fig. 3: Use different load resistors to test a CD amplifier.

2. Add an additional resistor R_L and a coupling capacitor 0.1 μF as shown in Fig. 3 for the CD amplifier design. Use R_L values of 1 KΩ and 10 KΩ, respectively, and measure the mid-band small-signal gain. This test is to investigate the effect of the load resistor on a CD amplifier. Compare the results under the two different loads. Also, compare the measured results with hand calculation. Comment on what you observe.

$(v_o/v_i)_{measured,\ 1k\Omega}$ = 0.464; $(v_o/v_i)_{measured,\ 10k\Omega}$ = 0.686.

$(v_o/v_i)_{calc.,\ 1k\Omega}$ = 0.476; $(v_o/v_i)_{calc.,\ 10k\Omega}$ = 0.718.

Comment:

when R_D = 10K, $R_S // R_D$ = 3750 Ω

I_D = 256u, $g_m = 6.28 \times 10^{-4}$

$r_o = 7.26 \times 10^5$

$\therefore A_V = 0.718$ #

$A_V = \frac{g_m (R_S // r_o // R_L)}{1 + g_m (R_S // r_o // R_L)}$

$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_{th})^2$

$\Rightarrow 2230 I_D = [1.72 - I_D (R_S // R_L)]^2$

when R_L = 1K, $R_S // R_L = \frac{6 \times 10^6}{7 \times 10^3} = 857\ \Omega$

$\rightarrow I_D$ = 627u $g_m = 1.065 \times 10^{-3}$; $r_o = 2.977 \times 10^5\ \Omega$

$\therefore A_V = 0.476$ #

Error rate

1KΩ → $\frac{0.464 - 0.476}{0.476} \sim -2.5\%$

10KΩ → $\frac{0.686 - 0.718}{0.718} \sim -4.45\%$

Calculation is closed to measured result

C. Design of a common-gate amplifier

1. Build a common-gate amplifier (Fig. 4) with the transistor without body effect (node 6-7-8) on your breadboard. Use the load resistor that you obtained in A-1 for the common-source amplifier. Apply a gate DC bias voltage of 2.0 V and V_{DD} of 5.0 V. Apply a small signal v_i at the source of the transistor and measure the mid-band small-signal gain v_o/v_i. Please also write down the previous common-source amplifier gain for comparison.

$(v_o/v_i)_{measured,\ CG}$ = 6.59 ; $(v_o/v_i)_{measured,\ CS}$ = -7.69 ;

2. Perform hand calculation based on the transistor parameters extracted in Lab 6. Compare the measured results with hand calculation and comment on what you observe.

$(v_o/v_i)_{calc.,\ CG}$ = 6.638 ;

Comment:

1. As there is a internal (R_{sig}) resistance at function generator, small signal gain is divided by a factor $(1+g_mR_{sig})$. So gain of CG stage is less than that of CS stage.

2. Measured gain is a little bit lower than calculated one, I think it's because internal resistance, R_{sig} is larger than 50Ω (assumed in hand calculation) $\Rightarrow A_V = \frac{g_mR_L}{1+g_mR_{sig}}$ would be a little lower.

$A_V = \frac{g_mR_L}{1+g_mR_{sig}}$

$I_D = \frac{1}{2}k_n\frac{W}{L}(V_{GS}-V_{th})^2$, $V_{GS} = V_G - 50I_D$

$\Rightarrow (2-50X-1.28)^2 = 2230X$ $(I_D = X)$

$\Rightarrow X = 210\ uA$

$g_m = \frac{2\times210\times10^{-6}}{0.7049} = 5.979\times10^{-4}$

$A_V = \frac{5.974\times11.8\times10^{-1}}{1+5.974\times50\times10^{-4}}$

≈ 6.638

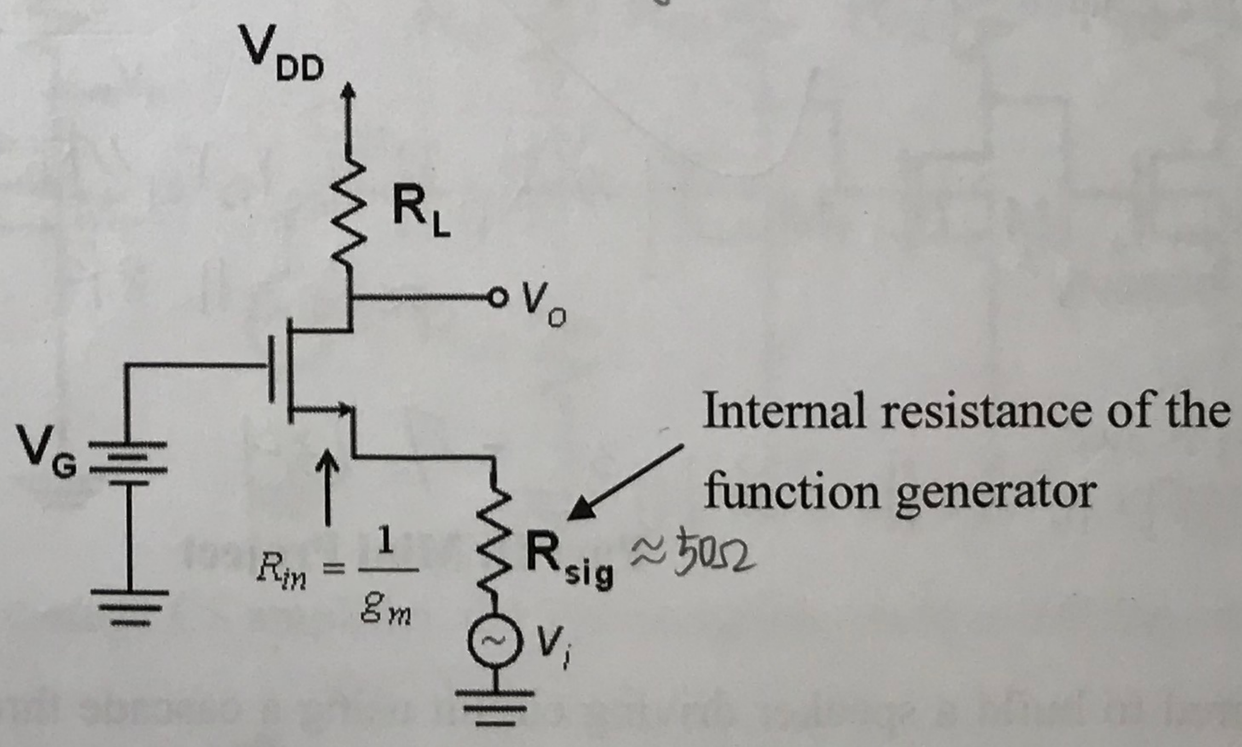
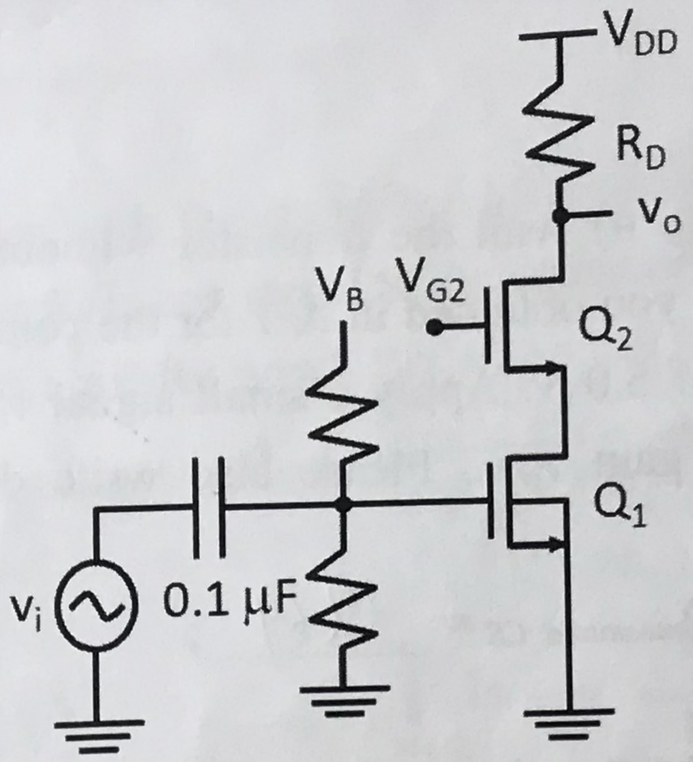


Fig. 4: Schematic of the common-gate amplifier.



$R_{out} = (1+g_{m2}r_{o1})(R_D /\!/ r_{o2})$

Fig. 5: The cascode amplifier.

D. Design of a cascode amplifier

1. Combine the common-source and common-gate stages to build a cascode amplifier (Fig. 5) on your breadboard. The gate bias of the CS stage is 2.0 V. Please adjust the gate bias of the CG stage to achieve the same DC current as that with the CS stage. The applied V_{DD} is 5 V and the load R_D is the same as that used in A-1. Measure the drain-source voltage drops for both stages. Make sure both transistors are in the saturation region. You can adjust V_{DD} if one of the transistors enters the linear region, but the drain current should be kept the same.

$V_{GS2} = 3V$

$V_{DS,\,Q1}$ = 0.781 V; $V_{DS,\,Q2}$ = 1.4708 V;

2. Measure the mid-band small-signal gain of the amplifier and compare that with the value by hand calculation. Give a brief comment on what you observe.

Comment: measured gain = -7.62

Calculation result is close to measured result!

Hand Calculation:

$R_{out} = \left[(1+g_{m2}r_{o2})r_{o1} + r_{o2}\right] /\!/ R_D \approx g_{m2}r_{o2}r_{o1} /\!/ R_D$

$\approx R_D = 11.8K$

$A_v = -g_{m1}R_{out}$

$= -647\times10^{-6}\times11.8\times10^{3} = -7.634$

Part II. Mini Project

1. You are required to build a speaker driving circuit using a cascade three-stage common-source amplifier as shown in Fig. 6(b). You will have to use the CD4007UB MOSFET array and the power transistor VN0606 to build the first two stages and the output stage, respectively. The first two-stage amplifier is shown in Fig. 6(a). Based on the experience obtained in Part I, please design the bias point of M1 through R_{G1} and R_{G2}, and design the load resistors R_{D1} and R_{D2} to have a combined gain of at least 50 (V/V) for the first two stages. Set the power supply voltage to 5.0 V. Perform hand calculation and compare with the measured results. Check if the upper -3dB frequency is larger than 20 kHz.

Gain of the first two stages: Measured = 64; calculated = 5055.

two-stage CS amplifier,

Comment:

$A_v = g_{m1} R_{D1} g_{m2} R_{D2}$

From part I, $g_{m1} = 649u$

$R_{D1} = 11.8K\Omega$

$\Rightarrow V_d = 5 - 233\times10^{-6} \times 11.8\times10^{3}$

$= 2.2506$

$g_{m1}R_{D1} = 7.65$ (1st stage gain)

$g_{m2} R_{D2} \geq 6.53$

$I = \frac{1}{2} u_n C_{ox} \frac{W}{L} (2.2506 - 1.2816)^2$

$= 421u$

$g_{m2} = \frac{2I}{V_{od}} = 868\,u$

$R_{D2} \geq \frac{6.53}{868u}$

$\geq 7523\Omega$ 取 $R_{D2} = 9K\Omega$

2. You are advised to extract the VN0606 transistor model (e.g. threshold voltage) by *i-v* measurements as performed in Lab 6, in order to design the last stage of the speaker driving circuit as shown in Fig. 6(b). The complete circuit has to achieve a total gain of at least 25. Describe your design process below.

As first two stages has reach gain = 50, and overall gain has to be larger than 25

$\Rightarrow$ the last stage gain ≥ 0.5. By the calculation above, $V_{D2} = V_{G3} = 5 - 421u \cdot 9K = 1.211\,V$

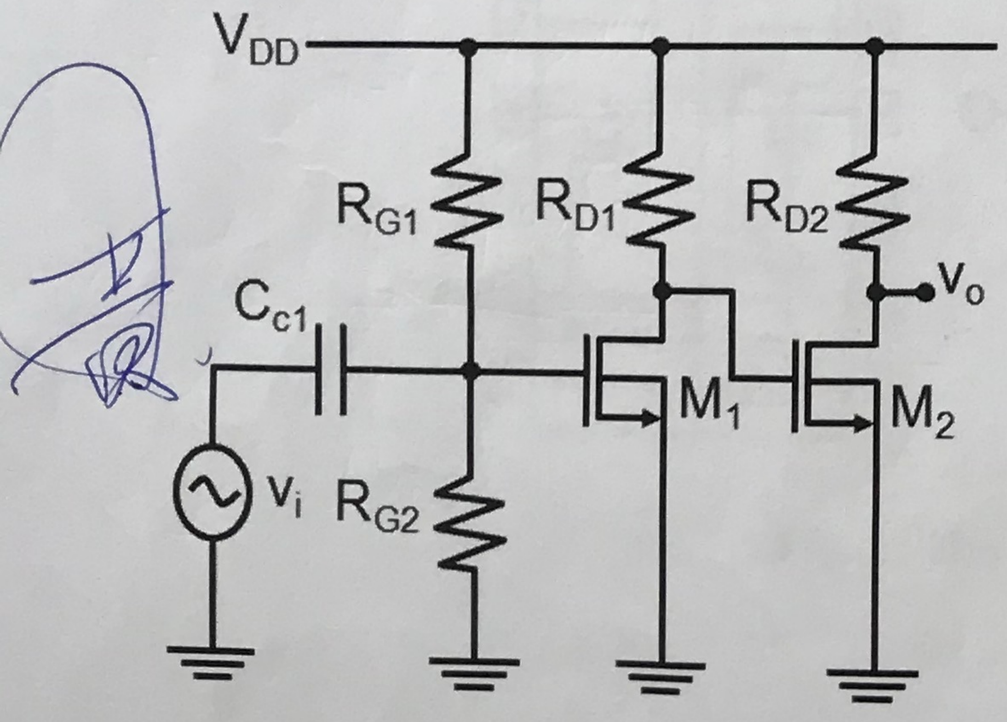
$I_{D3} = \frac{1}{2} K_n \frac{W}{L} (V_{od})^2 = 137u$

$g_m = \frac{2I_D}{V_{od}} = 1.37\times10^{-3}$

$A_v = 1.37\times10^{-3} \cdot R_{D3} \geq 0.5 \Rightarrow R_{D3} \geq 364\Omega$

But, we actually choose $R_{D3} = 150\Omega$ to complete. It's probably because parasitic resistance in the wire.

For demonstration, you need to apply an input signal of 20 mV (amplitude), from a functional generator, with increasing frequencies from 500 Hz to 20 kHz. The sound from the speaker should be heard by the TA.



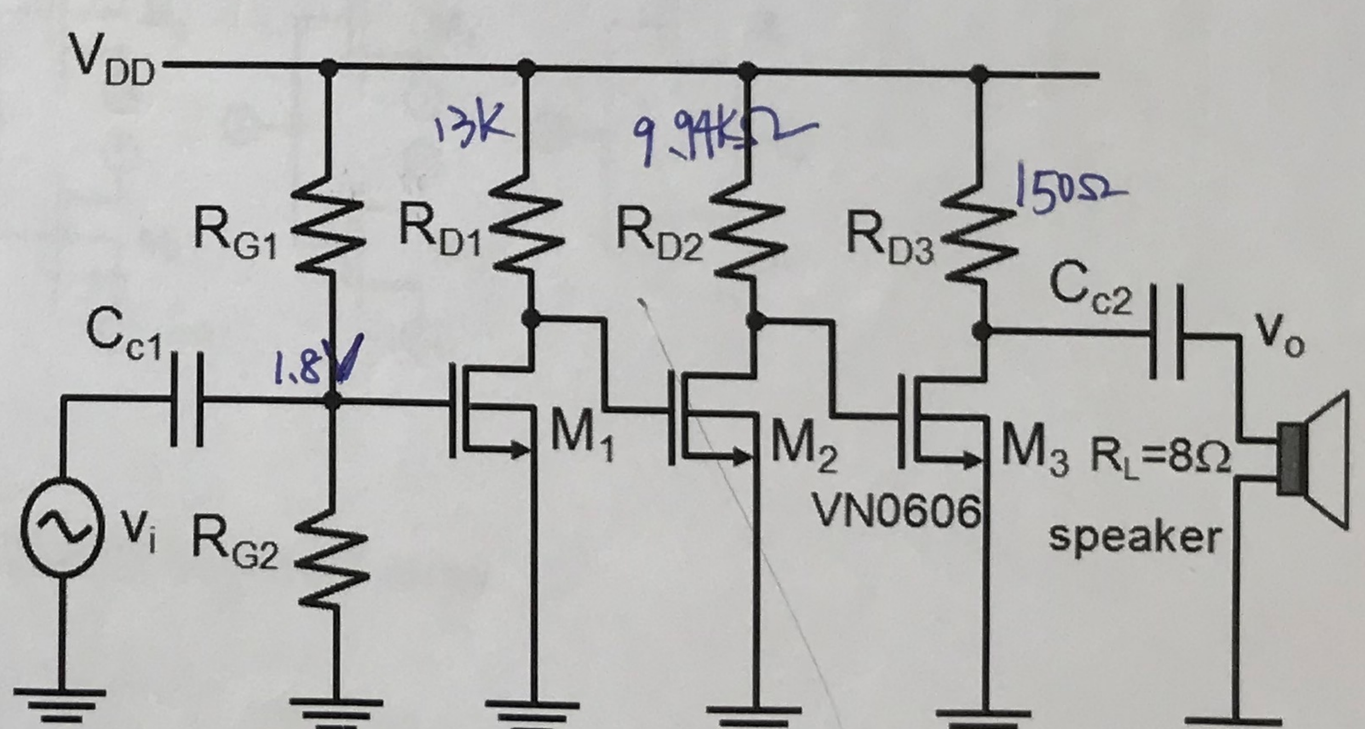


Fig. 6: (a) A cascade two-stage CS amplifier. (b) The complete speaker driving circuit.

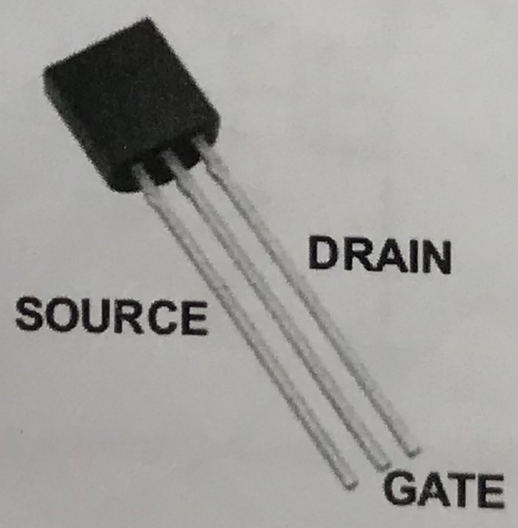


Fig. 7: The VN0606 chip.