EE2245 Microelectronics Lab

Final Exam Solutions

解答

1. (10%)

(a) (6%) For the circuit shown in Fig. 1(a), please determine the load resistance R_L between the terminals a-b to result in maximum power transfer.

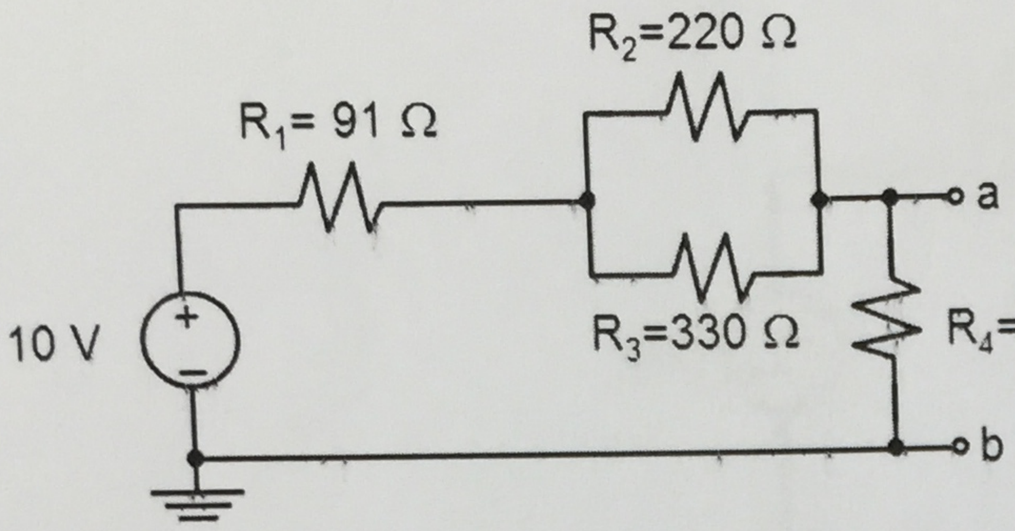


Fig. 1(a)

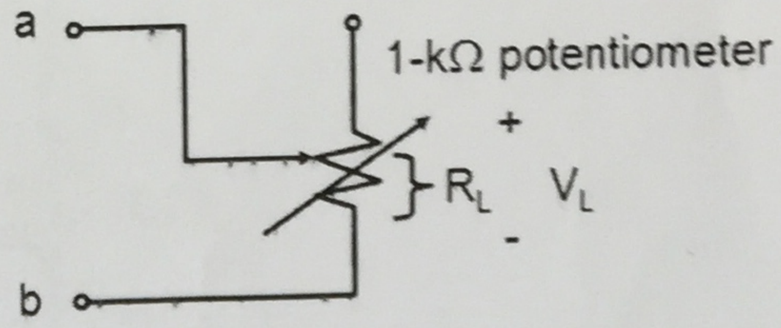


Fig. 1(b)

(b) (4%) The circuit in Fig. 2(a) can be represented as a Norton-equivalent circuit in Fig. 2(b). Please determine the value of I_N.

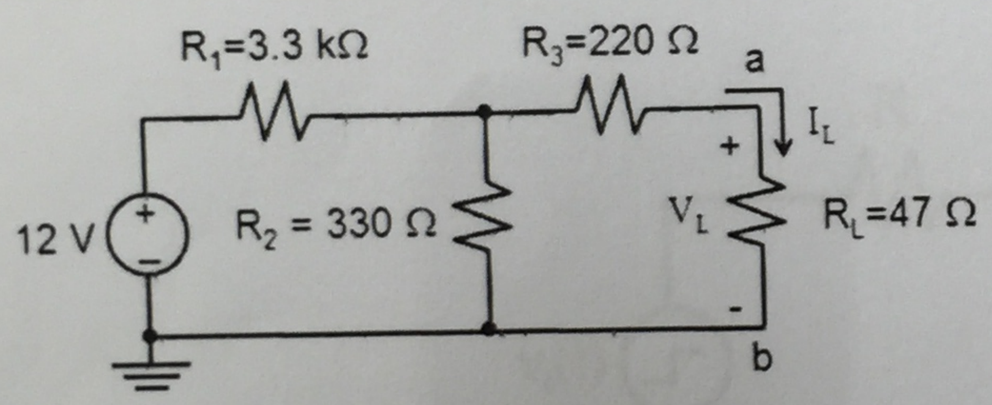


Fig. 2(a)

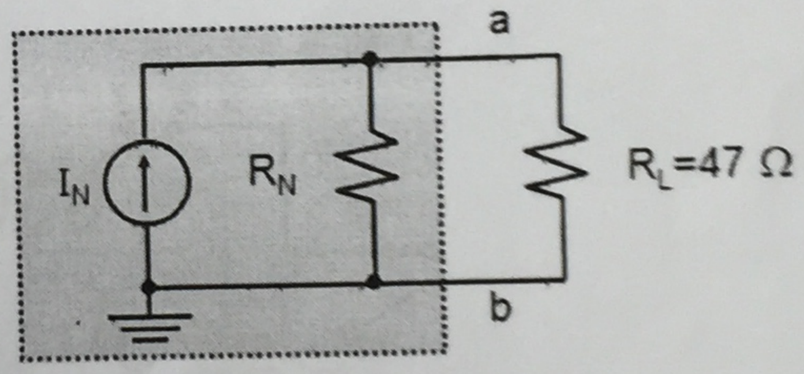


Fig. 2(b)

Sol.

(a) By Thévenin's Theorem:

$$V_{th} = 10V \cdot \frac{R_4}{(R_1 + (R_2 \parallel R_3)) + R_4} = 6.782\ V$$

$$R_{th} = [R_1 + (R_2 \parallel R_3)] \parallel R_4 = 151.24\ \Omega$$

Maximum power transfer is achieved when $R_L = R_{th} = 151.24\ \Omega$.

(b) By measuring the short-circuit current between terminals a-b with $R_L = 0$, we get

$$I_N = 12\,V / [3.3k\Omega + (220\Omega \parallel 330\Omega)] \times \frac{330\Omega}{220\Omega + 330\Omega} = 0.0021\,A$$

2. (15%)

(a) (8%) For the R-C circuit shown in Fig. 3(a), the input square waveform $v_i(t)$ has a minimum and a maximum values at 0 and 1 V, respectively. The period of $v_i(t)$ is also large enough for the output $v_o(t)$ to reach the steady state. Please derive $v_o(t)$ when $v_i(t)$ rises from 0 to 1 V. Also, please draw one period of the output waveform $v_o(t)$ ($v_i(t)$ = $0 \rightarrow 1$ V and $1 \rightarrow 0$ V) and explain your reasoning.

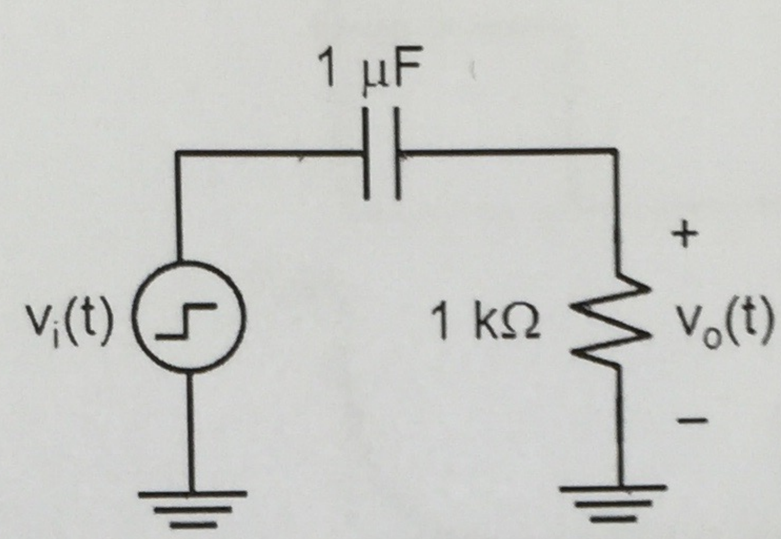


Fig. 3(a)

(b) (7%) For the R-L-C circuit as shown in Fig. 3(b), the input $v_i(t)$ is a unit-step with R = 10 Ω, L = 1 H, and C = 10 mF. Assume the initial condition $v_o(0) = 0$, please calculate the overshoot in the step response.

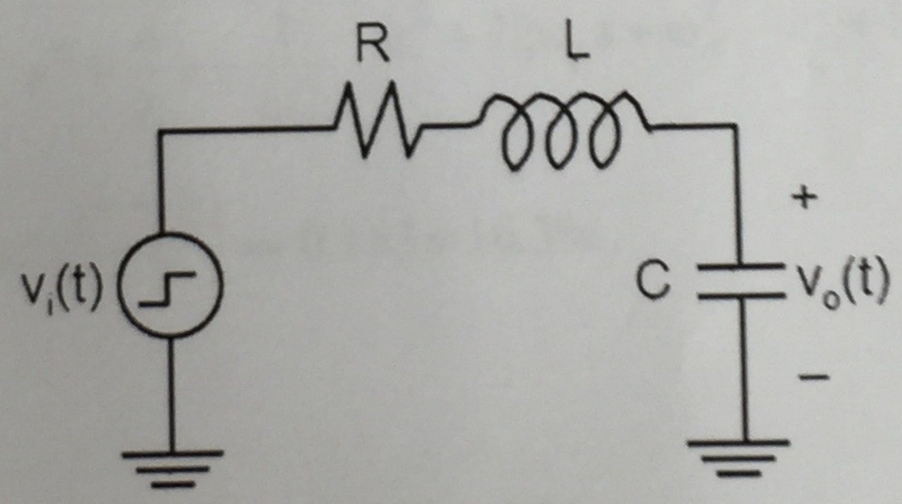


Fig. 3(b)

Sol.

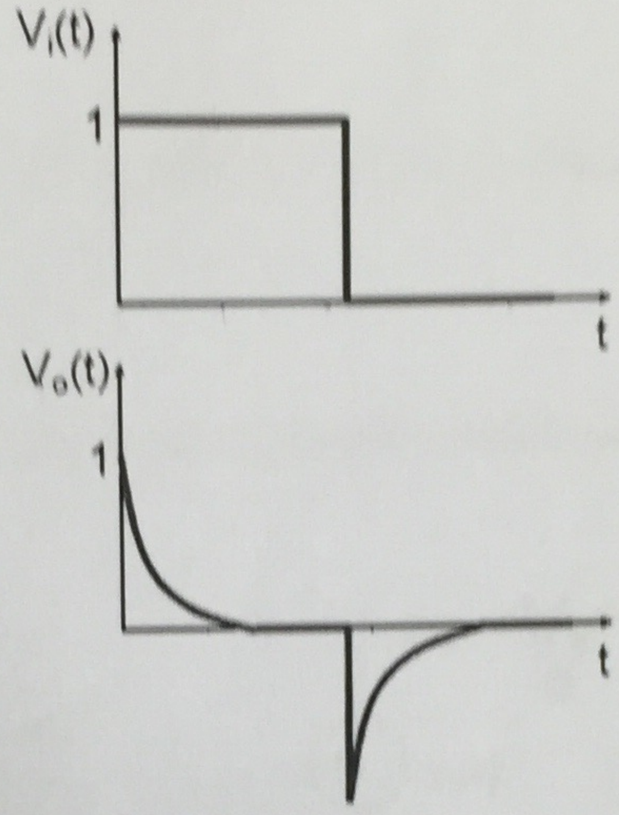
(a) $\dfrac{v_o(s)}{v_i(s)} = \dfrac{sRC}{1+sRC}$

When v_i increases from 0 to 1 V:

$$v_i(s) = \frac{1}{s},\ then\ v_o(s) = \frac{1}{s+\dfrac{1}{RC}} \therefore v_o(t) = e^{-\frac{1}{RC}t} = e^{-10^3 t} \quad \text{for } t \geq 0.$$

When $v_i(t)$ decreases from 1 to 0 V:

The voltage across the capacitor remains 1 V at the instant when $v_i(t)$ reduces to 0 V, making the voltage across the resistor $v_o(t)$ equal to -1 V by KVL. After that $v_o(t)$ will increase with the RC time constant to the steady-state value of 0 V. A complete period of $v_o(t)$ is shown below.



(b)

$$\frac{v_o(s)}{v_i(s)} = \frac{\frac{1}{sC}}{R+sL+\frac{1}{sC}} = \frac{\frac{1}{LC}}{s^2+\frac{R}{L}s+\frac{1}{LC}} = \frac{\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2} = \frac{100}{s^2+10s+100}, so\ \omega_n = 10, \xi = 0.5$$

Overshoot = $\exp\left(-\xi\pi/\sqrt{1-\xi^2}\right) == 0.163 = 16.3\%$.

3. (15%)

(a) (8%) The sinusoidal input and output waveforms of a 1st-order RC high-pass filter differ by 0.7854 second when the input frequency is 1 rad/sec. Given that R is 1 kΩ, please calculate the capacitance value.

(b) (7%) Please use one resistor (R), one capacitor (C), and one inductor (L) to implement a passive band-pass filter. Please indicate the input $v_i(t)$ and output $v_o(t)$, and derive the transfer function $v_o(s)/v_i(s)$.

Sol.

(a) The period for ω = 1 rad/sec: $T = \frac{2\pi}{\omega} = 6.2832$ sec

Based on a time difference $\Delta T = 0.7854$ sec, the phase difference

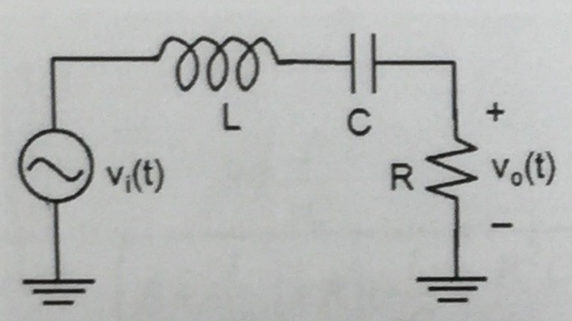
$$\Delta\theta = \frac{\Delta T}{T} \cdot 360° = 45°$$

Transfer function of a 1st-order RC high-pass filter is $F(s) = \frac{v_o(s)}{v_i(s)} = \frac{sRC}{1+sRC}$, thus

$$\angle F(j\omega) = 90° - \tan^{-1}(\omega RC)$$

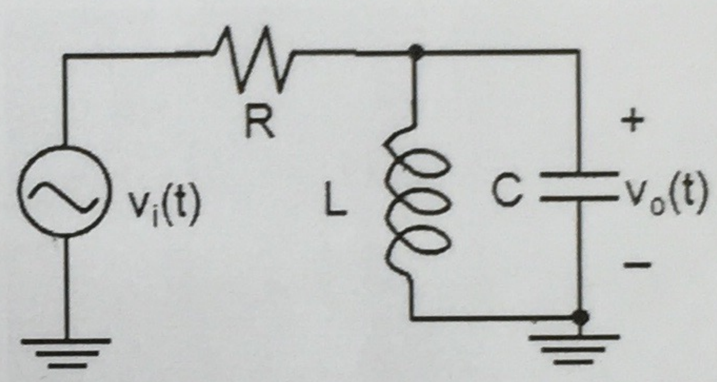
Since $\angle F(j1) = 90° - \tan^{-1}(RC) = 45°$ and R = 1 kΩ, we obtain C = 1 mF.

(b) Either of the circuits as shown below can be implemented as a band-pass filter.



$$\frac{v_o(s)}{v_i(s)} = \frac{R}{R + \left(sL + \frac{1}{sC}\right)}$$

$$= \frac{RCs}{LCs^2 + RCs + 1}$$



$$\frac{v_o(s)}{v_i(s)} = \frac{Ls}{LRCs^2 + Ls + R}$$

4. (15%)

(a) (10%) Please derive the oscillation frequency of the circuit in Fig. 4(a) and determine the R_1/R_2 ratio to start oscillation.

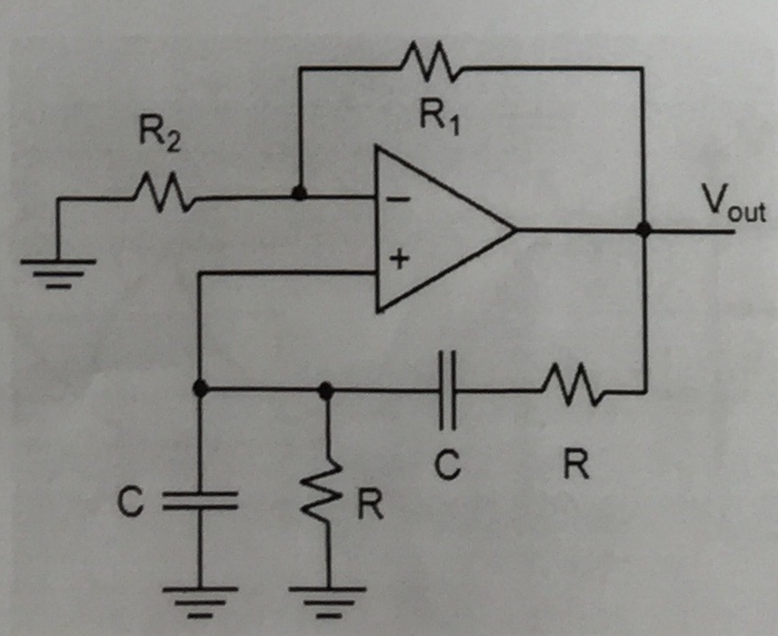


Fig. 4(a)

(b) (5%) Given the circuit and its output waveform as shown in Fig. 4(b), please draw the waveforms of V^+ and V^- in the figure and mark their maximum and minimum values.

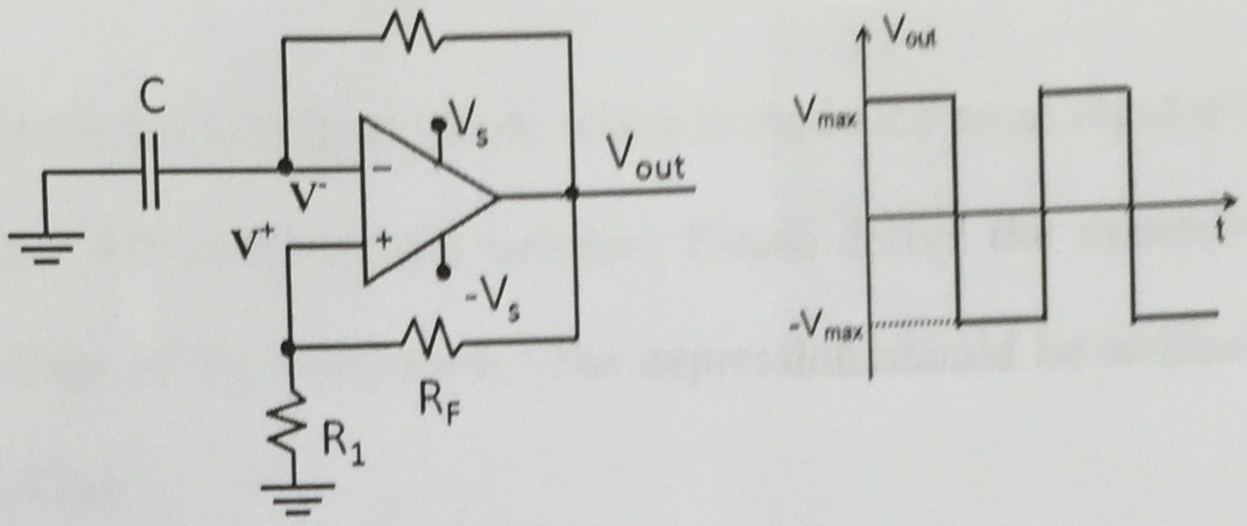


Fig. 4(b)

Sol:

(a)

$$\frac{V^+(s)}{V_{out}(s)} = \frac{R \| \frac{1}{sC}}{\left(R + \frac{1}{sC}\right) + R \| \frac{1}{sC}} = \frac{sRC}{R^2C^2s^2 + 3RCs + 1}$$

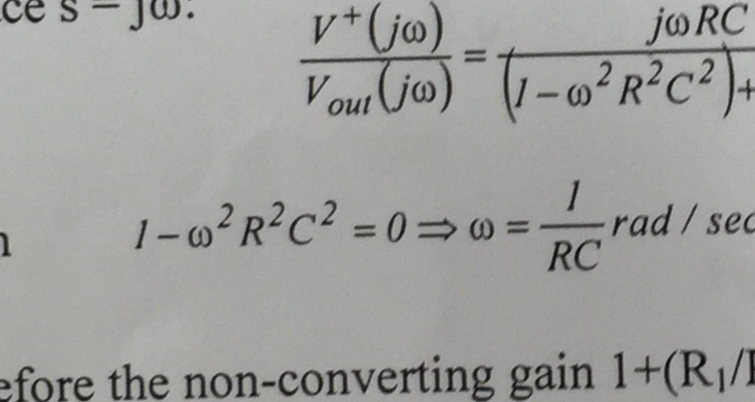
Replace s = jω:

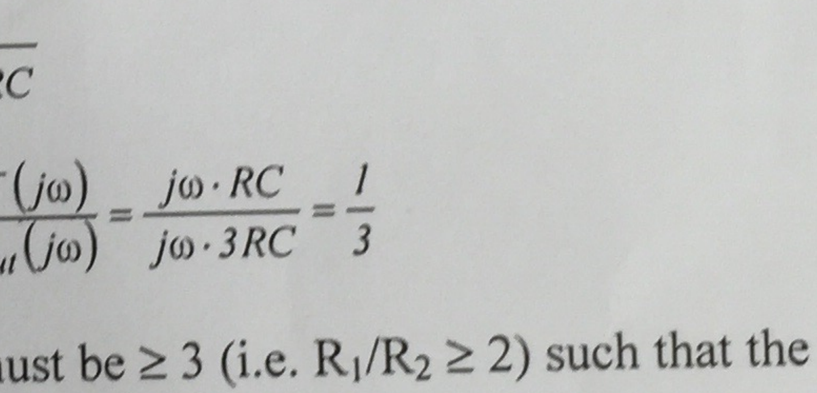
$$\frac{V^+(j\omega)}{V_{out}(j\omega)} = \frac{j\omega RC}{\left(1 - \omega^2 R^2 C^2\right) + j\omega 3RC}$$

When $1 - \omega^2 R^2 C^2 = 0 \Rightarrow \omega = \frac{1}{RC} rad/sec \therefore \frac{V^+(j\omega)}{V_{out}(j\omega)} = \frac{j\omega \cdot RC}{j\omega \cdot 3RC} = \frac{1}{3}$

Therefore the non-converting gain $1+(R_1/R_2)$ must be ≥ 3 (i.e. $R_1/R_2 \geq 2$) such that the loop gain will be ≥ 1 to start oscillation. The phase around the loop is 0° to satisfy the oscillation condition.

(b)





5. (15%) Consider the circuit in Fig. 5. Let $R_2C_2 > 100\ R_1C_1$

(a) (10%) Assume the Opamp is ideal. Please **plot the gain and phase responses** of $\mathbf{H}(w)=\mathbf{V_O/V_i}$ up to $w = 10/\ R_1C_1$. Please mark the pole frequencies and phase angles clearly in your plot.

(b) (5%)Assume the Opamp has a nonzero offset, which is modelled as an input offset voltage V_{OS} connecting at the positive input terminal. Please derive **the expression for the DC output voltage** of Vo when Vi=0. (The expression should be written in terms of R_1, C_1, R_2, C_2, V_{OS})

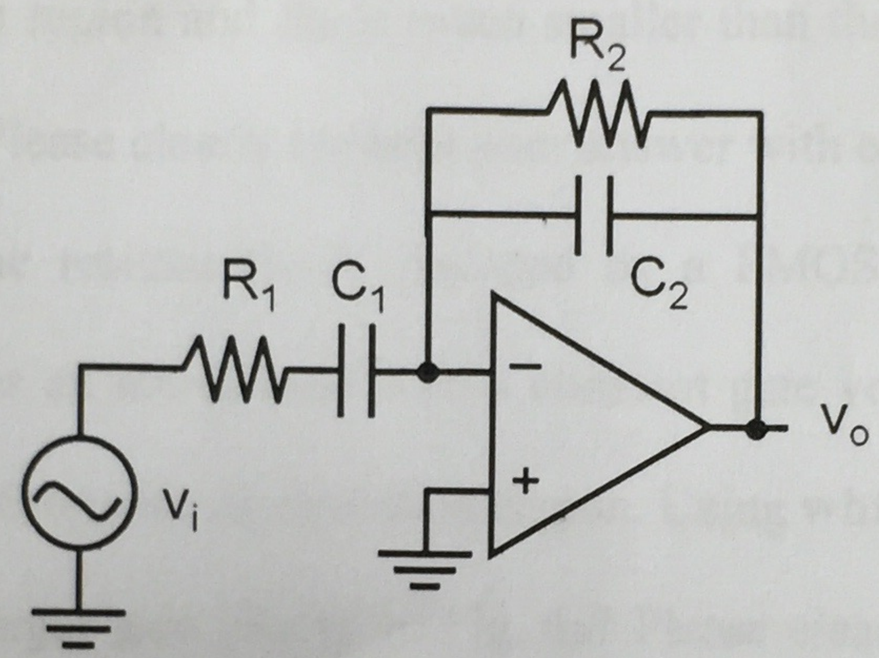


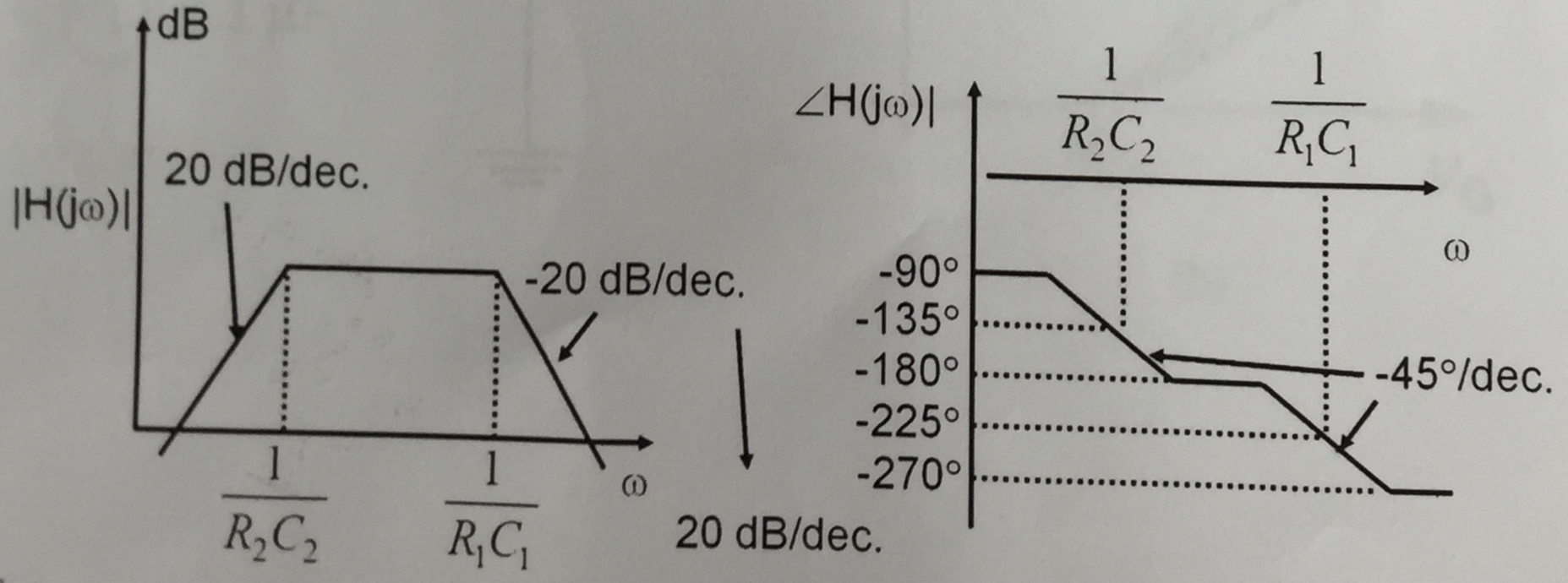
Fig.5

Sol:

(a)The frequency response is given as

$$H(s)=\frac{v_o(s)}{v_i(s)}=-\frac{R_2}{R_1}\frac{sR_1C_1}{sR_1C_1+1}\cdot\frac{1}{sR_2C_2+1}$$

It has a zero at s=0 and two poles, one at $1/\ R_1C_1$, the other at $1/\ R_2C_2$. As $R_2C_2 > 100\ R_1C_1$, the gain and phase response are plotted as



Note: a zero contributes 90°. The minus sign contributes either 180° or -180°, so the phase can start from 270° at ω = 0 to 90° at ω = ∝, or -90° at ω = 0 to -270° at ω = ∝.

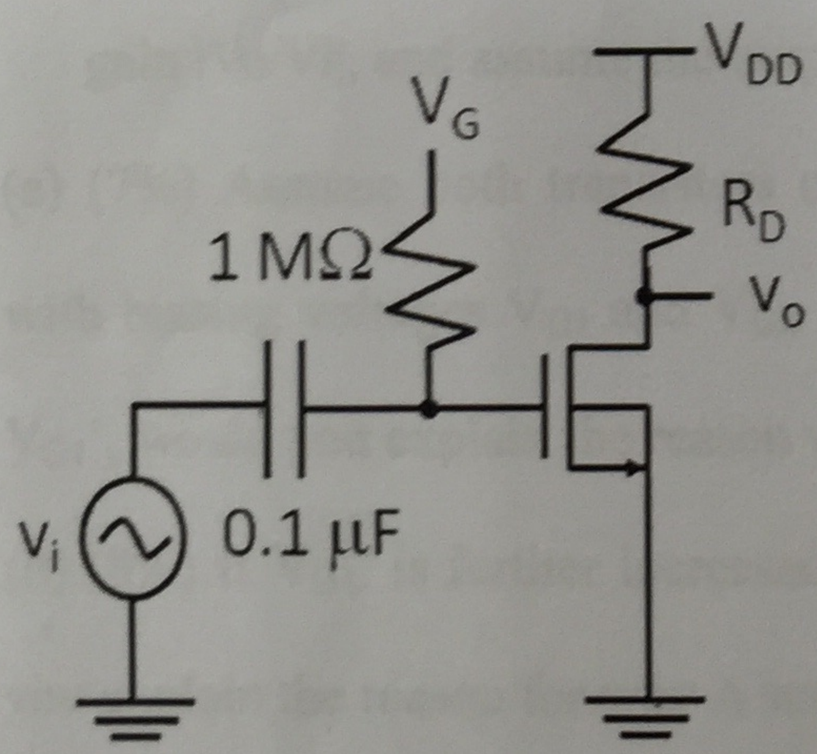
(b) the gain due to V_{os} is $G(s)=1+\frac{R_2}{R_1}\frac{sR_1C_1}{sR_1C_1+1}\cdot\frac{1}{sR_2C_2+1}$

At DC ($s = j\omega = 0$), the gain = 1. Therefore, $V_o = V_{os}$.

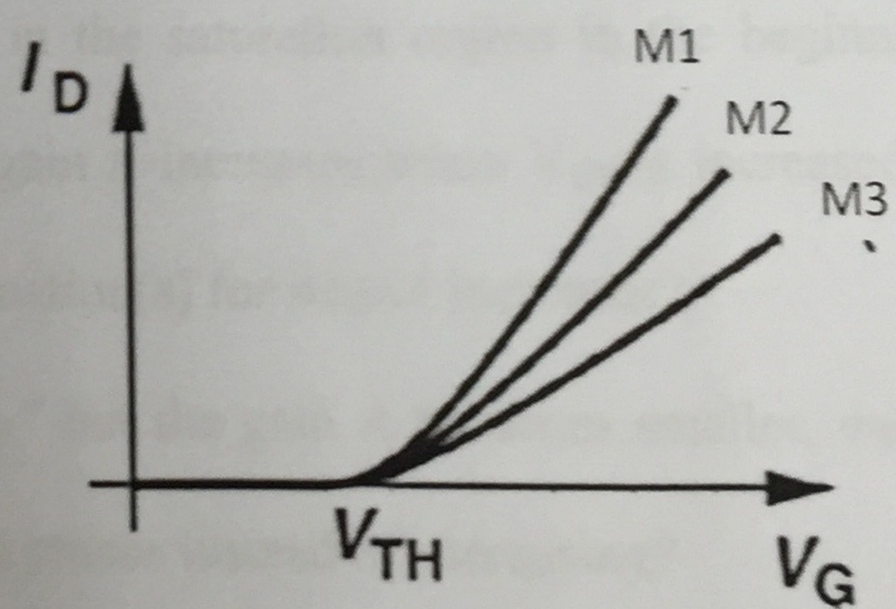
6. (15%) Fig. 6a shows a single transistor amplifier. Fig. 6b shows the measured I_D-V_G curves of three different NMOS transistors. Fig. 6c shows the $|I_D|$-$|V_{DS}|$ curves of two different PMOS transistors.

(a) (8%) Given the same biasing voltage and R_D. Using **which NMOS transistor** in Fig.6b will result in a largest voltage gain |Vo/Vi| in Fig. 6a? Assume the transistor operates in saturation region and R_D is much smaller than the small-signal resistance r_{ds} of all transistors. Please clearly **explain** your answer with equation(s).

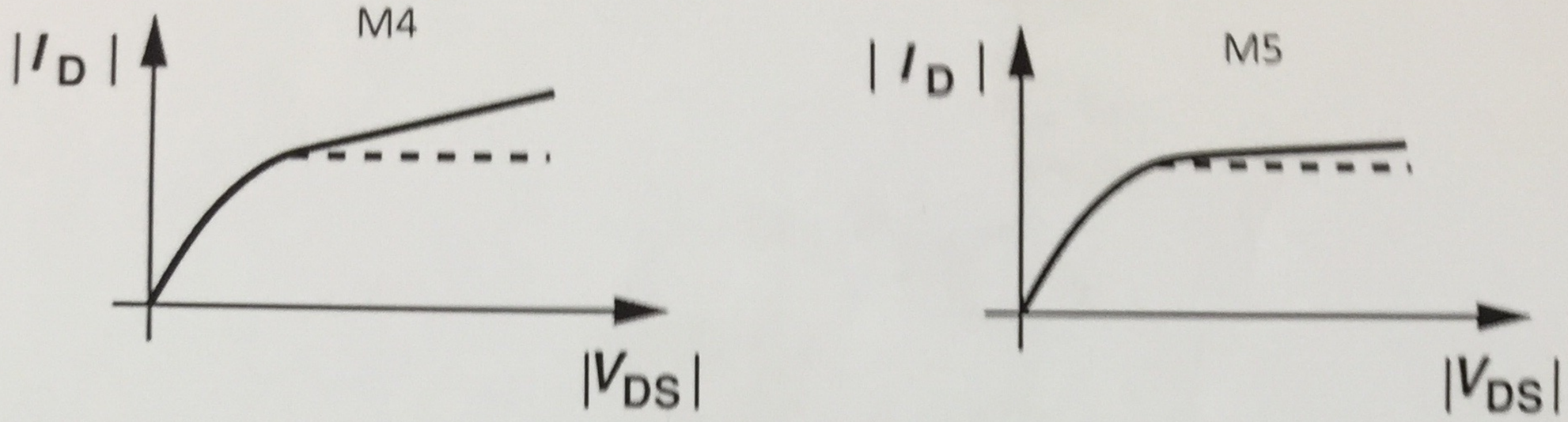
(b) (7%) Assume the resistor R_D is replaced by a PMOS transistor. The PMOS transistor functions as an active load with a constant gate voltage. Assume both the PMOS and the NMOS operate in saturation region. Using **which PMOS transistor** in Fig.6c will result a larger gain |Vo/Vi| in Fig. 6a? Please clearly **explain** your answer with equation(s).



(a)



(b)



(c)

Fig. 6

Sol:

(a) M1.

Because M1 has a steepest I_D-V_G curve, which corresponds to a largest current and largest transconductance (g_m) for the same biasing voltage V_G

(Note: $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2$; $g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})$).

Since the gain of the amplifier in Fig. 6a is -gm*R_D, M1 will provide the largest gain

(b) M5.

Because the gain of the amplifier is given as $-g_{mn}*(r_{dsn}//r_{dsp})$, where g_{mn} is the transconductance of the NMOS. r_{dsn} and r_{dsp} are the small-signal resistance of NMOS and PMOS. respectively. Fig. 6c shows that M5 has a larger r_{ds} than M4 with a smaller λ (note: $r_{ds} = \frac{1}{\lambda I_D}$). Therefore, using M5 gives a larger voltage gain.

7. (15%) Consider the cascode amplifier circuit in Fig. 7. Let *A* represent the voltage gain |Vo/Vi|, and assume the output resistance at Vo is approximately equal to R_D.

(a) (7%) Assume both transistors operate in the saturation region in the beginning with biasing voltages V_{G1} and V_{G2}. If the gain *A* increases when V_{G1} is increased to V_{G1}', would you explain the reason with equation(s) for why *A* increases?

(b) (8%) If V_{G1}' is further increased to V_{G1}" but the gain A becomes smaller, would you explain the reason for why A starts to decrease instead of increasing?

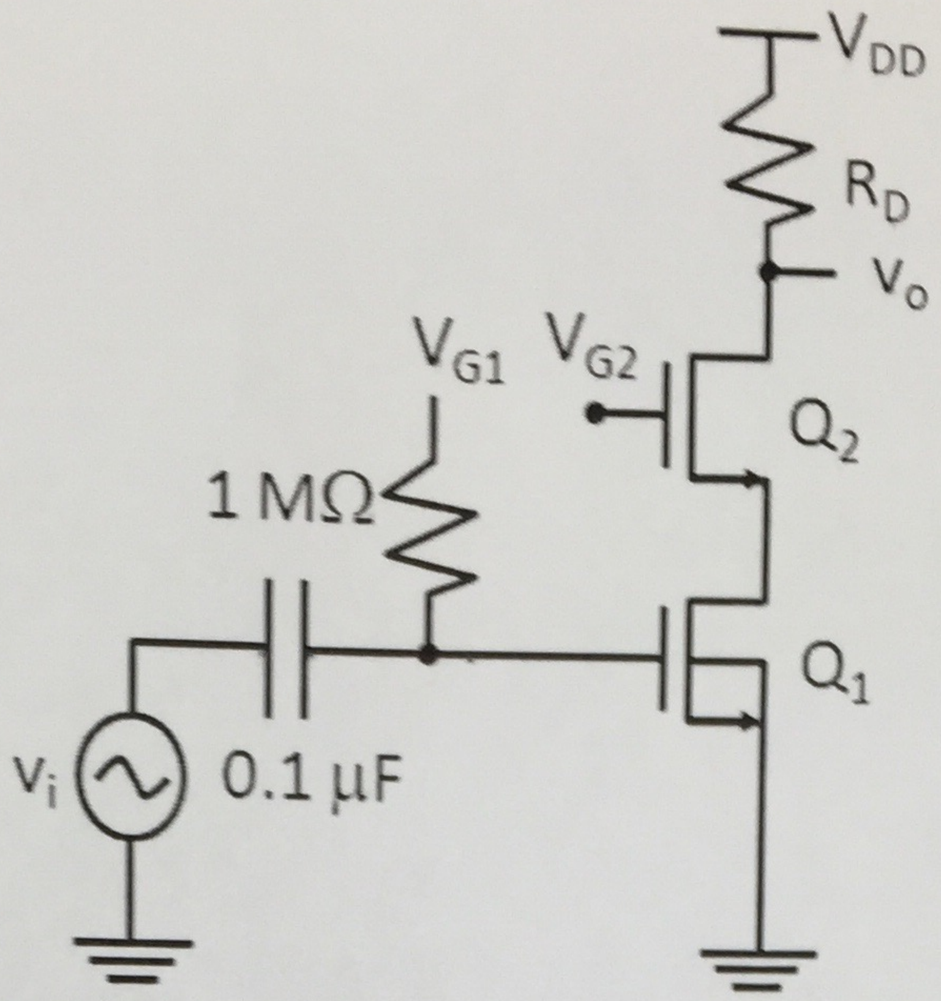


Fig. 7

Sol:

The amplifier has a gain $A = -g_{m1} * R_D$

(a)Increasing V_{G1} causes the biasing current of Q1/Q2 to increase. The transconductance g_{m1} is thus increased, so is the gain A.

(b) Further increasing V_{G1} will result in larger V_{GS} for both Q1 and Q2. The voltage across R_D also increases. As a result, both changes below could cause gain to reduce

(i) Q1 enters triode operation because both V_{GS2} and V_{G1} continue to increase

→ g_{m1} reduces → A reduces

(ii)Q2 enters triode operation because the voltage drop across R_D increases.

→ the small-signal resistance looking into the drain of Q2 decreases

→R_D no longer dominates the small-signal output resistance at Vo, so that the total small-signal resistance at Vo reduces

→ A reduces

(iii) both Q1 and Q2 enter triode regions because of the reasons above.