EE2245 Microelectronics Labs

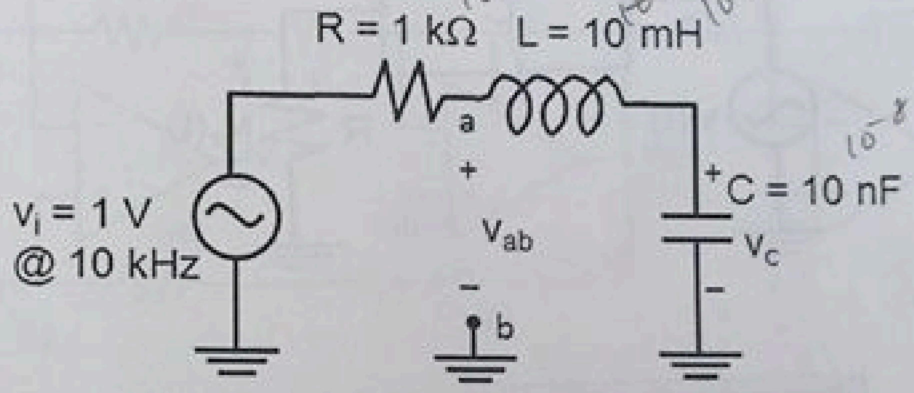
Final Exam

Date: January 14, 2014

1. AC response (10%)

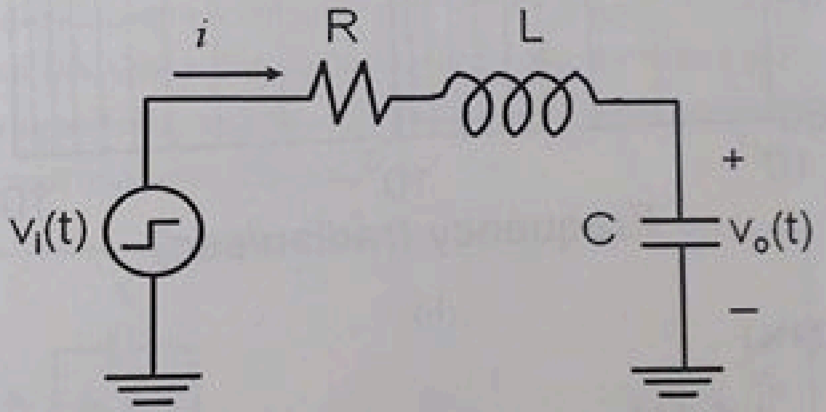
(a) (5%) For the RLC circuit as shown, the input v_i is a sinusoidal signal of 1 V (amplitude) at 10 kHz, please calculate the amplitude of v_{ab} at steady state.

(b) (5%) You are free to adjust the input frequency and observe the output v_c on the capacitor. Please calculate the frequency at which you will observe v_c lags v_i by 90°.



2. Time-domain responses (16%)

Consider the circuit as shown. Let $v_i(t)$ be a square-wave voltage with a minimum value at 0 V and a maximum value at 1 V.



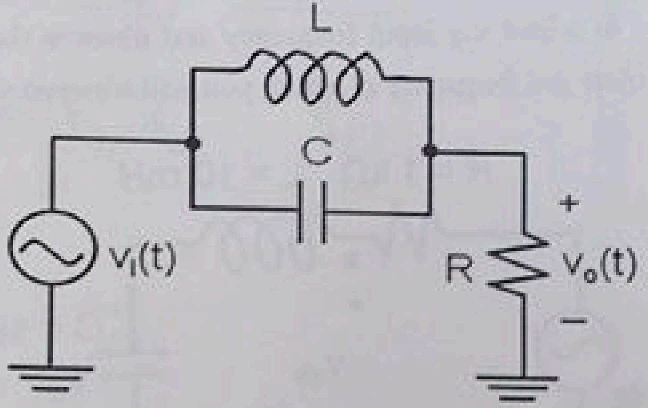
(a) (6%) Please derive **the condition (in terms of R, L, C) for the corresponding** response of $v_o(t)$ to be **underdamped.**

(b) (6%) Assume the circuit is underdamped, and the response of $v_o(t)$ exhibit overshoots. **Which action(s)** below would **cause the maximum overshoot to increase**? (i) Increase R (ii) Increase L (iii) Increase C (iv) Increase the frequency of $v_i(t)$. Please **explain your answer** clearly.

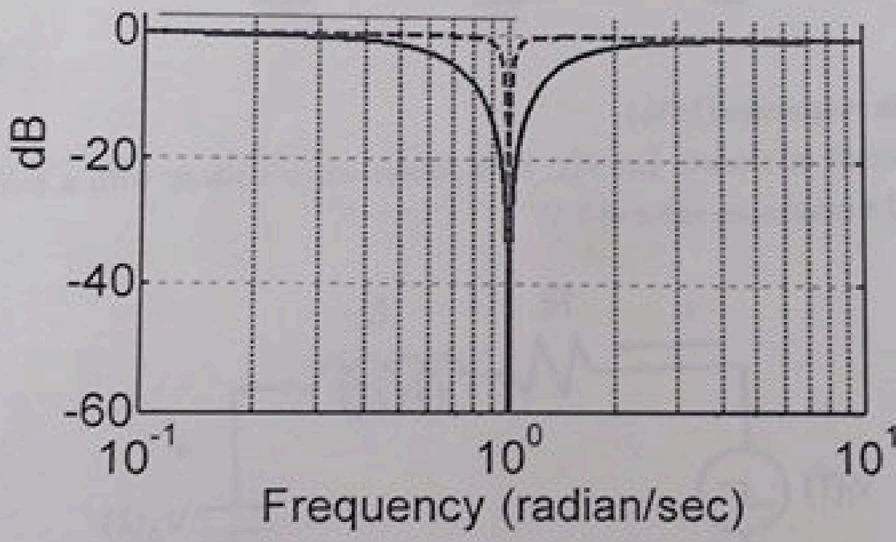
(c) (4%) If the square-wave voltage source exhibit a **source resistance compatible to R, will the overshoot increase or decrease?** Please **explain your answer** clearly.

3. Passive filters (8%)

Consider the band-reject filter in Fig.3a. Assume its frequency response is shown by the black solid curve in Fig.3b. If we would like to **enhance the selectivity of the filter** (i.e. modify the frequency response to be the one shown by the dashed curve in Fig.3b), **should R be increased or decreased?** Please **explain your answer** clearly.

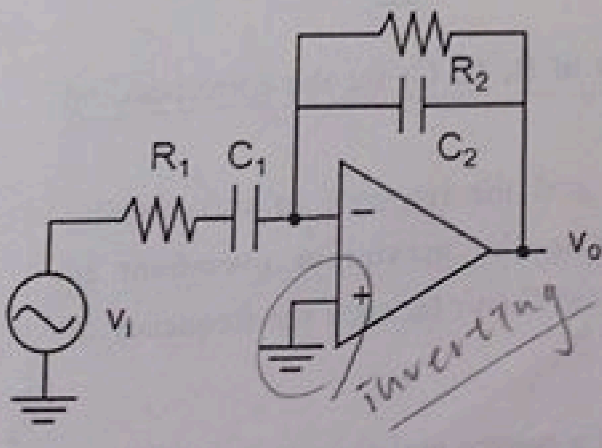


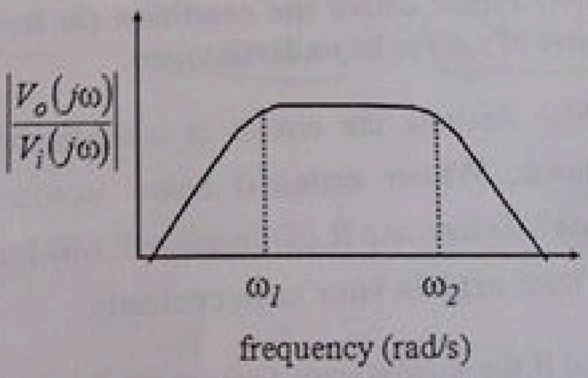
(a)



(b)

4. Active filter (20%)

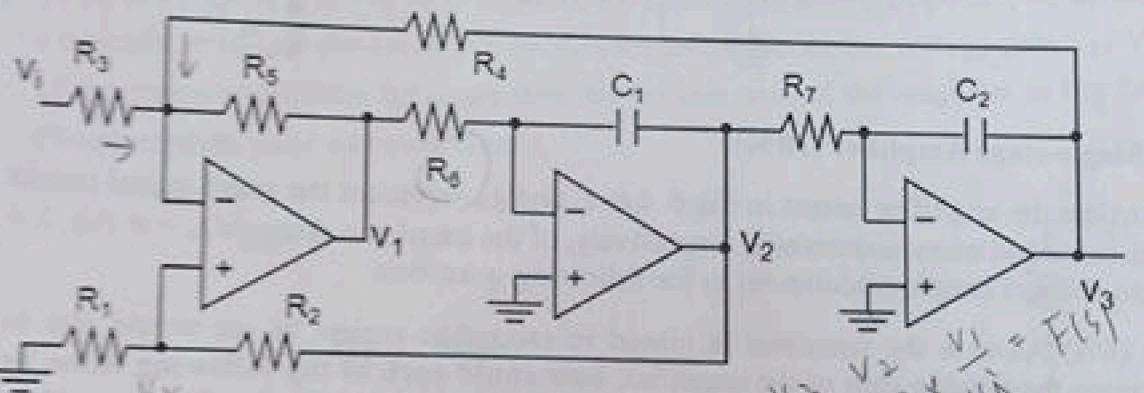




(a) (8%) Please derive the transfer function $V_o(s)/V_i(s)$ of the filter as shown above.

The frequency response on the right shows the corner (-3 dB) frequencies ω_1 and ω_2. For $R_1C_1 > R_2C_2$, please determine ω_1 and ω_2, respectively.

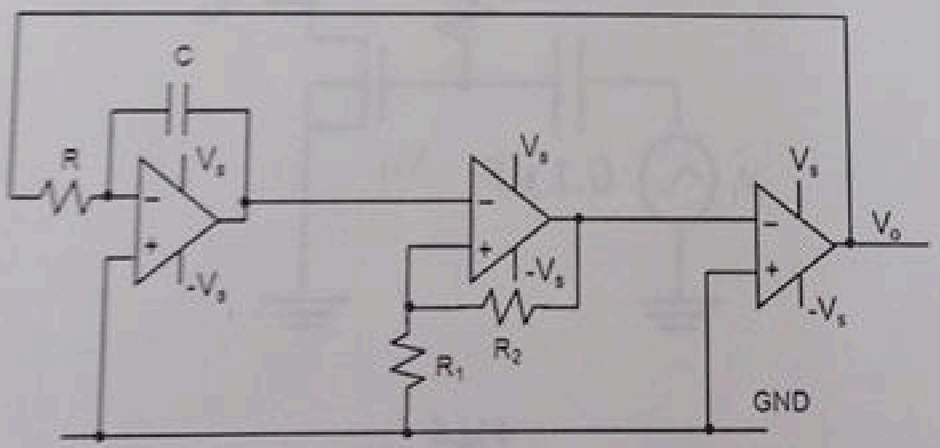
(b) (8%) Schematic of the state-variable filter is shown below. Assume the transfer function of $V_3(s)/V_i(s)$ is $F(s)$. Please derive $V_1(s)/V_i(s)$ and $V_2(s)/V_i(s)$ using $F(s)$. Also, if $F(s)$ is known as a low-pass filter, please determine the filter types for $V_1(s)/V_i(s)$ and $V_2(s)/V_i(s)$, respectively (you have to explain and get both $V_1(s)/V_i(s)$ and $V_2(s)/V_i(s)$ correct to receive credits).



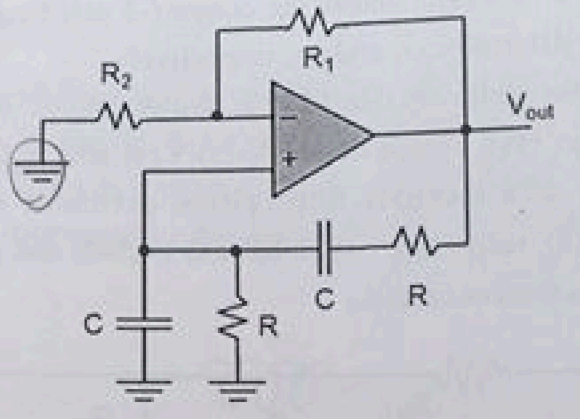
(c) (4%) Instrumentation amplifier has been used for ECG measurement in our lab. Please draw the schematic of an instrumentation amplifier with the output v_o related to the inputs (v_1 and v_2) by $v_o = v_1 - v_2$

5. Oscillator (20%)

(a) (10%) The following shows the schematic of the triangular, square-wave oscillator circuit used in our lab. Given that all resistor and capacitor values in the circuit are 1 kΩ and 1 μF, respectively, and the final output oscillates between ±20 V, please determine the output oscillation frequency.



(b) (10%) Please derive the condition for the Wien-bridge oscillator (as shown below) to start oscillation and determine the corresponding oscillation frequency.



6. Single-stage Amplifier (10%)

Consider the amplifier circuit in Fig.6. Let r_o and g_m represent the small-signal output resistance and transconductance, respectively, of the transistor. Assume $r_o = \infty$ (i.e. $\lambda = 0$, no channel length modulation) in the following questions.

(a) (6%) Assume the transistor is biased in saturation region. If we would like to increase the voltage gain of the amplifier, **how could each of the following items be adjusted individually** (increase or decrease)? (i) V_G (ii)V_{DD} (iii) R_D. Please **explain your answers** clearly. Note that some of the items above MAY NOT affect the voltage gain.

(b) (4%)Assume we take one of the actions you propose in (a). The gain does increase in the beginning, but if we continue to adjust (increase or decrease) a certain item too much, the gain stops increasing and starts to decrease instead. Would you explain why the gain become decreasing?

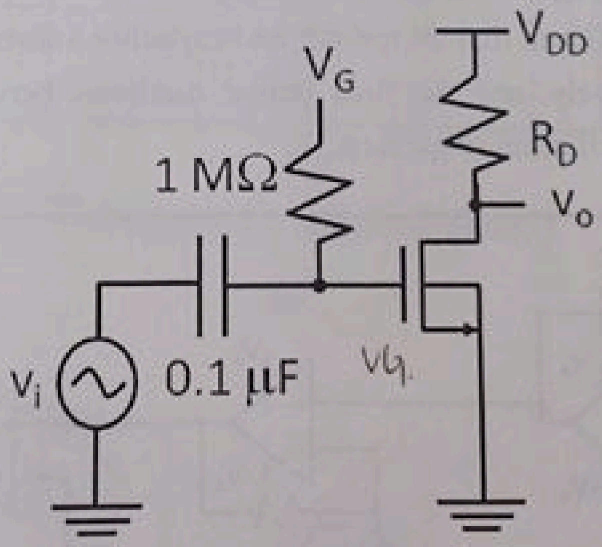


Fig.6

7. MOS Amplifiers (16%)

Consider the amplifier circuits in Fig.7. Let r_o and g_m represent the small-signal output resistance and transconductance, respectively, of **all transistors**. Assume r_o

∞ (i.e. $\lambda = 0$, no channel length modulation) in the following questions.

(a) (6%) Assume $1/g_m \gg R_{sig}$ in Fig. 7a, please derive the expression for the voltage gain V_O/V_i?

(b) (6%) If we would like to increase the voltage gain of the amplifier, **how could each of the following items be adjusted individually** (increase or decrease)? (i) V_G (ii) V_{DD} (iii) R_L. Please **explain your answers** clearly. Note that some of the items above MAY NOT affect the voltage gain.

(c) (4%) If V_i and R_{sig} in Fig.7a is replaced by a common-source amplifier, we obtain a cascade amplifier shown in Fig.7b. Let $R_L = R_D$. Would the voltage gain V_O/V_i of the cascade amplifier be larger than the voltage gain of the amplifier in Fig.7a? Please **explain your answers** clearly.

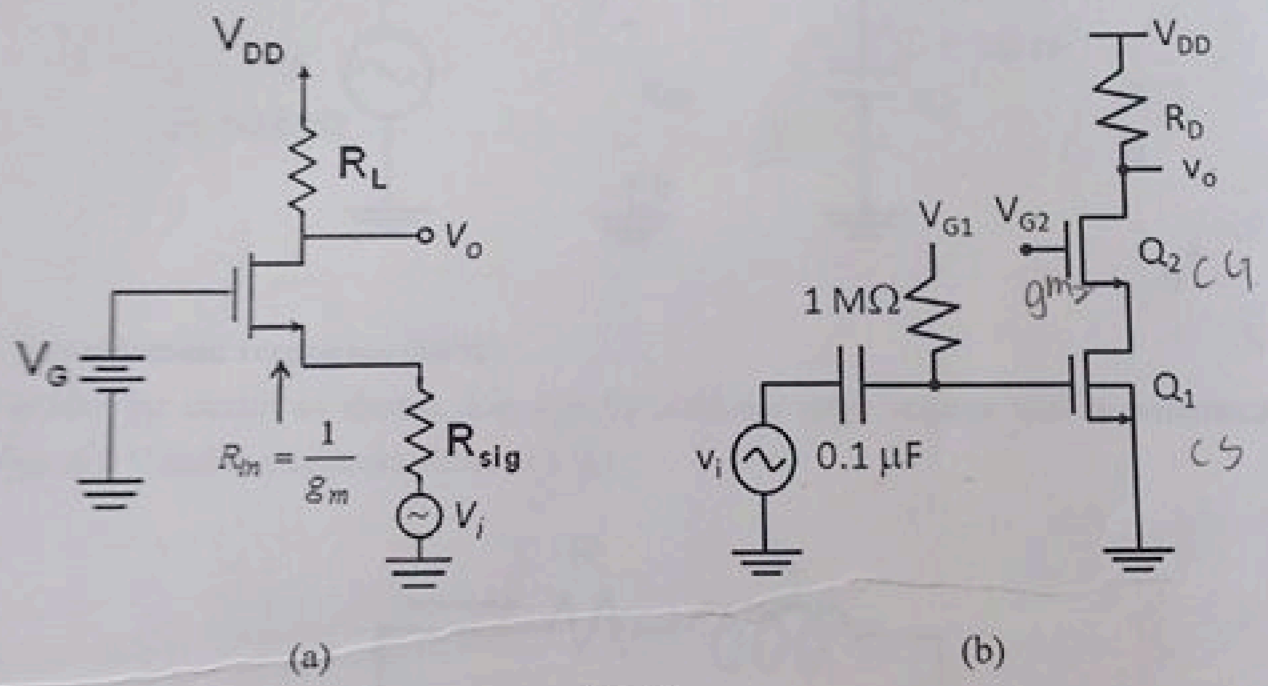
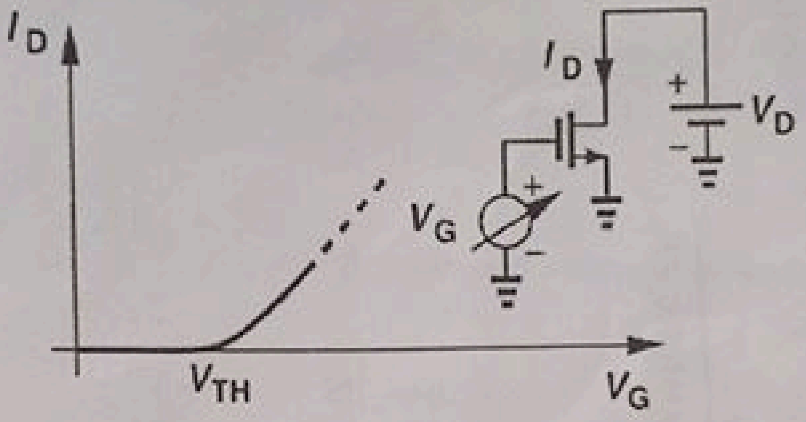


Fig.7



(b)

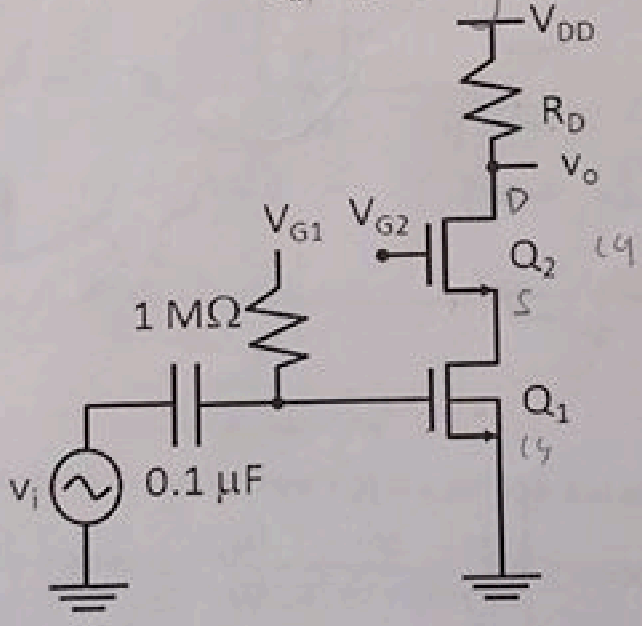
8. (16%) MOS Amplifier

Consider the MOS amplifier shown below.

(1) (8%) Assume that the total output resistance at V_O approximates R_D. If we would like to increase the voltage gain V_o/V_i, **how could each of the following items be adjusted individually?** (increase or decrease?) (i) V_{G1}; (ii) R_D. Assume that all transistors remain in saturation operation after the adjustment. Please **explain** your answer clearly. both decreasing

(2) (8%) If we find that Q2 operate in the triode (linear) region instead of the saturation region, **how could each of the following items be adjusted individually** (increase or decrease)? (i) V_{G1}; (ii) V_{G2}; (iii) R_D. Assume that Q1 remains in saturation operation after the adjustment. Please **explain** your answer clearly.

all decreasing



$V_{DS} > V_{GS} - V_{th} > 0$