EE 2245 Microelectronics Lab

Lab 7: Experiment: Single-Stage and Multi-Stage MOSFET Amplifiers

實驗室：_____組別 _____Names and ID Numbers: _____

Material, instrument and software

- CD4007UB MOSFET array × 1; VN0606 (power transistor); resistors and capacitors
- Power supply, function generator, oscilloscope, and digital multi-meter.
- HSPICE and Awaves

Procedure

In this lab, the CD4007UB MOSFET array is chosen to build various MOSFET amplifiers. This array consists of three N-MOSFETs and three P-MOSFETs. The definition of each pin is depicted in Fig. 1. Note that the body terminal in N-MOSFETs should always be connected to the most negative voltage, while those of P-MOSFETs should be connected to the most positive voltage. The CD4007 is a delicate device. M**ake sure you turn off the power supply before changing any circuit connections**. Use the model that you established in Lab 6 to design the amplifiers and compare with the measured results. Note: The VN0606 power transistor will be used for building the output stage of the audio amplifier.

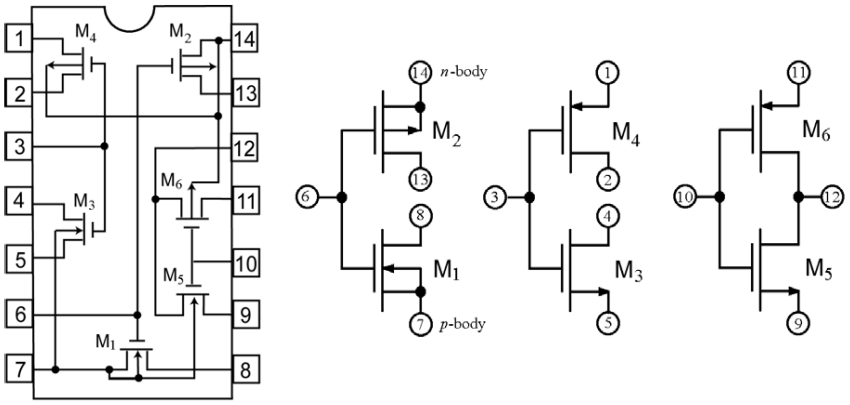

Fig. 1: The CD4007 MOSFET array.

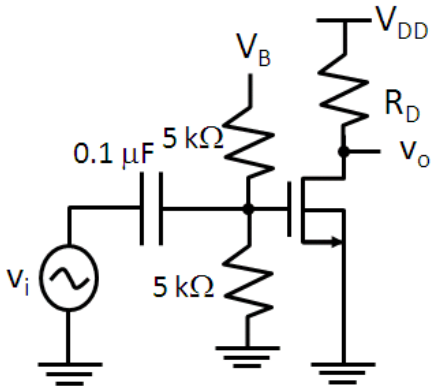

Fig. 2: The common-source amplifier.

Part I. Design and characterization of single-stage amplifiers

A. Design of a common-source amplifier

1. According to Fig. 2, please build a common-source amplifier on your breadboard with the power supply voltage and the gate voltage fixed at 5.0 V (the power supply has a fixed 5-V output) and 2.0 V, respectively (make sure that COM1 and COM2 are connected together). You should use the NMOS transistor without body effect (node 6-7-8). Please add bias resistors of 5 kΩ and a coupling capacitor of 0.1 μF to apply the input signal to the gate. With simple hand calculation, please determine the load resistor necessary to achieve a small-signal gain in the range between **15 dB to 20 dB** at the mid-band. Please explain your design process.
   $(v_o/v_i)_{calc.}$ = _____

   Based on your design, measure the drain current I_D (DC), the voltage across drain and source (DC), and the mid-band small-signal gain v_o/v_i. Compare the measured data with your analysis in the space provided below.

   Measured values: V_{GS} = _____ V; I_D = _____A; V_{DS} = _____V; v_o/v_i = _____
   Comment:

2. Perform HSPICE simulation based on the transistor parameters extracted in Lab 6. Compare the measured results (DC values and gain) with HSPICE simulation, and comment on what you observe.
   Comment:

3. Based on your design, measure the output swing under a few different input signal levels (v_i) and record these in the data sheet provided below. What is the maximum linear output swing of your design?

v_i (V_{pp})	v_o (V_{pp})

Maximum output swing (in terms of linear amplification): $v_{o,\text{peak-to-peak}}$ = _____ V

4. Plot the load line of your design together with the simulated I_D-V_{DS} curves obtained from Lab 6. Is your design optimized for maximum output swing? Please explain.
   If not, adjust the gate voltage to achieve the maximum output swing under the same load resistor. Also, measure the drain current I_D, the voltage across drain and source, and the mid-band small-signal gain v_o/v_i under the optimized V_{GS}. How does the gain change? Give a brief comment.

   Measured values: $V_{GS(optimal)}$ = _____ V; I_D = _____A; V_{DS} = _____V; v_o/v_i = _____
   Comment:

5. Add a source degeneration resistor of 1 kΩ in the CS amplifier. Adjust the gate voltage to achieve the same drain current as in Step 1. Measure the mid-band small-signal gain and maximum linear output swing. How does the gain compare to your hand calculation?

   $(v_o/v_i)_{measured}$= _____ ; $(v_o/v_i)_{calc.}$= _____; maximum output swing = _____ V
   Comment:

B. Design of a common-drain amplifier (source follower)

1. Design the common-drain amplifier with the transistor of nodes 6-7-8 to achieve a small-signal gain larger than 0.8 by selecting R_S, where R_S is connected to the source of the transistor directly (please refer to Fig. 3, but do not connect R_L and 0.1 μF for now). Set V_{DD}= 5.0 V and V_G= 3.0 V. Please explain your design process.

   Calculation: $(v_o/v_i)_{calc.}$= _____

   Measure the DC drain current I_D, the voltage across drain and source, and the mid-band small-signal gain v_o/v_i.

   Measured values: I_D = _____A; V_{DS} = _____V; v_o/v_i = _____

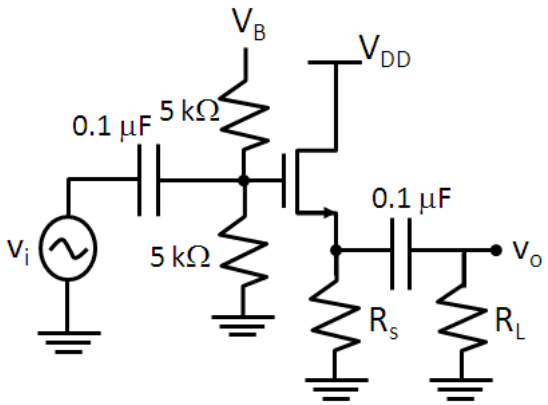

Fig. 3: Use different load resistors to test a CD amplifier.

2. Add an additional resistor R_L and a coupling capacitor 0.1 μF as shown in Fig. 3 for the CD amplifier design. Use R_L values of 1 KΩ and 10 KΩ, respectively, and measure the mid-band small-signal gain. This test is to investigate the effect of the load resistor on a CD amplifier. Compare the results under the two different loads. Also, compare the measured results with hand calculation. Comment on what you observe.

   $(v_o/v_i)_{measured,\ 1k\Omega}$ = _____; $(v_o/v_i)_{measured,\ 10k\Omega}$ = _____.

   $(v_o/v_i)_{calc.,\ 1k\Omega}$ = _____; $(v_o/v_i)_{calc.,\ 10k\Omega}$ = _____.

   Comment:

C. Design of a common-gate amplifier

1. Build a common-gate amplifier (Fig. 4) with the transistor without body effect (node 6-7-8) on your breadboard. Use the load resistor that you obtained in A-1 for the common-source amplifier. Apply a gate DC bias voltage of 2.0 V and V_{DD} of 5.0 V. Apply a small signal v_i at the source of the transistor and measure the mid-band small-signal gain v_o/v_i. Please also write down the previous common-source amplifier gain for comparison.

   $(v_o/v_i)_{measured,\ CG}$ = _____; $(v_o/v_i)_{measured,\ CS}$ = _____;

2. Perform hand calculation based on the transistor parameters extracted in Lab 6. Compare the measured results with hand calculation and comment on what you observe.

   $(v_o/v_i)_{calc.,\ CG}$ = _____;

Comment:

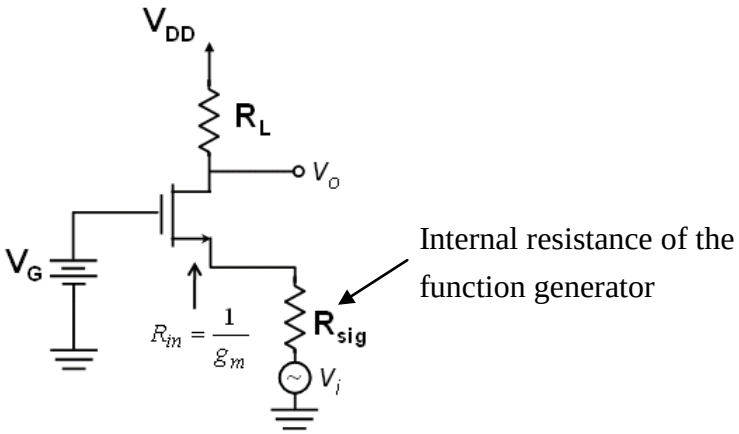

Fig. 4: Schematic of the common-gate amplifier.

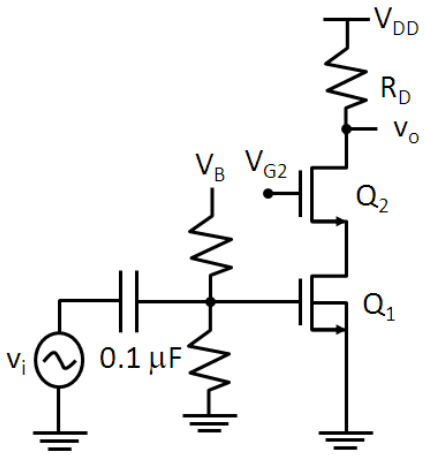

Fig. 5: The cascode amplifier.

D. Design of a cascode amplifier

1. Combine the common-source and common-gate stages to build a cascode amplifier (Fig. 5) on your breadboard. The gate bias of the CS stage is 2.0 V. Please adjust the gate bias of the CG stage to achieve the same DC current as that with the CS stage. The applied V_{DD} is 5 V and the load R_D is the same as that used in A-1. Measure the drain-source voltage drops for both stages. Make sure both transistors are in the saturation region. You can adjust V_{DD} if one of the transistors enters the linear region, but the drain current should be kept the same.

$V_{DS,\,Q1}$ = _____ V; $V_{DS,\,Q2}$ = _____ V;

2. Measure the mid-band small-signal gain of the amplifier and compare that with the value by hand calculation. Give a brief comment on what you observe.
Comment:

Part II. Mini Project

1. You are required to build a speaker driving circuit using a cascade three-stage common-source amplifier as shown in Fig. 6(b). You will have to use the CD4007UB MOSFET array and the power transistor VN0606 to build the first two stages and the output stage, respectively. The first two-stage amplifier is shown in Fig. 6(a). Based on the experience obtained in Part I, please design the bias point of M1 through R_{G1} and R_{G2}, and design the load resistors R_{D1} and R_{D2} to have a combined gain of at least 50 (V/V) for the first two stages. Set the power supply voltage to 5.0 V. Perform hand calculation and compare with the measured results. Check if the upper -3dB frequency is larger than 20 kHz.

Gain of the first two stages: Measured = _____; calculated = _____.

Comment:

2. You are advised to extract the VN0606 transistor model (e.g. threshold voltage) by *i*-*v* measurements as performed in Lab 6, in order to design the last stage of the speaker driving circuit as shown in Fig. 6(b). The complete circuit has to achieve a total gain of at least 25. Describe your design process below.

For demonstration, you need to apply an input signal of 20 mV (amplitude), from a functional generator, with increasing frequencies from 500 Hz to 20 kHz. The sound from the speaker should be heard by the TA.

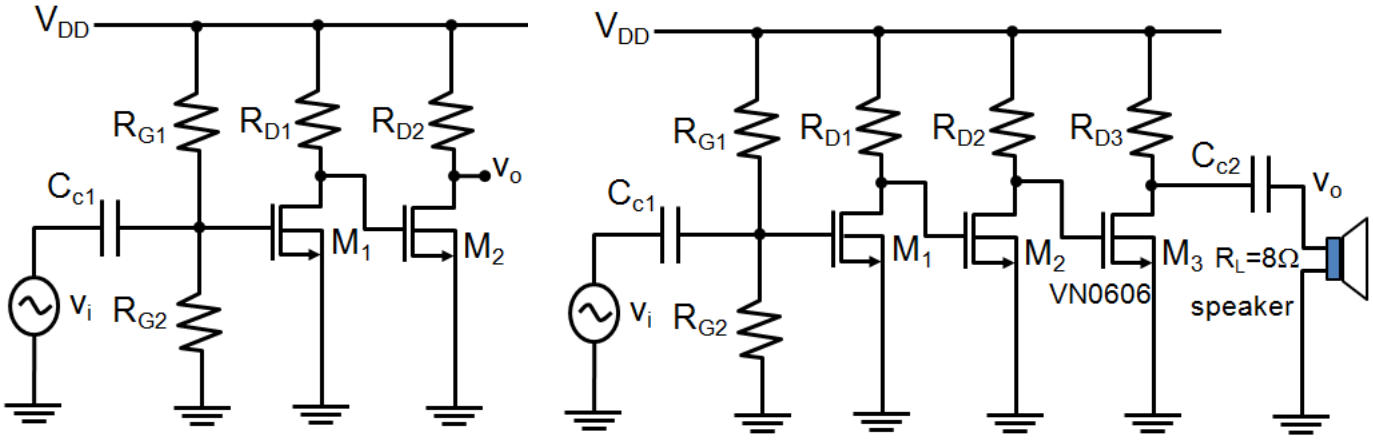

Fig. 6: (a) A cascade two-stage CS amplifier. (b) The complete speaker driving circuit.

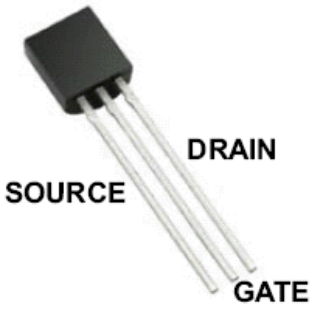

Fig. 7: The VN0606 chip.