Introduction to HSPICE

- **What's SPICE?**
  - **Simulation Program with Integrated Circuit Emphasis**
- **Netlist (.sp) syntax and writing**
  - **Basic architecture**
  - **Simulation environment setup**
  - **Components and source**
  - **Performing analysis**
  - **Output specify**
- **Star-HSpice environment orientation**
  - **Hspui user interface**
  - **AvanWaves graph interface**

HSPICE Notice

- In Hspice, there's no difference between uppercase and lowercase.
- There's no priority between lines and lines.
- Types of components and sources are defined by the first letter.
- Chinese characters in the directory of .sp files and library files are forbidden.
- Check out ' **job concluded** ' in the .lis file to ensure simulation is finished.

Simulation Environment Setup

- **1st line is the title. Hspice will neglect it in simulation.**
- **.LIB: Library files can be included for model statements.**

  ex .lib ' mm0355v.l ' TT
- **.MODEL: Create a new model with parameters provided.**

  .MODEL <name> <type> <version=# or level=#>
  + <parameter name1=# parameter name2=# …>

  ex .model nch NMOS level=1
  + vto=vt kp=163.1u lambda=0.0041
- **.PARAM: Declare a new variable with initial value.**

  ex .param vt=1.232574
- **.Alter: Alter condition and repeat analysis.**
- **.Probe: Probe pin names & types to get values or wave-forms.**

  .PROBE <DC/AC/TRAN> <ov1> <ov2> <ov3> …
- **.END: End of the file. (must appear in the last line of file)**

Components & Sources

- **Components:**

Resistor
Rxxx node1 node2 (R=)<value>

Capacitance
Cxxx node1 node2 (C=)<value>

MOSFET
Mxxx **<D>** **<G>** **<S>** **<B>** <model>
+(L=)<value> (W=)<value> (m=)<value>

Head characters	Devices represented
C	Capacitor
D	Diode
J	JFET
K	Mutual inductor
L	Inductor
M	MOSFET
Q	BJT
R	Resistor
T,U,W	Transmission line
X	Subcircuit

- **Sources:**

Voltage source
Vxxx node+ node- (DC=)<value>
+ (AC=)<magnitude> <phase>

Current source
Ixxx node+ node- (DC=)<value>
+ (AC=)<magnitude> <phase>

Performing Analysis

- **.OP: Analyze operation point of nodes in circuit.**

  Syntax. .OP

- **.DC: DC analysis to sweep parameter, source and temperature values.**

  Syntax. .DC <var1> <start> <stop> <step>
  ex .DC Vin 0 3.3 0.1

- **.AC: AC analysis to sweep frequency.**

  Syntax. .AC <DEC/LIN> <Number of points> <start> <stop>
  ex .AC DEC 10 10 10x

- **.Tran: Transient analysis to sweep time.**

  Syntax. .Tran <step> <start> <stop>
  ex .Tran 100n 1u 10u

- **.TF: Small signal analysis and dc gain, input/output resistance**

  Syntax. .TF type<node> <Voltage/Current Source>

Components & Sources

- **Input line format :**
  - **Upper and lower case are ignored, except in quoted filenames.**
  - **Names:**
    - Names must begin with an alphabetic character.
  - **Delimiters:**
    - Tab, blank, comma, equal sign (=), and parentheses“( )”.
  - **Nodes:**
    - Leading zeros are ignored in node numbers.
    - Trailing alphabetic characters are ignored in node numbers.
    - Can be any natural number, but **node 0 is GND.**
  - **Numbers:** **=GND!**
    - Numbers can use exponential format or engineering key letter format, but not both (1e-12 or 1p, but not 1e-6u).

Code		Meaning
1t	1E+12	10^{12}
1g	1E+09	10^{9}
1x/1meg	1E+6	10^{6}
1k	1E+3	10^{3}
1m	1E-3	10^{-3}
1u	1E-6	10^{-6}
1n	1E-9	10^{-9}
1p	1E-12	10^{-12}
1f	1E-15	10^{-15}

Output Specify

- **Output Variable Syntax:**

DC Analysis Output Variable		
Type	**Output Variable Syntax**	**Meaning**
Voltage	V(N)	Voltage at Node N
	V(N1,N2)	Voltage difference between N1 and N2
	VX(D)	Voltage at Node X in Device D
	V(D:X)	Voltage at Node X in Device D
Current	I(D)	Current through Device D
	IX(D)	Current into Node X in Device D
Parameter	par(PAR)	Parameter PAR
	par('Expression')	Parameter described by Expression
AC Analysis Output Variable		
Type	**Output Variable Syntax**	**Meaning**
Voltage	V(N)	Magnitude of voltage at Node N
	VM(N)	Magnitude of voltage at Node N
	VR(N)	Real part of voltage at Node N
	VI(N)	Imaginary part of voltage at Node N
	VP(N)	Phase of voltage at Node N
	VdB(N)	Magnitude of voltage at Node N in dB

Output Specify

- **Output Variable Syntax: (cont'd)**

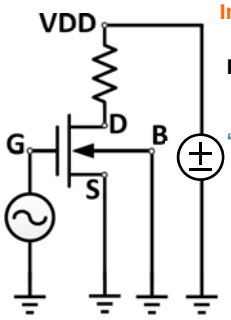
AC Analysis Output Variable (cont'd)		
Type	**Output Variable Syntax**	**Meaning**
Current	I(D)	Magnitude of current through Device D
	IM(D)	Magnitude of current through Device D
	IR(D)	Real part of current through Device D
	II(D)	Imaginary part of current through Device D
	IP(D)	Phase of current through Device D
	IdB(D)	Magnitude of current through Device D in dB
	IMX(D)	Magnitude of current at Node X in Device D
	IRX(D)	Real part of current at Node X in Device D
	IIX(D)	Imaginary part of current at Node X in Device D
	IPX(D)	Phase of current at Node X in Device D
	IdBX(D)	Magnitude of current at Node X in Device D in dB
Parameter	par(PAR)	Parameter PAR
	par('Expression')	Parameter described by Expression

*Node X in Devices:

MOSFET: 1:D 2:G 3:S 4:B

BJT: 1:C 2:B 3:E

Basic Architecture



Environment Setup

Included filename

Parameter Setup

"nch" parameter

Components

Voltage Source

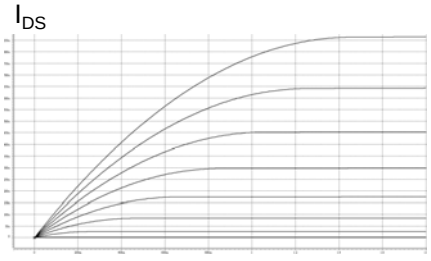
Performing Analysis

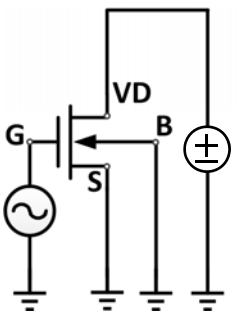
Alter Parameter

```
********* EXAMPLE_AC *********
.option  post  acout=0  accurate        精確度設定
.option  post  probe
.option  dccap=1  CAPTAB                列出節點電容值
.include 'mos.sp' (製程廠提供的元件參數)
.param  vt=1.232574     k=163.1853u  lbd=0.004127
+       cgdo=0.5u       cbd=10p      pb=0.8
+       rl=20k
.model  nch     NMOS   level=1
+       vto=vt          kp=k         lambda=lbd
+       cgso=cgdo       cgdo=cgdo    cbd=cbd
+       cbs=cbd         pb=pb
Mn      D      G     0     B    nch  W=30u  L=0.5u
RL      VDD    D     rl
VGS     G      0     dc  3   ac  1
VBS     B      0     dc  0
.ac     dec    10    10  10x
.probe  ac  vdb(D)
.alter
.param vt=0.8
.end
```

This example is only for lecture

Example

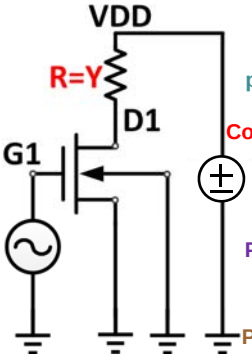




DC Sweep

```
********* EXAMPLE_DC_SWEEP *********
.option  post  acout=0  accurate
.option  post  probe
.option  dccap=1  CAPTAB
.param  vt=0.35     k=163.1853u     lbd=0.004127
+       cgdo=0.5u       cbd=10p      pb=0.8
.model  nch     NMOS   level=1
+       vto=vt          kp=k         lambda=lbd
+       cgso=cgdo       cgdo=cgdo    cbd=cbd
+       cbs=cbd   pb=pb
M1      D      G     0     B     nch    W=1.0u   L=0.2u
VDS     D      0     dc    1.8
VGS     G      0     dc    1
VBS     B      0     dc    0
.op
.dc     VDS  0  1.8   0.01   sweep   VGS   0  1.8  0.2
.print  i(m1)

.end
```

Example: A NMOS with a Varying Load




```
**************** NMOS **********
.option  post  acout=0  accurate
.option  post  probe
.param   Vt=0.68      k=156.8u     lam=0.0098
+        toxn=100n    cbd0=2p      cgso=0.1p      pb=0.8
.model   nch    NMOS   level=1
+        vto=vt              kp=k              lambda=lam
+        tox=toxn            cgdo=cgdo         pb=pb
+        cbd=cbd0            cbs=cbd0
M1       D1     G1     GND    GND    nch    W=30u    L=5u
R1       D1     VDD    Y
VDD1     VDD    GND    dc     3.3
VIN1     G1     GND    dc     1
.DC      VIN1   0      3.3    0.01   sweep  Y   1k   10k   2k
.print   V( D1 )     I(M1)
.alter
M1       D1     G1     GND    GND    nch    W=60u    L=5u
*M1      D1     GND    GND    nch    W=30u    L=10u
.end
```

Environment

Parameter

"nch" parameter

Components

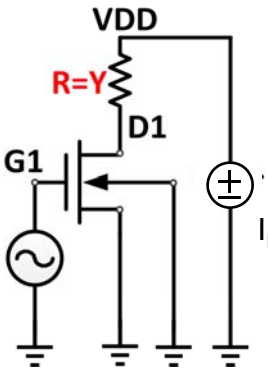
Voltage Source

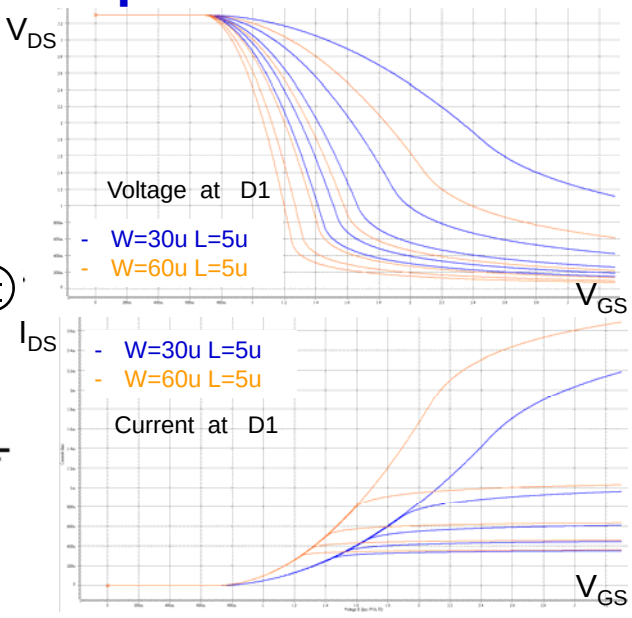
Performing Analysis

Alter Parameter

" * " For temporarily disabled

Output Result





Performing Analysis

- **SWEEP: Additional nested sweep analysis. Sweep parameter, source or temperature values but not model parameters.**
- Syntax.

  <Analysis> SWEEP <var> <start> <stop> <step>
  or <Analysis> SWEEP <var> <DEC/LIN> <number of points> <start> <stop>

- **.MEASURE: Use the .MEASURE statement to modify information and define the results of successive simulations.**
- Syntax.

  .measure <type> <measure_name> find <function> when <function>
  .measure <type> <measure_name> find <function> at <function>
  .measure <type> <measure_name> max/min <parameter>
  .measure <type> <measure_name> param = ' function '

- **.PRINT: Print voltage, current or parameter values in .lis file.**
- Syntax.

  .PRINT <DC/AC/TRAN> <ov1> <ov2> <ov3> / <function>…

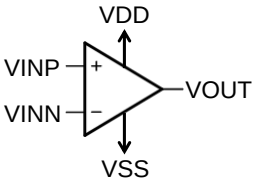
Appendix: AC Simulation

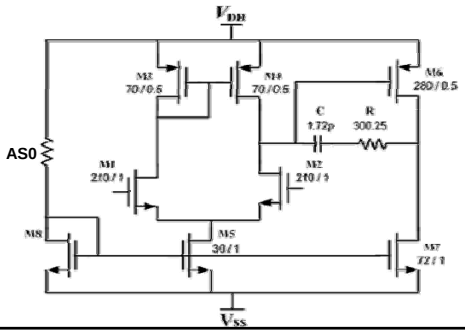
File name : Two_stage_op.spi

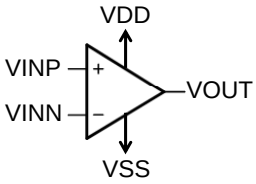
.SUBCKT AMP VINP VINN VOUT VDD VSS

M1	M1_D	VINN	M5_D	VSS	nch	w=15u	l=1u	m=14
M2	M2_D	VINP	M5_D	VSS	nch	w=15u	l=1u	m=14
M3	M1_D	M1_D	VDD	VDD	pch	w=14u	l=0.5u	m=5
M4	M2_D	M1_D	VDD	VDD	pch	w=14u	l=0.5u	m=5
M5	M5_D	AS0	VSS	VSS	nch	w=5u	l=1u	m=6
M6	VOUT	M2_D	VDD	VDD	pch	w=14u	l=0.5u	m=20
M7	VOUT	AS0	VSS	VSS	nch	w=12u	l=1u	m=6
M8	AS0	AS0	VSS	VSS	nch	w=1u	l=1u	m=1
RC	M2_D	2	300.25					
CC	2	VOUT	1.71906p					
R_AS0	VDD	AS0	116k					

.ENDS

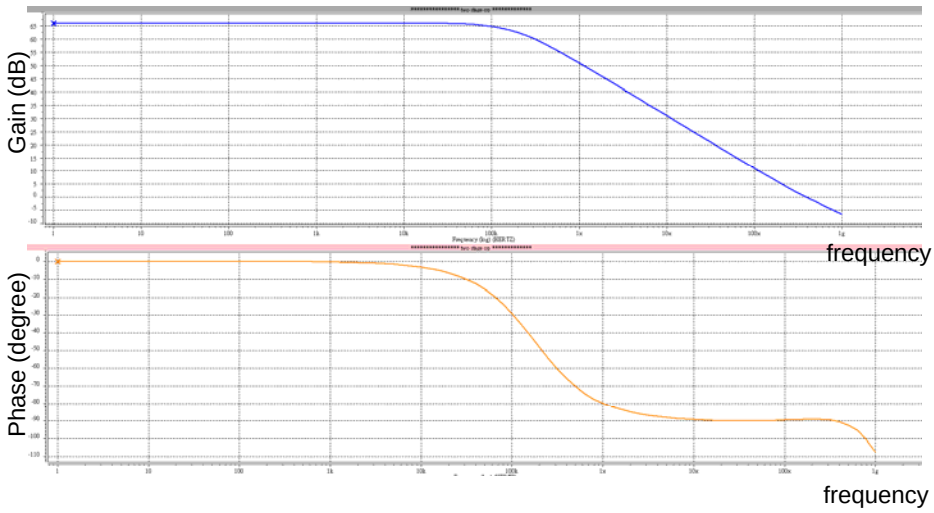






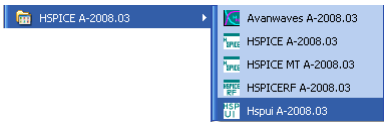
File name : Testbench.sp

```
**************  TWO STAGE OP  *************
.protect
.lib ' mm0355v.l '  TT
.unprotect
.include ' Two_stage_op.spi '
.option  post  acout=0  accurate
.option  post  probe
.option  dccap=1  CAPTAB
xOP1   INP   INN    OUT   VDD   VSS    AMP
VDD   VDD  GND   dc  1.65
VSS   VSS  GND   dc  -1.65
VINP  INP   GND   dc    0   ac   0.5   0
VINN  INN   GND   dc    0   ac   0.5   180
.ac     dec    10     1    1G
.print   ac   vdb( out )   vp( out )
.meas  ac   dcgain_in_db   max    vdb( out )
.meas  ac   dcgain            max     vm( out )
.meas  ac   f_3db  when  vdb( out ) = ' dcgain_in_db - 3.0 '
.meas  ac   unity_frequency   when   vdb( out ) = 0
.meas  ac   phase   find   vp( out )   at = unity_frequency
.meas  ac   phase_margin   param = ' 180+phase '
.tf   v(out)  vinp
.END
```

dcgain_in_db	= 66.05dB	dcgain	= 200.69 v/v
f_3db	= 178.99kHz	unity_frequency	= 391.13MHz
phase	= -90.524°	phase_margin	= 89.476°

Hspui User Interface

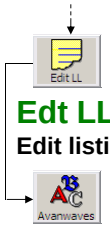


Click!

Open: Open netlist files (.sp)

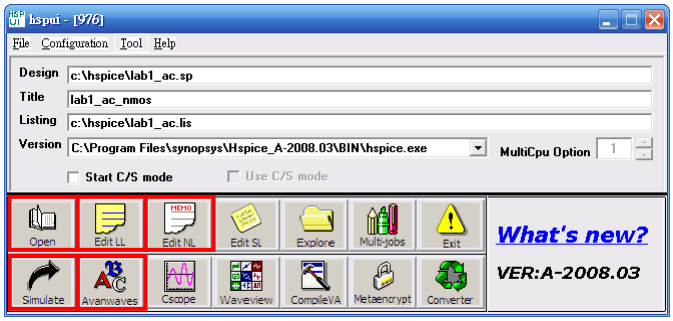
Edt NL: Edit netlest files (.sp)

Simulate: Run HSpice



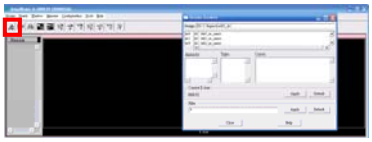
Edt LL:
Edit listing files (.lis)

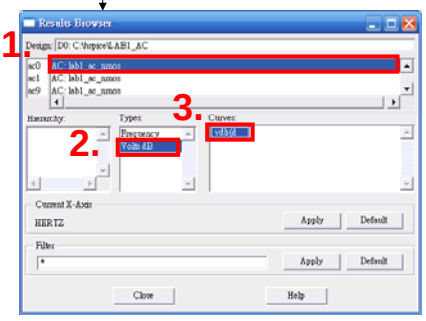
Avanwaves:
Edit listing files (.lis)

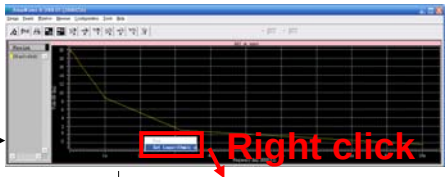


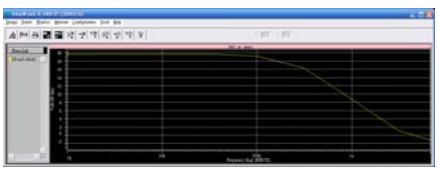
Check Result: AvanWaves Graph Interface

Click!





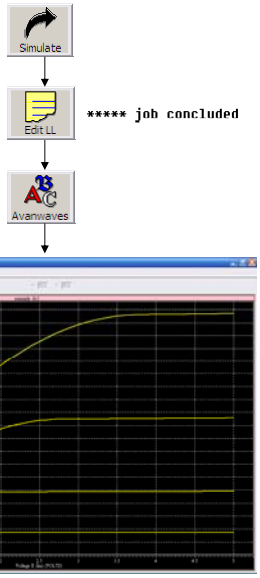




Example

- **Example_DC1:** I_D-V_{DS} curve sweep V_{GS}

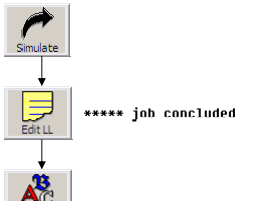
```
Example_DC1
.OPTION POSET=2 PROBE
.LIB '.\NOTHING.l' TT
.INCLUDE '.\EMPTY.sp'
.PARAM  vt=1.232574     k=163.1853u
+       lbd=0.004127    cgdo=0.5u
+       cbd=10p         pb=0.8
.MODEL  nch     NMOS    level=1
+       vto=vt  kp=k    lambda=lbd
+       cgso=cgdo       cgdo=cgdo
+       cbd=cbd cbs=cbd pb=pb

Mn      d       g       gnd     gnd     nch W=30u L=10u

Vd      d       gnd     DC=5V
Vg      g       gnd     DC=2V   AC=1V

.DC     Vd 0 5 0.1      SWEEP Vg 2 5 1
.PROBE  DC ID(Mn)

.END
```

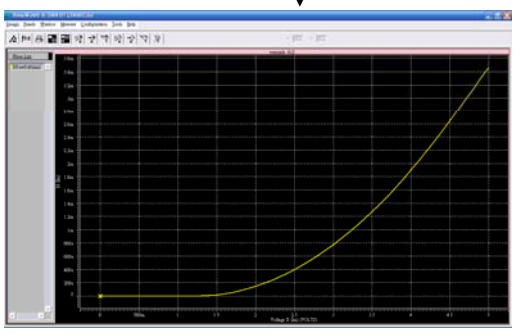


Example

- **Example_DC2:** I_D-V_{GS} curve

```
Example_DC2
.OPTION POSET=2 PROBE
.LIB '.\NOTHING.l' TT
.INCLUDE '.\EMPTY.sp'
.PARAM  vt=1.232574     k=163.1853u
+       lbd=0.004127    cgdo=0.5u
+       cbd=10p         pb=0.8
.MODEL  nch     NMOS    level=1
+       vto=vt  kp=k    lambda=lbd
+       cgso=cgdo       cgdo=cgdo
+       cbd=cbd cbs=cbd pb=pb

Mn      d       g       gnd     gnd     nch W=30u L=10u

Vd      d       gnd     DC=3.3V
Vg      g       gnd     DC=2V   AC=1V

.DC     Vg 0 5 0.1
.PROBE  DC ID(Mn)

.END
```





Star-HSpice Environment Orientation

- **After setup software, before simulation:**
  Create a working folder! CAUTION: No Chinese in directory.
  Ex. C:\lab1\lab1.sp (O)
  C:\Documents and Settings\Administrator\桌面\lab1.sp (X)

Ouput File Type	Extension
Output listing	.lis
Transient analysis results	.tr#
DC analysis results	.sw#
AC analysis results	.ac#
Transient analysis measurement results	.mt#
DC analysis measurement results	.ms#
AC analysis measurement results	.ma#
FFT analysis graph data files	.ft#
Output status files	.st#
Nets operation voltages	.ic#

Hspice manual http://0rz.tw/OCScF