EE 2245 Microelectronics Labs

Lab 4: Active Filter Design (4 weeks)

實驗室：_____組別 _____Names and ID Numbers: _____

Design Problem I:

You are required to implement a biquad band-pass filter shown in Fig. 1 with the following specifications:

(1) Band-pass frequency = 8 kHz (with a tolerance less than ±2%); Note: Band-pass frequency is the frequency where $|v_{BP}(j\omega)/ v_i(j\omega)|$ has the maximum value.

(2) Quality factor ≥ 8

Note:

(1) **Please show your analysis, including the input-output relationship of $v_{BP}(s)/v_i(s)$, the band-pass frequency, and the quality factor, to a teaching assistant before implementing the circuit.**

Hint: You can start with the KCL analysis at the "-" node of the 1st op amp.

(2) Demonstrate your result to a TA or teacher.

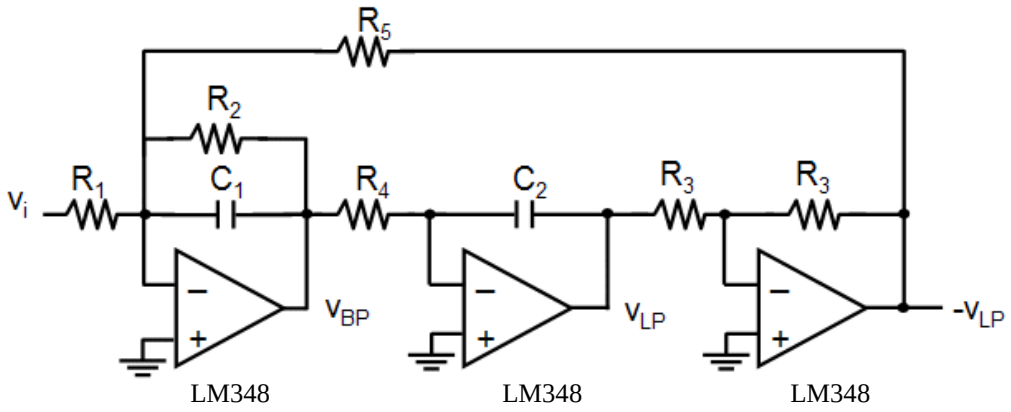

Figure 1: Schematic of the biquad filter. Note: the LM348 op-amps are biased at ±18 V.

For your implementation, please use resistor values in the range of 2 kΩ ≤ R_i ≤ 500 kΩ, and use C_1 = 1 nF. The amplitude of the input voltage should be kept at a proper value to get enough output signals at low frequencies and avoid saturation of the high-Q circuit at the band-pass frequency.

In the report, you need to provide:

(1) Analysis of the band-pass filter, including the input-output relationship, the band-pass frequency, and the quality factor.

(2) Design process regarding to how you select the values of passive elements.

(3) Measured frequency response (gain vs. frequency).

Design Problem II:

請注意：Design Problems II, III, and IV 所用的 op-amp 與 Design Problem I 不同。Problem IV 將整合 II、 III 部份進行 ECG 量測，以下電路量完不要馬上拆。

You are required to implement an active high-pass filter shown in Fig. 2 with the following specifications:

(1) High-pass corner frequency = 1 Hz (i.e. Design both poles of the filter to locate at 1Hz);

(2) Flat-band voltage gain = 100 (V/V) (maximum tolerable gain error = ±10%);

(3) Input impedance ≥ 1 MΩ at 1 Hz.

Note:

(1) **Please show your analysis, including the input-output relationship of $v_{HP}(s)/v_i(s)$, the pole frequency, the flat-band voltage gain, and the input impedance to a teaching assistant before implementing the circuit.**

(2) **Demonstrate your result to a TA or teacher.**

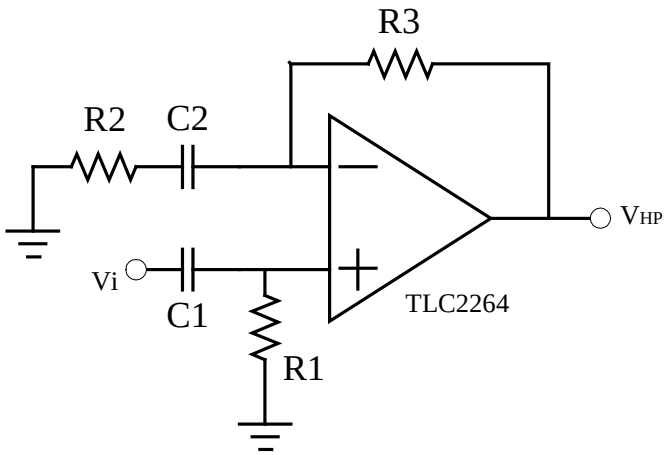

Figure 2: Schematic of the high-pass filter. Note: the TLC2264 op-amps are biased at ±8 V.

In the report, you need to provide:

(1) Analysis of the high-pass filter, including the input-output relationship, the pole frequency, the flat-band voltage gain, and the input impedance.

(2) Complete design process (how do you select the passive elements).

(3) Measured frequency response (Gain vs. frequency). The gain at 0.1 Hz, 1 Hz, and 10Hz must be measured.

(4) Does the measured gain response agree with your analysis by satisfying the following three conditions? (i) The flat-band voltage gain is 40 dB (with ±10% tolerance) at 10 Hz. (ii) The gain reduces by about 5 dB at 1 Hz. (iii) The gain is smaller than 5 dB at 0.1 Hz. If any of the conditions is not satisfied, please discuss the reasons based on the derived input-output relationship and the real values of resistors and capacitors in your experiment.

Design Problem III:

You are required to implement the Sallen-Key low-pass filter shown in Fig. 3 with the following specifications:

(1) The natural frequency 20 Hz ≤ f_n ≤ 60Hz (note: $\omega_n = 2\pi f_n$)

(2) Flat-band voltage gain ≥ 3 (V/V);

(3) R1 ≥ 10 kΩ

Note:

(1) **Please show your analysis, including the input-output relationship of $v_{LP}(s)/v_i(s)$, the natural frequency, the flat-band voltage gain to a teaching assistant before implementing the circuit.**

(2) **Demonstrate your result to a TA or teacher.**

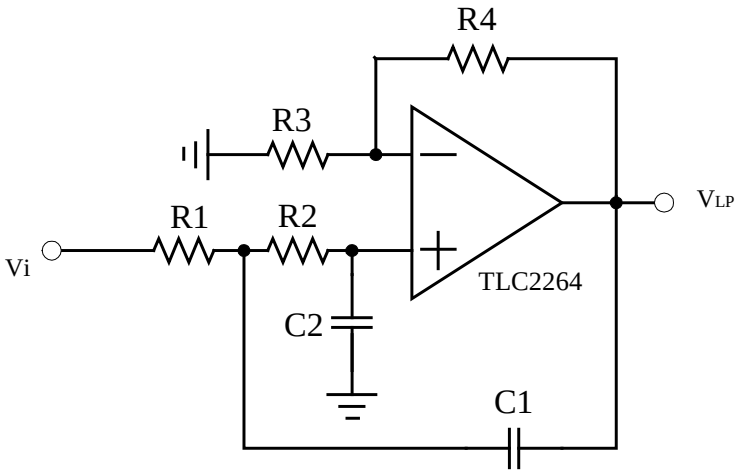

Figure 3: The Sallen-Key low-pass filter.

In the report, you need to provide:

(1) Analysis of the low-pass filter, including the input-output relationship, the natural frequency, and the flat-band voltage gain.

(2) Complete design process (how do you select the passive elements).

(3)Apply a 100-mV sinusoidal signal at the designed natural frequency (f_n) to the input V_i, measure the phase difference between V_i and $V_{LP.}$ Is the phase difference equal to 90°?

(4) Measured frequency response (Gain vs. frequency). The gain at 1 Hz, 10 Hz, your designed natural frequency, 60 Hz, and 100 Hz must be measured.

(5) Does the measured gain response agree with your analysis? If not, please discuss the reasons.

Design Problem IV:

In this task, you are going to integrate the filters designed in problem II and III to form an amplifier capable of recording electrocardiograms (ECGs), as shown by Fig. 4. An instrumentation amplifier (INA) is added at the front end to remove common-mode interferences. Fig. 5 shows the circuit diagram of INA, where the external R_G determines the voltage gain.

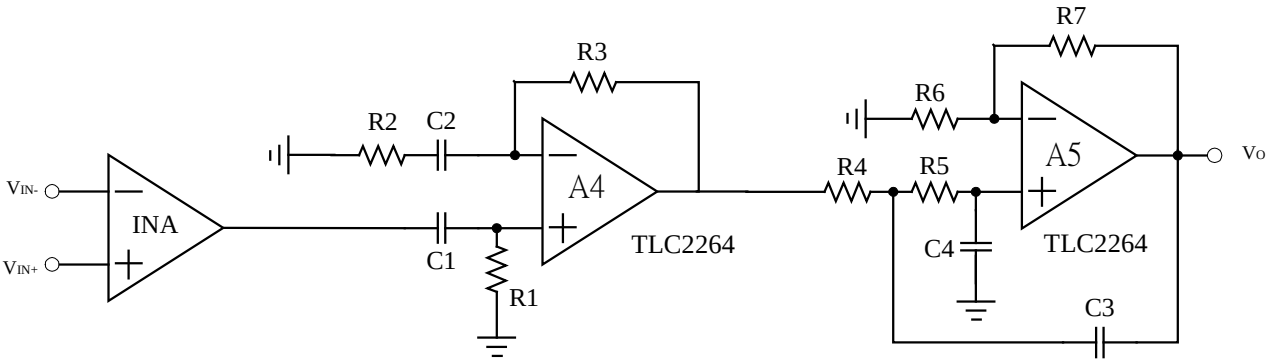

Figure 4: The complete circuit for recording ECG.

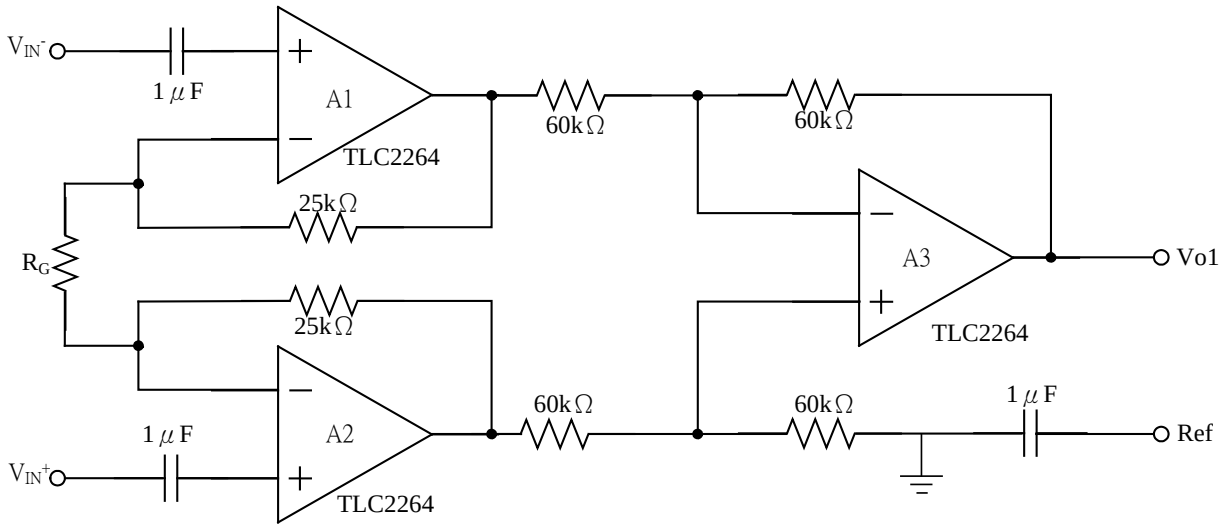

Figure 5: The circuit diagram of the instrumentation amplifier.

Experiments :

(1) Design R_G to achieve a voltage gain greater than 6 (V/V) for the circuit in Fig. 5. Apply a 10-mV, 10-Hz sinusoidal signal across the differential input (V_{IN}^+, V_{IN}^-). Measure the corresponding output at V_{O1} and answer the following questions.

(a) How much is the voltage gain V_{O1} / (V_{IN}^+ - V_{IN}^-)?

(b) Does the output signal contain any DC offset?

If yes, please discuss the main amplifier(s)(A1-A5) that contribute the DC offset at the output.

(2) Connect the input to wet electrodes and measure your own electrocardiograms as Fig.6. Does the output contain DC offsets or interference? Please answer the following questions

(a)What is the main frequency component of the interference?

(b)How could we reduce the interference?

You must demonstrate your measured ECG signals before leaving the lab.

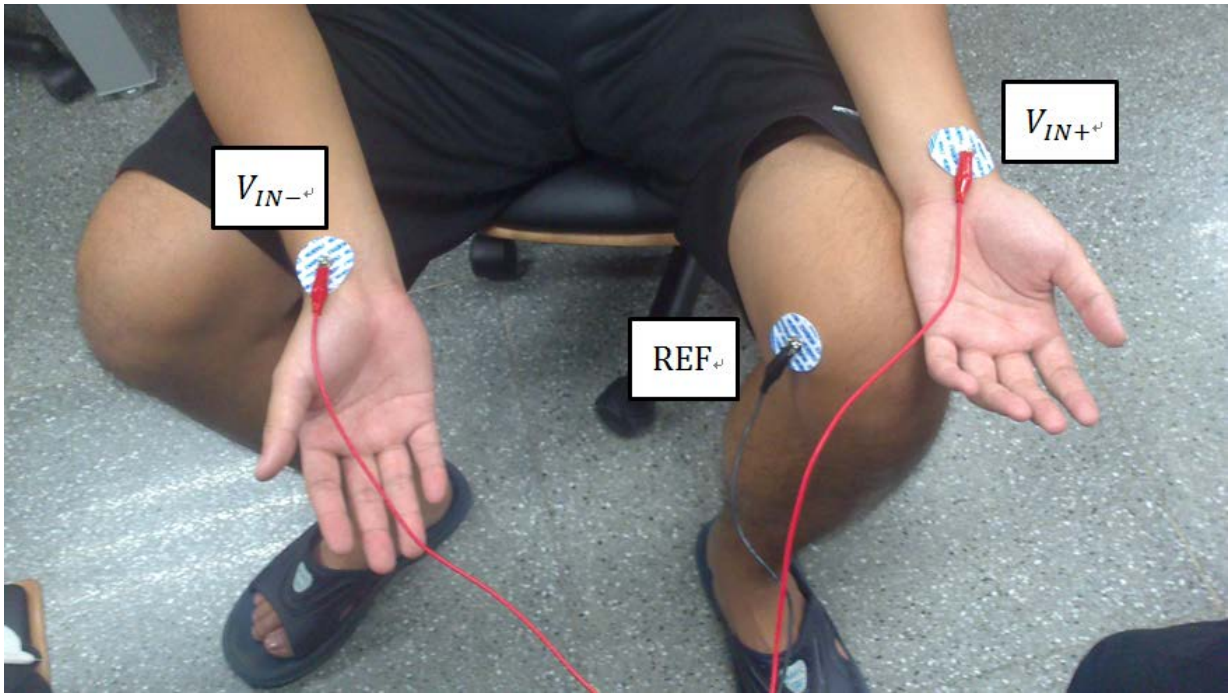

Figure 6: Illustration of ECG measurement.