Lab 6: Parameter Extraction in SPICE MOSFET Model

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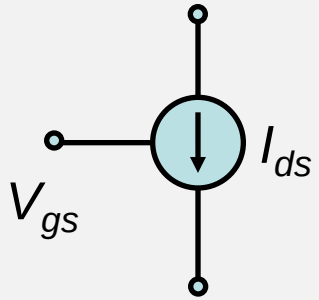
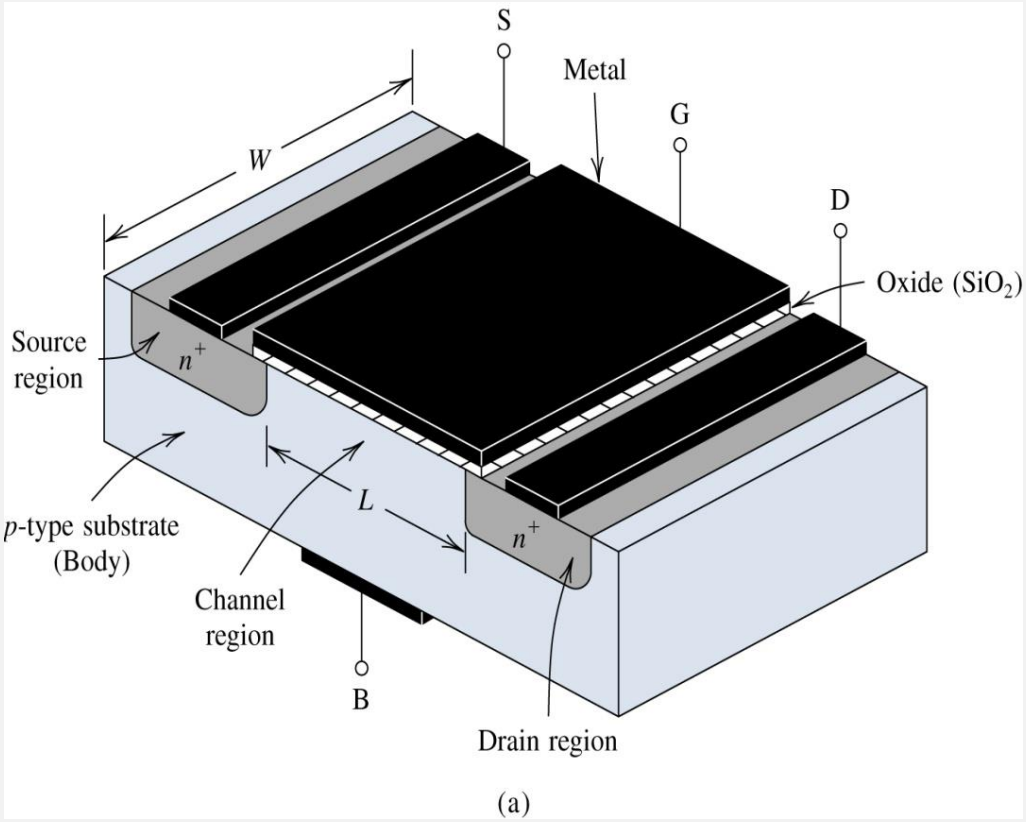
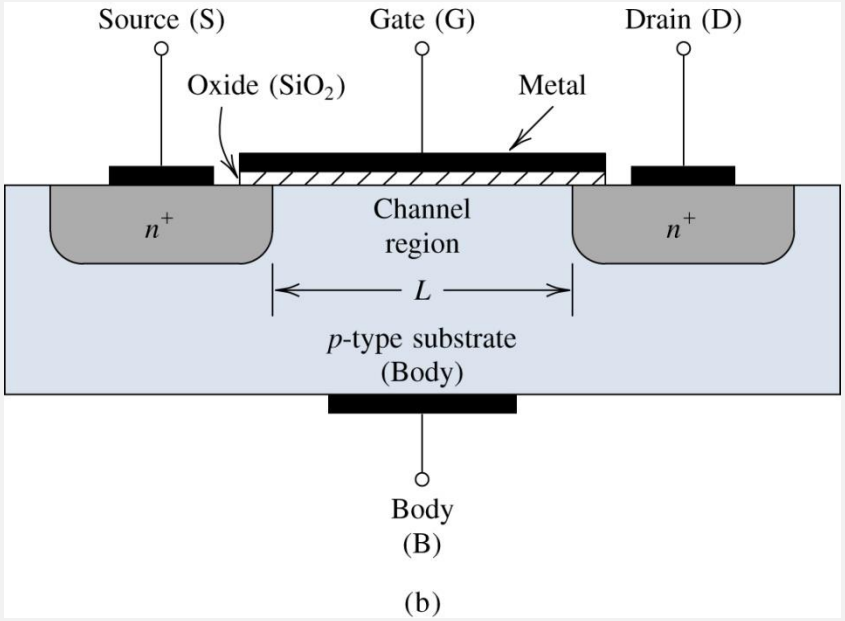
Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

A voltage-controlled current source

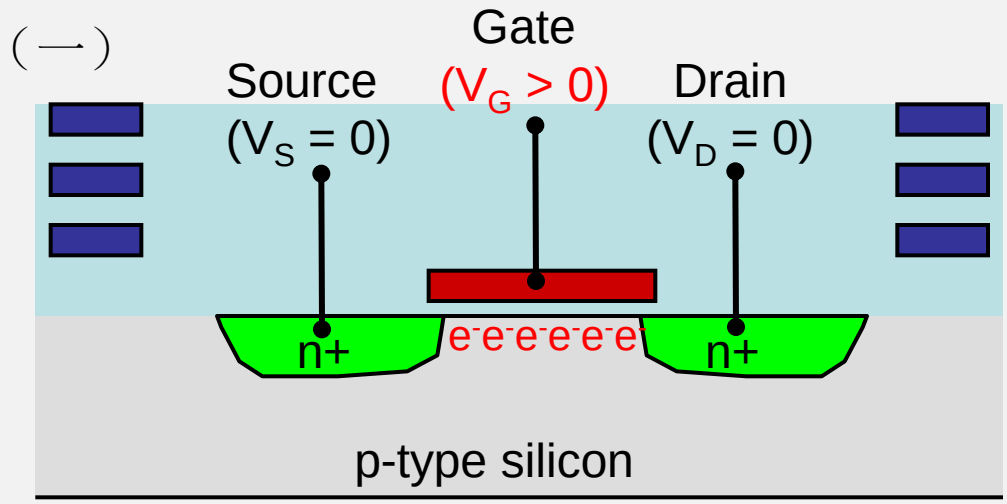




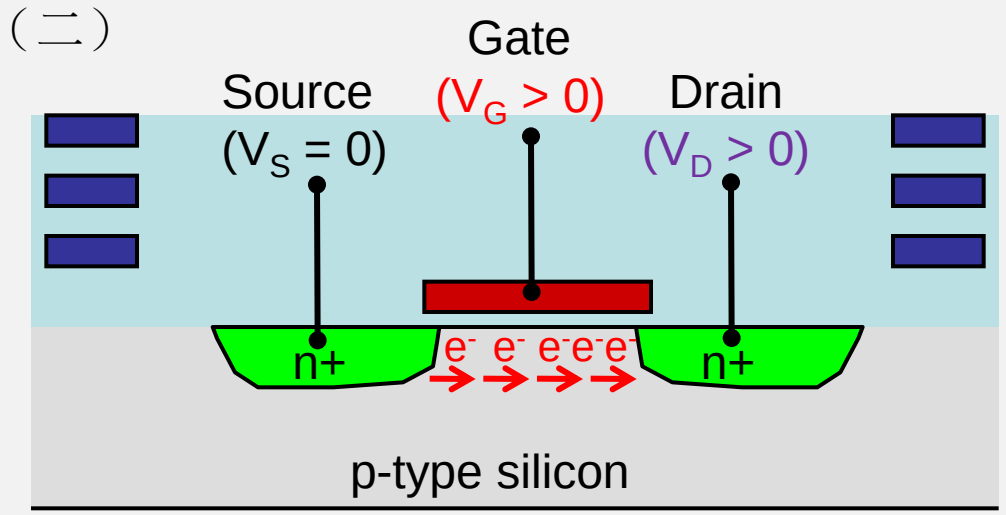


Example: Operation of a N-type MOS Transistor

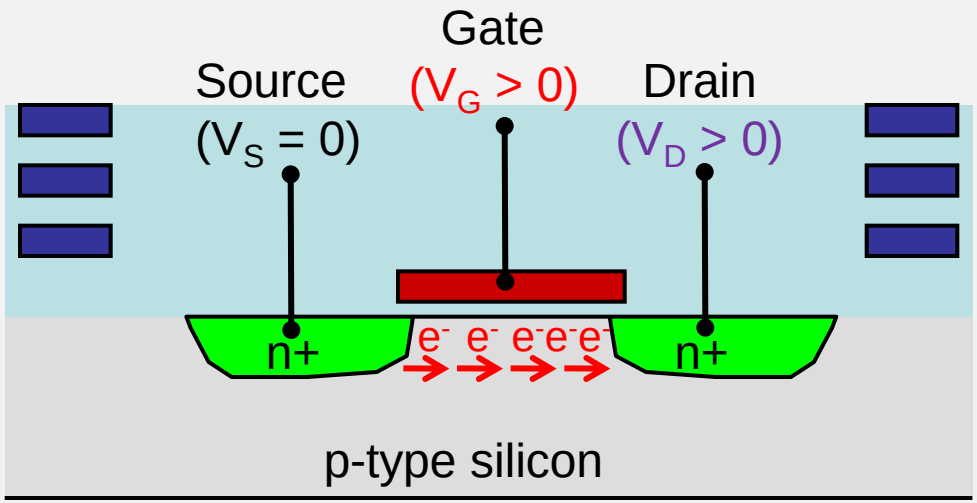
- 步驟一：增加gate電壓，吸引drain及source端電子累積在矽基板表面



- 步驟二：增加drain電壓，將所累積之電子吸引過去，便形成電流 (由drain流到source)

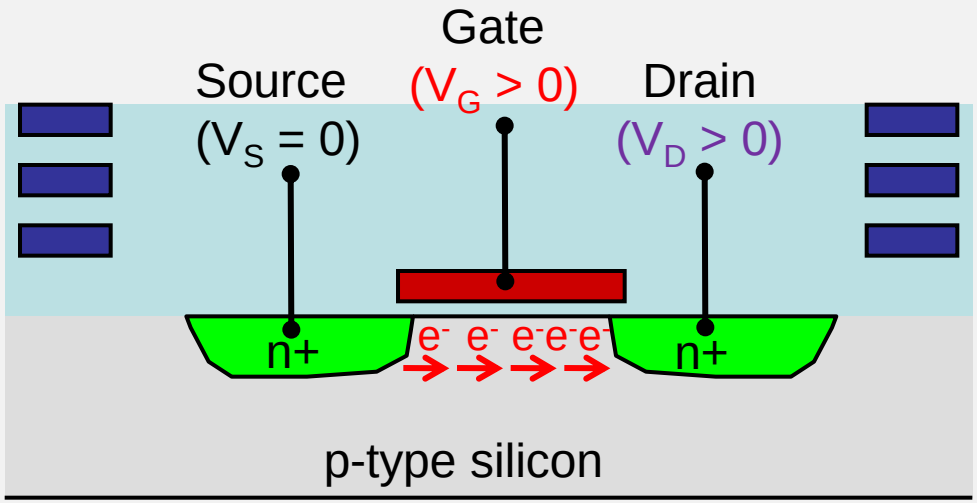


Cont'd: Threshold Voltage



- $V_{GS} > V_t$ (V_t: threshold voltage)，則在silicon表面形成n channel（可稱之為channel inversion）
- $V_{GS} < V_t$，則電晶體可能不導通、或導通微量的sub-threshold current

$V_{GS} > V_t$: Triode and Active (Saturation) Regions



- Given that $V_{GS} > V_t$:
  1. $V_{DS} < V_{GS} - V_t$ (即$V_{GD} > V_t$) : the transistor operates in the triode region
  2. $V_{DS} = V_{GS} - V_t$ ($V_{GD} = V_t$,此為n channel在drain端成立的最小V_{GD}值): the channel becomes pinched off
  3. $V_{DS} > V_{GS} - V_t$ ($V_{GD} < V_t$) : the transistor operates in the active (or saturation) region

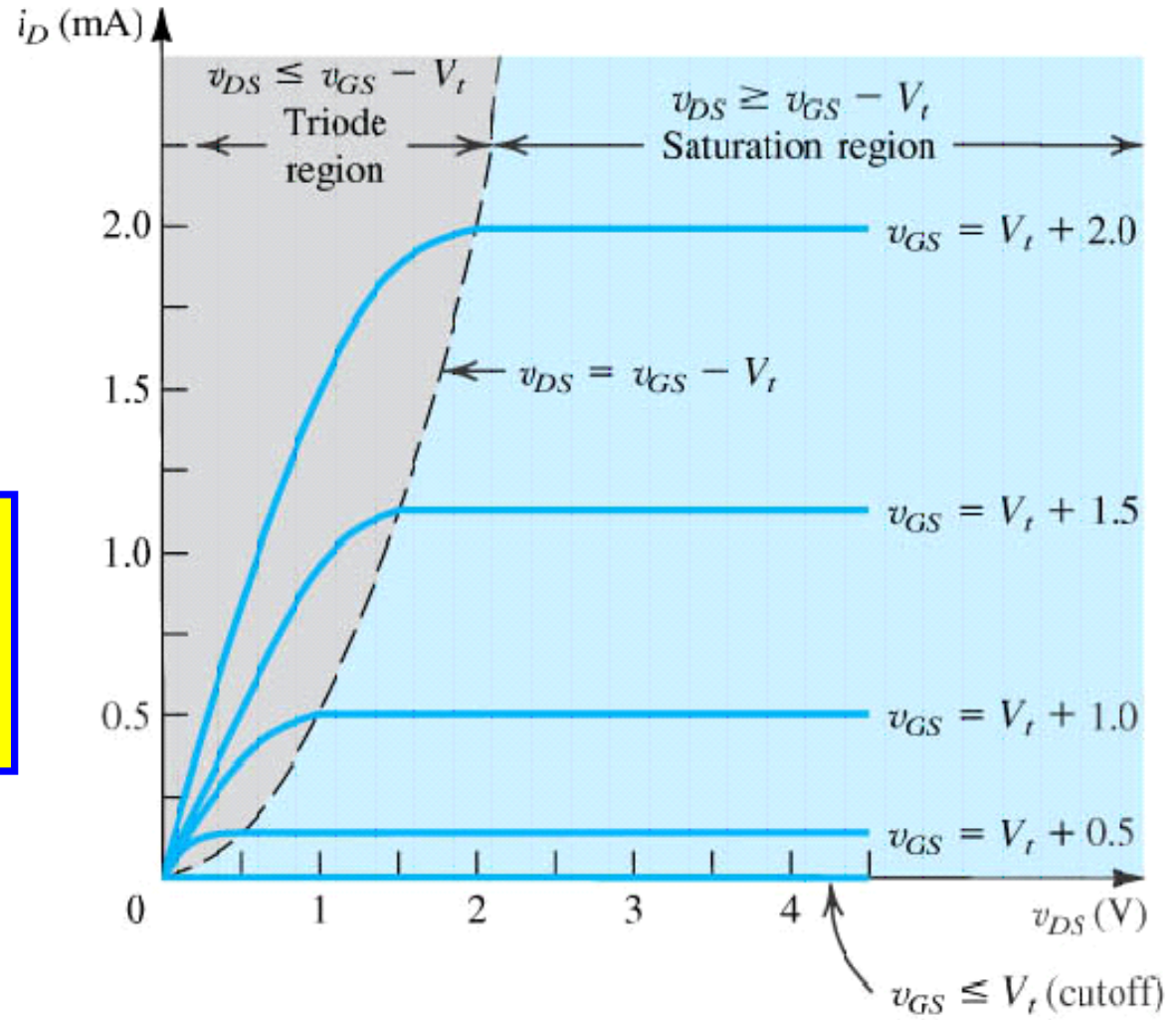
MOSFET I-V Relationship

In saturation region:

$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(v_{GS} - V_t)^2$$

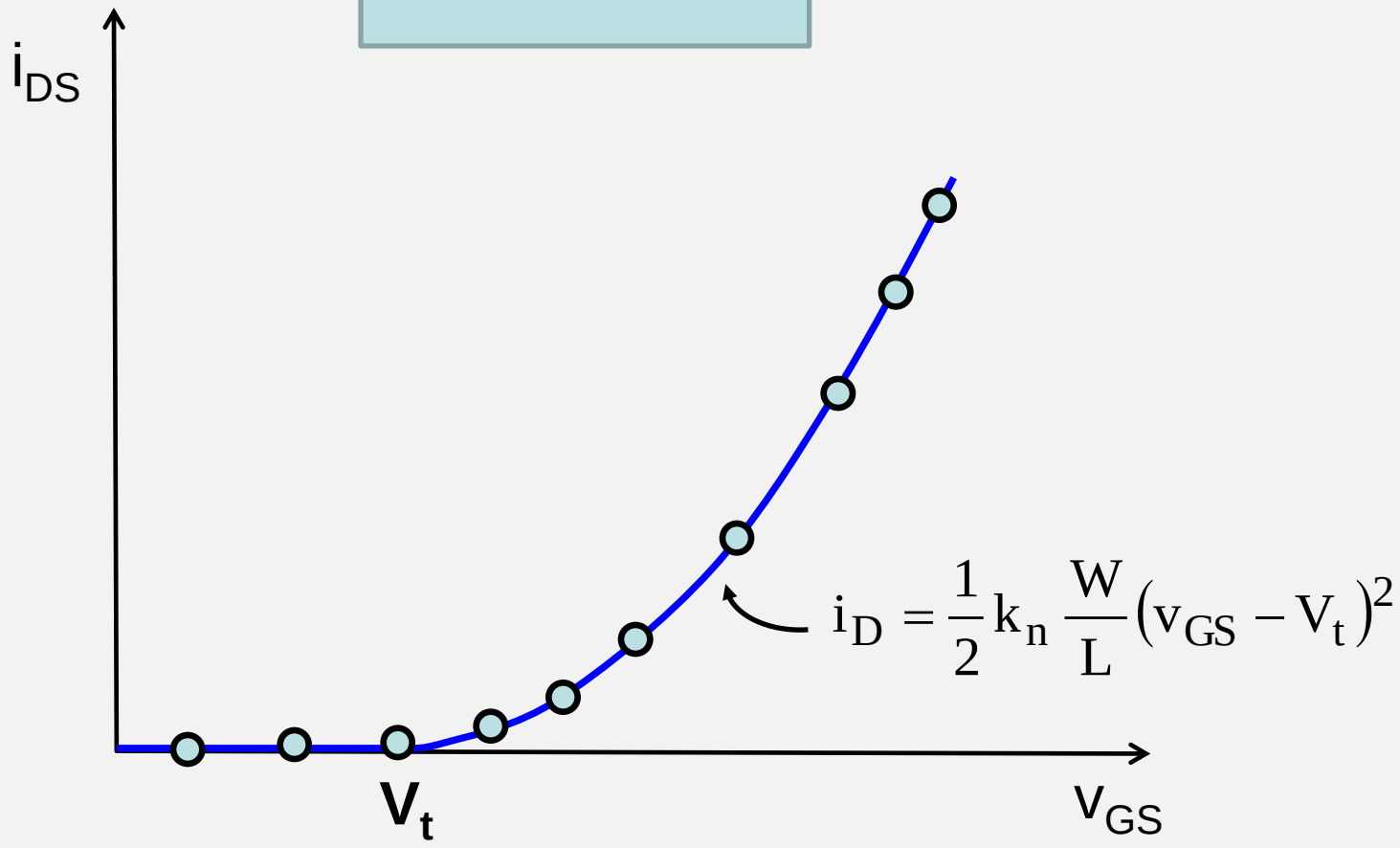
$$= \frac{1}{2}k_n \frac{W}{L}(v_{GS} - V_t)^2$$

μ_n: mobility ($m^2/(V \cdot sec)$)
C_{ox}: gate capacitance per unit area (F/m^2)
V_t: threshold voltage



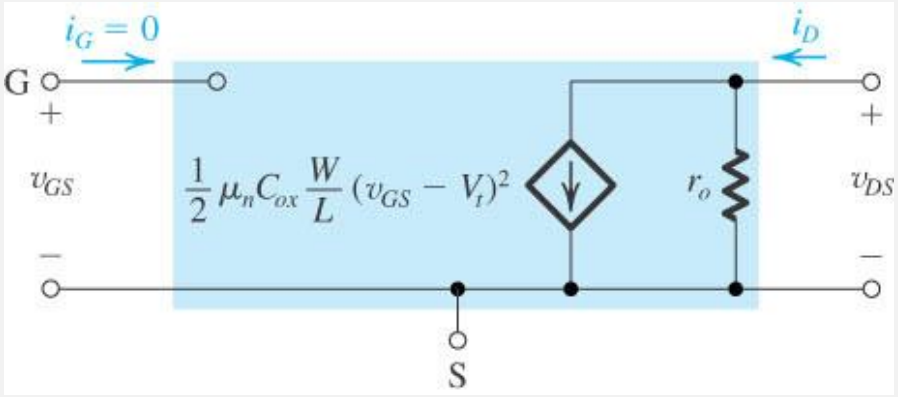
Threshold Voltage Measurement

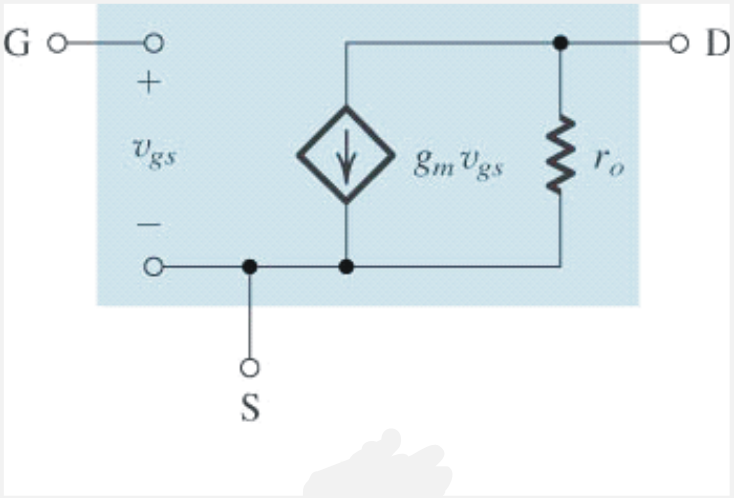
Set $v_{DS} \geq v_{GS} - V_t$



Large-Signal vs. Small-Signal Models

- **Under a fixed DC bias → By linearization to get the small-signal model**



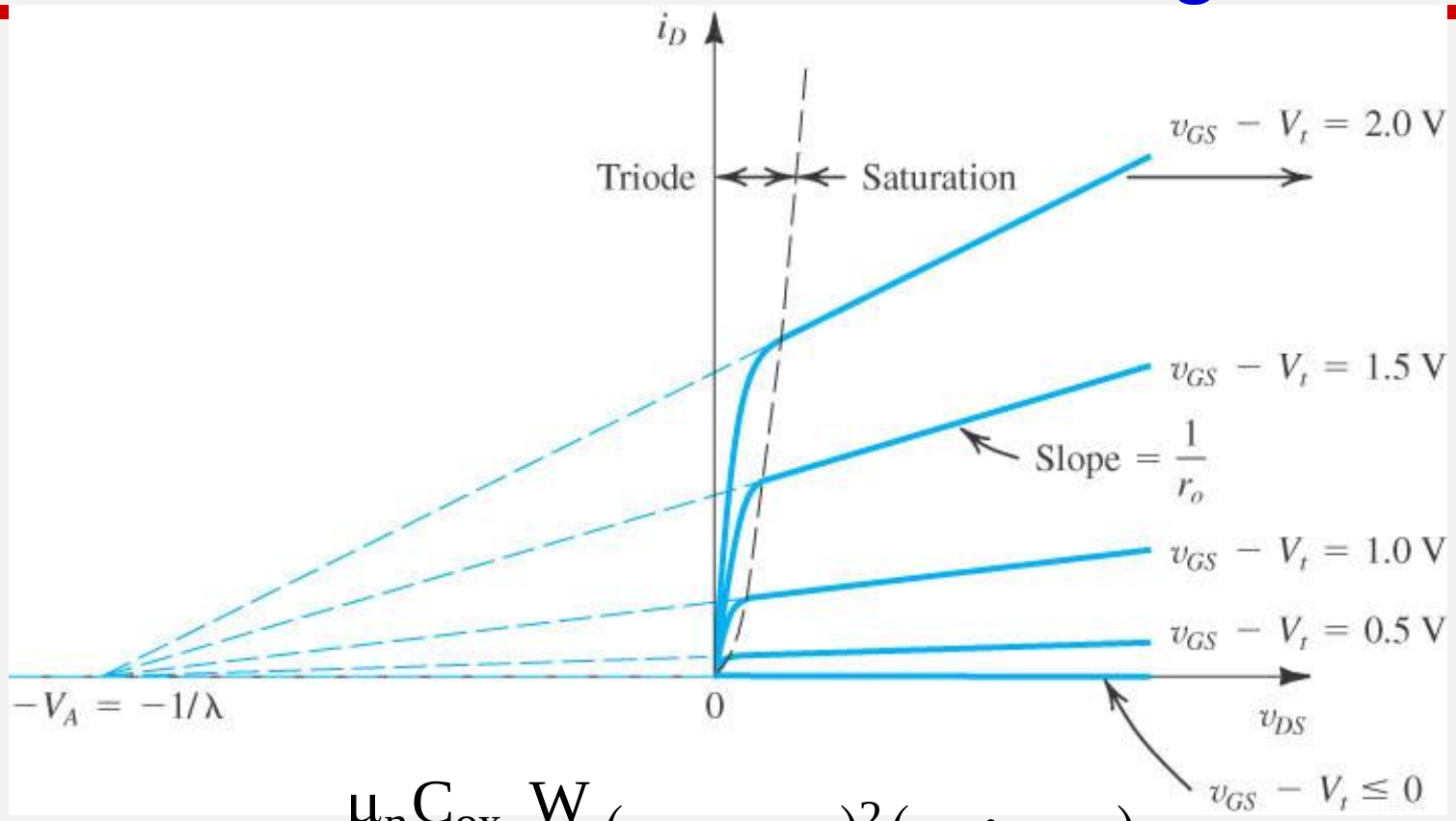


- **Definition of g_m (transconductance)**

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \mu_n \cdot C_{ox} \cdot \frac{W}{L}\left(V_{gs} - V_t\right)$$

$$\text{or} \quad g_m = \frac{2I_D}{V_{gs} - V_t}$$

Non-Ideal Effect: Finite Output Resistance in Saturation Region

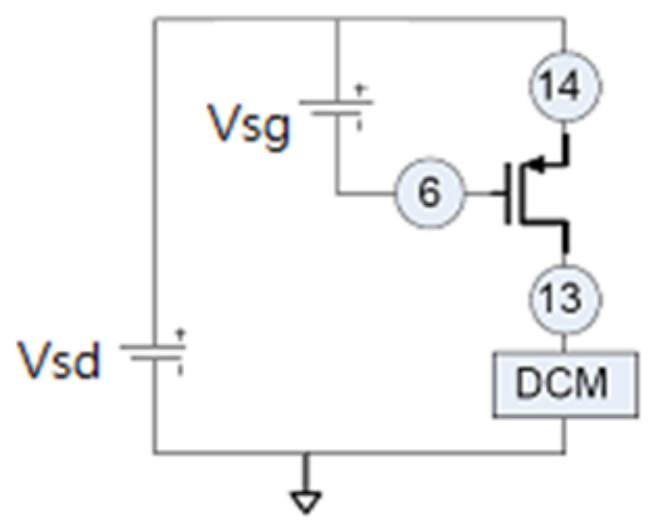


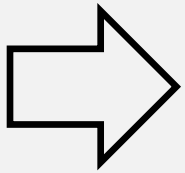
$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

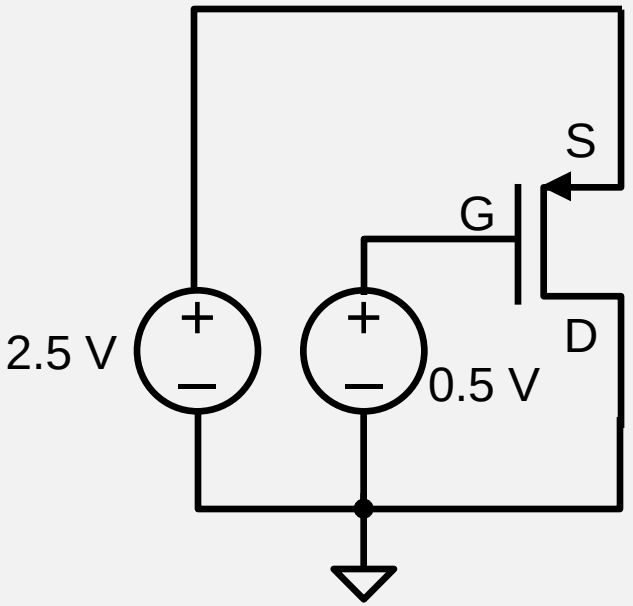
$$\frac{1}{r_o} = \frac{\partial I_D}{\partial V_{DS}} = \lambda I_D = \frac{I_D}{V_A},\ I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\cdot(V_{GS} - V_t)^2$$

Important for the Lab: Use Two Power Supplies for PMOS I-V Measurement

- For example: V_{sd} = 2.5 V, V_{sg} = 2 V: use the connection as shown on the right-hand side







MOSFET Level 1 SPICE Model Parameters

Note: threshold voltage is positive for a NMOS, negative for a PMOS

Parameter	Name	Default value
Vto	Zero-bias threshold voltage	1.0 V
KP	Transconductance parameter	2×10^{-5} A/V^2
LAMBDA	Channel-length modulation	0.0 V^{-1}
TOX	Thin oxide thickness	1×10^{-7} m
GAMMA	Body-effect parameter	0.0 V$^{0.5}$
PB	Bulk junction potential	0.80 V
CBD	Zero-bias body-drain capacitance	0.0 F/m^2
CBS	Zero-bias body-source capacitance	0.0 F/m^2
CGBO	Gate-body overlap capacitance	0.0 F/m
CGDO	Drain-body overlap capacitance	0.0 F/m

A More Complete MOSFET Model for Advanced Technology

- **BSIM (Berkeley Short-channel IGFET Model) CMOS model (the major MOS model used in industry)**
  - **semi-empirical model**

- **BSIM model ~ 250 parameters**

BSIM4_Model
BSIM4M1

NMOS=yes	Igbmod=	Xj=	Vbx=	Dvt0=	U0=	Rdswmin=	Pdits=	Pbswgs=	Mjswgd=	Voffcv=	Llc=	Wln=	Clc=	Cigc=	Pigcd=	Rbpd=
PMOS=no	Paramchk=	Vsat=	Vbm=	Dvt1=	Eu=	Rsw=	Peditsl=	Mjswgs=	Cjd=	Dmcg=	Lln=	Ww=	Cle=	Aigsd=	Poxedge=	Noia=
Capmod=	Binunit=	At=	Xt=	Dvt2=	Ute=	Rdw=	Peditsd=	Cjs=	Cjswd=	Dmci=	Lw=	Wwc=	Dwc=	Bigsd=	Ijthdfwd=	Noib=
Diomod=	Version=	A0=	K1=	Dvt0w=	Voff=	Rdwmin=	Pscbe1=	Cjsws=	Cjswgd=	Dmdg=	Lwc=	Wwn=	Dlc=	Cigsd=	Ijthsfwd=	Noic=
Rdsmod=	Toxe=	Ags=	Kt1=	Dvt1w=	Minv=	Rswmin=	Pscbe2=	Cjswgs=	Vfbcv=	Dmcgt=	Lwn=	Wwl=	Dlcig=	Aigbacc=	Ijthdrev=	Tnoia=
Tmqsmod=	Toxp=	A1=	Kt1l=	Dvt2w=	Voffl=	Prwg=	Pvag=	Jsd=	Vfb=	Xgw=	Lwl=	Wwlc=	Dwj=	Bigbacc=	Ijthsrev=	Tnoib=
Acnqsmod=	Toxm=	A2=	Kt2=	Drout=	Tnom=	Prwb=	Jss=	Jswd=	Tpb=	Xgl=	Lwlc=	Wmin=	Alpha0=	Cigbacc=	Xjbvd=	Ntnoi=
Mobmod=	Toxref=	Keta=	K2=	Dsub=	Trise=	Prt=	Jsws=	Jswgd=	Tcj=	Rshg=	Lmin=	Wmax=	Alpha1=	Aigbinv=	Xjbvs=	Em=
Rbodymod=	Dtox=	Nsub=	K3=	Vth0=	Cgso=	Eta0=	Jswgs=	Pbd=	Tpbsw=	Ngcon=	Lmax=	B0=	Beta0=	Bigbinv=	Bvd=	Ef=
Rgatemod=	Epsrox=	Ndep=	K3b=	Ua=	Cgdo=	Etab=	Pbs=	Njd=	Tcjsw=	Xrcrg1=	Wr=	B1=	Agidl=	Cigbinv=	Bvs=	Af=
Permod=	Cdsc=	Nsd=	W0=	Ua1=	Cgbo=	Pclm=	Njs=	Xtid=	Tpbswg=	Xrcrg2=	Wint=	Cgsl=	Bgidl=	Nigc=	Gbmin=	Kf=
Geomod=	Cdscb=	Phin=	Dvtp0=	Ub=	Xpart=	Pdiblc1=	Xtis=	Mjd=	Tcjswg=	Xw=	Dwg=	Cgdl=	Cgidl=	Nigbinv=	Rbdb=	Imelt=
Fnoimod=	Cdscd=	Ngate=	Dvtp1=	Ub1=	Delta=	Pdiblc2=	Mjs=	Pbswd=	Acde=	Xl=	Dwb=	Ckappas=	Egidl=	Nigbacc=	Rbpb=	AllParams=
Tnoimod=	Cit=	Gamma1=	Lpe0=	Uc=	Rsh=	Pdiblcb=	Pbsws=	Mjswd=	Moin=	Lint=	Wl=	Ckappad=	Aigc=	Ntox=	Rbsb=	
Igcmod=	Nfactor=	Gamma2=	Lpeb=	Uc1=	Rdsw=	Fprout=	Mjsws=	Pbswgd=	Noff=	Ll=	Wlc=	Cf=	Bigc=	Eigbinv=	Rbps=	

CD4007 MOSFET Array

- **To avoid damaging the transistors, make sure that you always turn the power off before making any circuit changes**