Part2_B卷

姓名:	林 靖	交卷時間 (IP):	2021-06-22 12:00	分數:	26 / 60

很抱歉，測驗結果沒有達到及格門檻 36 分。

溫馨小提醒

(0) 此考卷為**B卷** 請確認自己學號為**偶數**

(1) 建議同學準備好**計算紙** 寫考卷時自己標記題號並書寫計算過程
除了方便同學檢查自己答案是否有填寫正確之外
當題目有連貫性時 也可以幫助同學快速回顧之前答題時的想法

(2) 請同學**把握考試時間**
不像現場考試 助教沒辦法提醒同學再過幾分鐘收卷
建議同學先把會寫的題目寫完 再回頭處理比較困難的題目

(3) 填充題務必將答案四捨五入到**小數點第一位** (整數也請表示到小數第一位)
有特別標記需要填**正負號**的題目 請不要忘記
單位和**科學記號**都需要特別注意

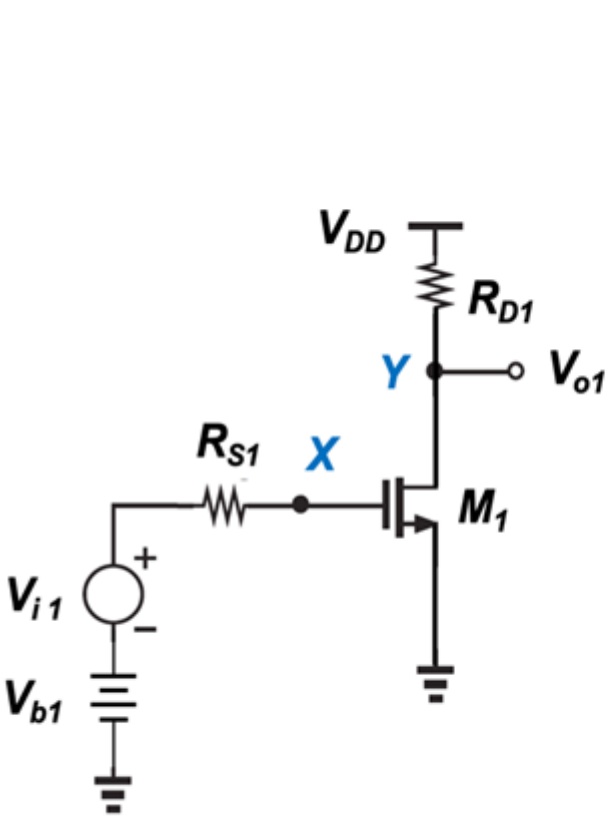
(4) 測試題範例
1+10 = 11.0
10-2-8 = 0.0 (add +/-)
1.5*1.5 = +2.3 (add+/-)
1.2*1.2 = 1.4

題組 (共 3 題)

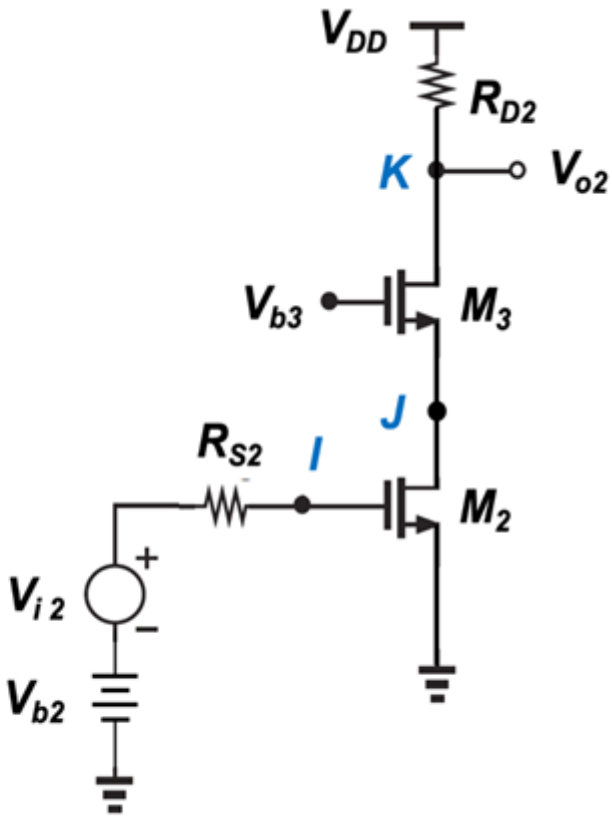
Problem Set 3-1
單選題 [6pts]

If not otherwise specified, please use the following parameters.

$$\mu_n C_{ox} = 0.25mA/V^2,\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 100, V_{TH} = 0.5V, \lambda = 0,$$
$$V_{DD} = 2V, I_{D1} = I_{D2} = 0.5mA,\ R_{D1} = R_{D2} = 2k\Omega,\ R_{S1} = R_{S2} = 2k\Omega$$
$$C_{GS} = 1pF, C_{GD} = C_{SB} = C_{DB} = 0.3pF, (\text{for each } M_1, M_2, \text{and } M_3)$$



Circuit D



Circuit E

In the **Circuit E**, to get the same voltage gain as **Circuit D**, the power dissipation will be

- A. higher than Circuit D
- B. lower than Circuit D
- C. same as Circuit D

正確答案: **C**

2

In the **Circuit E**, if there is no channel length modulation effect in MOS transistors, the output linear swing range compared to the **Circuit D** will be

- A. larger
- B. smaller
- C. the same

2

In the **Circuit E**, if bias voltage V_{b3} is reduced to make M_2 into triode region, the voltage gain of this circuit will

- A. increase
- B. decrease
- C. no change

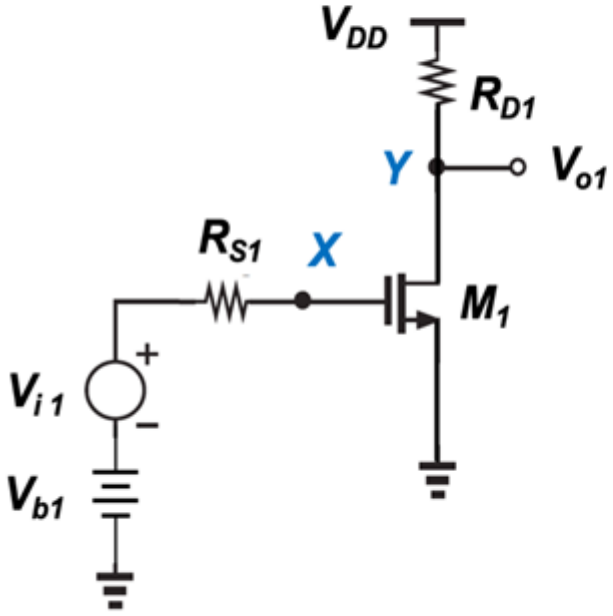
2

題組 (共 3 題)

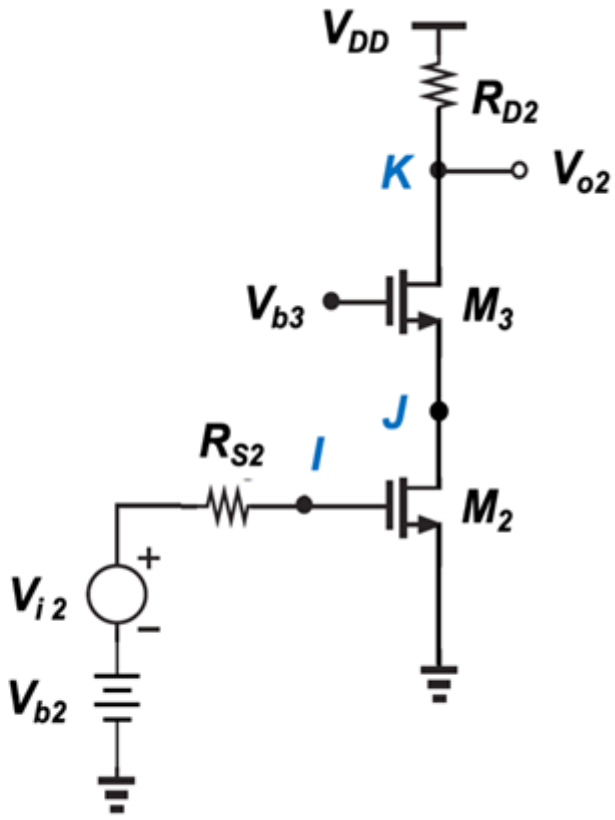
Problem Set 3-2
填充題 [28pts]

If not otherwise specified, please use the following parameters.

$$\mu_n C_{ox} = 0.25mA/V^2,\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 100, V_{TH} = 0.5V, \lambda = 0,$$
$$V_{DD} = 2V, I_{D1} = I_{D2} = 0.5mA,\ R_{D1} = R_{D2} = 2k\Omega,\ R_{S1} = R_{S2} = 2k\Omega$$
$$C_{GS} = 1pF, C_{GD} = C_{SB} = C_{DB} = 0.3pF, (\text{for each } \mathrm{M_1}, \mathrm{M_2}, \text{and } \mathrm{M_3})$$



Circuit D



Circuit E

Please calculate the voltage gain $|V_{out}/V_{in}|$ of **Circuit D** as 10.0 (4 分) V/V, and of **Circuit E** as 10.0 (4 分) V/V.

8

Please calculate the bias voltage V_{b1} of **Circuit D** as 0.5 **0.7** (4 分) V, and the bias voltage V_{b2} and **lowest bias voltage** V_{b3} of **Circuit E** as 0.5 **0.7** (4 分) V and 0.5 **0.9** (4 分) V, to keep all the transistors in saturation region.

12

In real case the transistors cannot enter triode region during signal swing. Based on Problem 5, when the input V_{i2} for **Circuit E** is A_2*cosωt , please find a V_{b3} voltage 1500.0 **1000.0** (4 分) mV to get the **maximum amplitude** A_2 500.0 **50.0** (4 分) mV. Make sure to keep all the transistors in saturation region when the maximum amplitude signal is applied. (e.g, 5.56=>5.6, 23.32=>23.3)

8

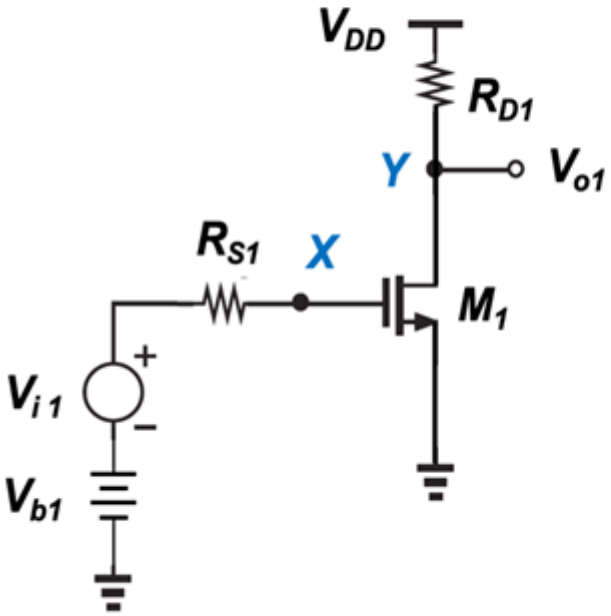
題組 (共 2 題)

Problem Set 3-3
填充題 [20pts]

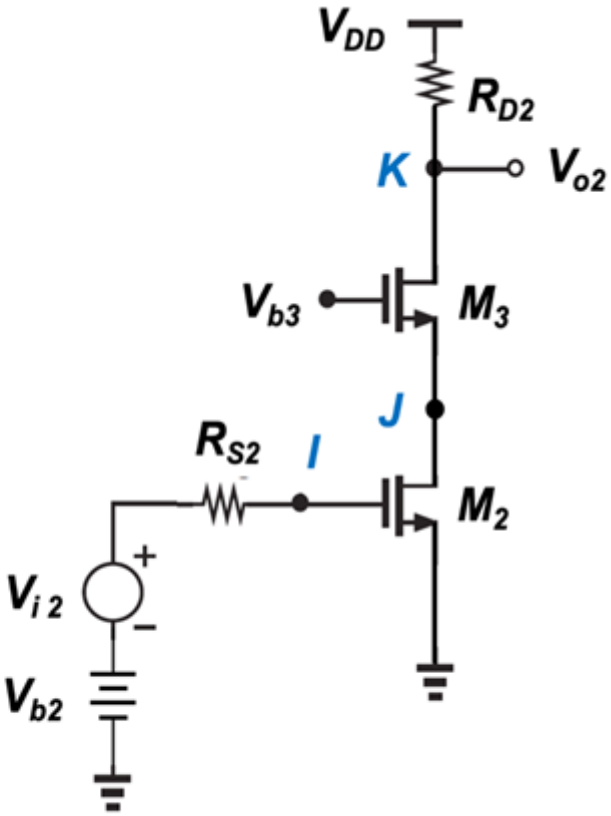
If not otherwise specified, please use the following parameters.

$$\mu_n C_{ox} = 0.25mA/V^2,\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 100, V_{TH} = 0.5V, \lambda = 0,$$
$$V_{DD} = 2V, I_{D1} = I_{D2} = 0.5mA,\ R_{D1} = R_{D2} = 2k\Omega,\ R_{S1} = R_{S2} = 2k\Omega$$
$$C_{GS} = 1pF, C_{GD} = C_{SB} = C_{DB} = 0.3pF, (\text{for each } M_1, M_2, \text{and } M_3)$$

Based on the bias condition in Problem 5, please use these parameters for each active device to calculate the frequency responses of **Circuit D** and **Circuit E**:



Circuit D



Circuit E

Please calculate the poles of **Circuit D**. At node X is 1.2 (4 分) x10^8 rad/sec and node Y is 7.9 (4 分) x10^8 rad/sec.

8

Please calculate the poles of **Circuit E**. At node I is 1.2 **3.1** (4 分) x10^8 rad/sec, node J is 5181.3 **22.7** (4 分) x10^8 rad/sec, and node K is 8.3 (4 分) x10^8 rad/sec.

12

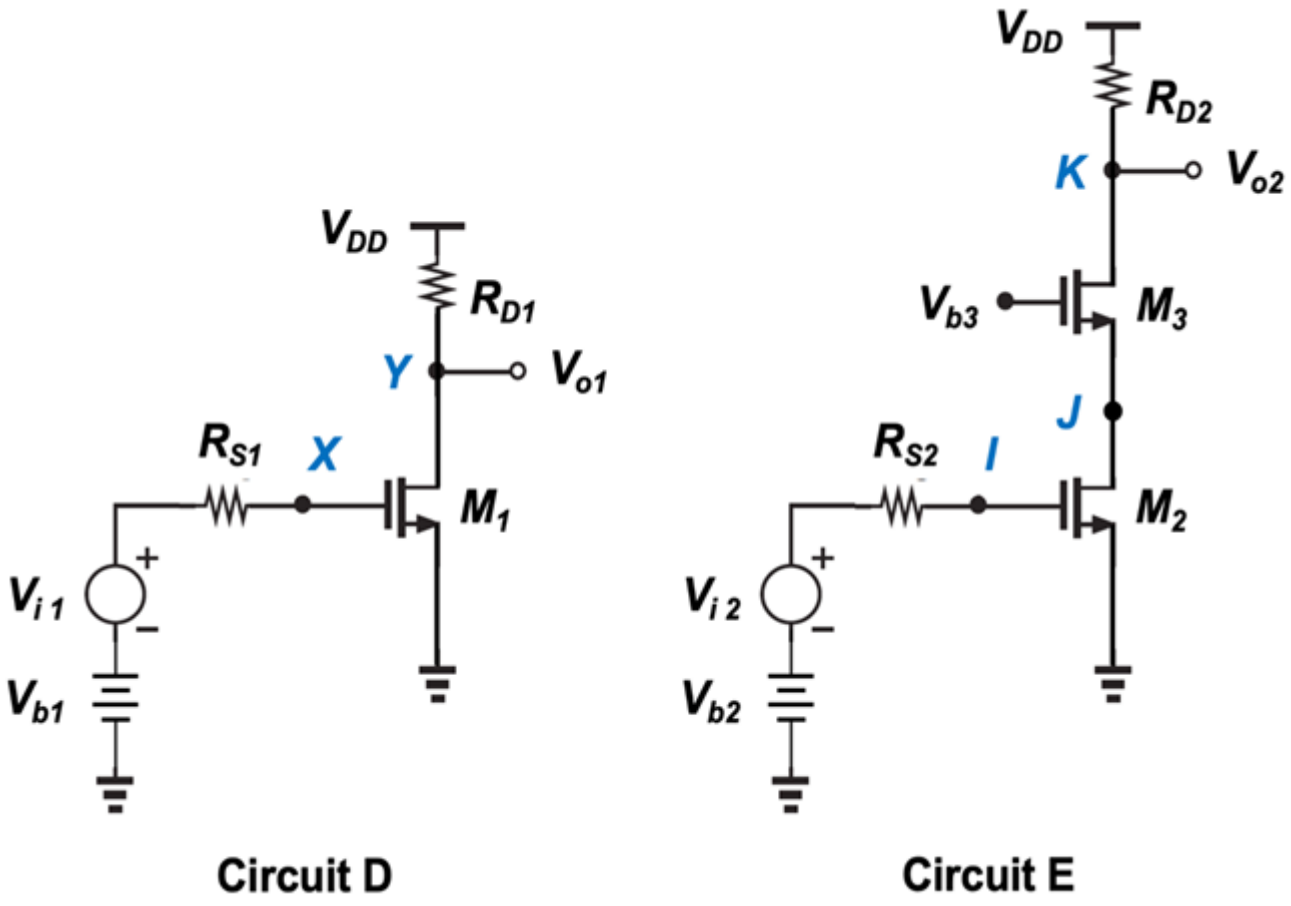
題組 (共 3 題)

Problem Set 3-4
單選題 [6pts]

If not otherwise specified, please use the following parameters.

$$\mu_n C_{ox} = 0.25mA/V^2,\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 100, V_{TH} = 0.5V, \lambda = 0,$$
$$V_{DD} = 2V, I_{D1} = I_{D2} = 0.5mA,\ R_{D1} = R_{D2} = 2k\Omega,\ R_{S1} = R_{S2} = 2k\Omega$$
$$C_{GS} = 1pF, C_{GD} = C_{SB} = C_{DB} = 0.3pF, (\text{for each } M_1, M_2, \text{and } M_3)$$

In **Circuit E**, we enlarge the load resistor R_{D2} for higher gain. If all the transistors are in saturation region,



the pole at node I will be

- A. at higher frequency
- B. at lower frequency
- C. no change

正確答案: **C**

2

the pole at node J will be

- A. at higher frequency
- B. at lower frequency

C. no change

正確答案: **C**

2

the pole at node K will be

A. at higher frequency

B. at lower frequency

C. no change

2