Part1_B卷

姓名:	林 靖	交卷時間 (IP):	2021-06-22 10:55	分數:	35 / 40

恭喜您，通過測驗的及格門檻 24 分!

溫馨小提醒

(0) 此考卷為**B卷** 請確認自己學號為**偶數**

(1) 建議同學準備好**計算紙** 寫考卷時自己標記題號並書寫計算過程
除了方便同學檢查自己答案是否有填寫正確之外
當題目有連貫性時 也可以幫助同學快速回顧之前答題時的想法

(2) 請同學**把握考試時間**
不像現場考試 助教沒辦法提醒同學再過幾分鐘收卷
建議同學先把會寫的題目寫完 再回頭處理比較困難的題目

(3) 填充題務必將答案四捨五入到**小數點第一位** (整數也請表示到小數第一位)
有特別標記需要填**正負號**的題目 請不要忘記
單位和**科學記號**都需要特別注意

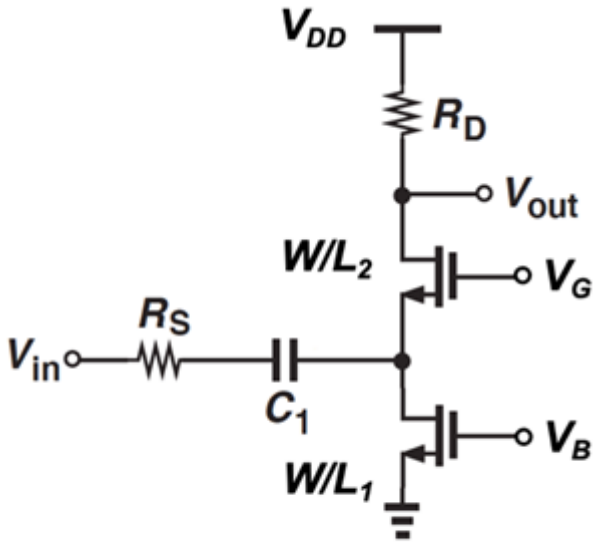
(4) 測試題範例
1+10 = 11.0
10-2-8 = 0.0 (add +/-)
1.5*1.5 = +2.3 (add+/-)
1.2*1.2 = 1.4

題組 (共 4 題)

Problem Set 1-1
單選題 [8pts]

Please answer problem 1~4 according to Circuit A.

Circuit A is a common gate circuit. If all the transistors are in saturation region and ignore the channel length modulation, V_{DD}, V_B, V_G voltages are fixed, to **decrease the voltage gain $|(V_{out}/V_{in})|$**,



Circuit A

The load resistor R_D has to

- A. increase
- B. decrease
- C. no change

2

The common gate size $(W/L)_2$ has to

- A. increase
- B. decrease
- C. no change

2

The bias transistor size $(W/L)_1$ has to

- A. increase
- B. decrease
- C. no change

2

The source impedance R_S has to

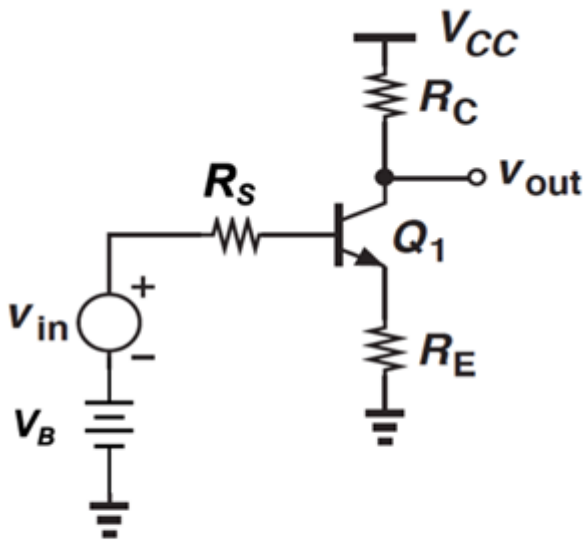
- A. increase
- B. decrease
- C. no change

題組 (共 4 題)

Problem Set 1-2
單選題 [8pts]

Please answer problem 5~8 according to Circuit B.

Circuit B is an emitter degenerated amplifier. If the transistor Q_1 is in active region, V_{CC}, V_B voltages are fixed, when the **degeneration resistor R_E decreases**,



Circuit B

The voltage gain will

- A. increase
- B. decrease
- C. no change

2

The input impedance will

- A. increase
- B. decrease
- C. no change

2

The output impedance will

- A. increase
- B. decrease
- C. no change

2

The output swing range will

- A. increase
- B. decrease
- C. no change

正確答案: **C**

2

題組 (共 4 題)

Problem Set 2:
填充題 [21pts]
單選題 [3pts]

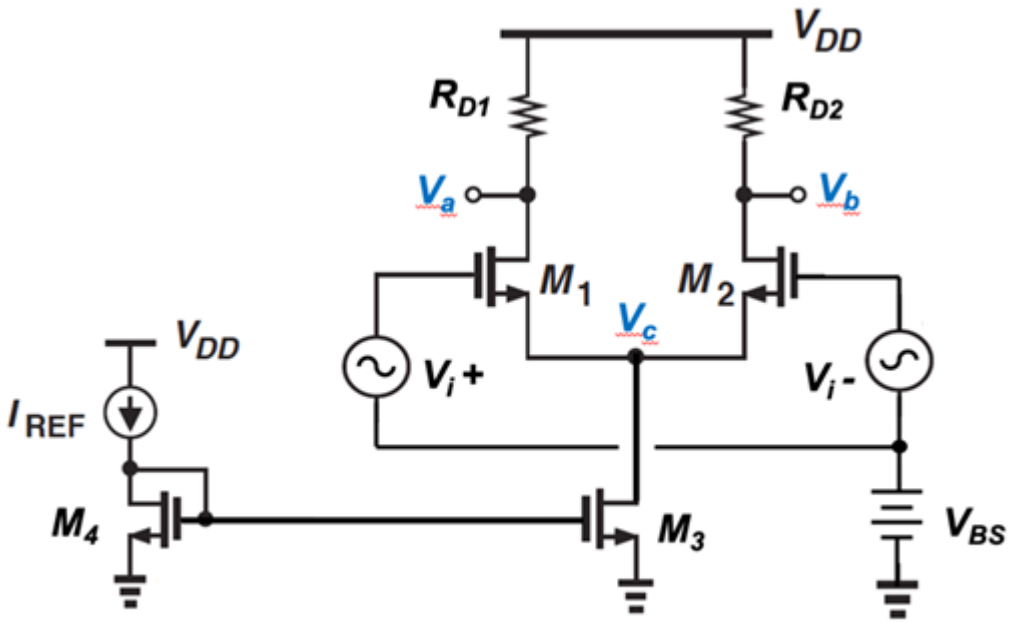
Please answer problem 9-12 according to Circuit C.
Please use the following parameters.

$$\mu_n C_{ox} = 0.125\,mA/V^2,\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 100,\ V_{TH} = 0.4V,$$

$\lambda_1 = \lambda_2 = 0,\ \lambda_3 = \lambda_4 = 0.1\,V^{-1},$

$V_{DD} = 2.0V,\ R_{D1} = R_{D2} = 4k\Omega, I_{REF} = 0.1mA, and\ \left(\frac{W}{L}\right)_3 : \left(\frac{W}{L}\right)_4 = 5:1$

In Circuit C, all the transistors are with no body effect.



Circuit C

If the output common mode level is 1V, and the V_{GS3} is 0.5V, the input common mode level V_{BS} has to be 0.5 **1.1** (3 分) V to make the M_1 DC current 2.5 (3 分) x10^{-1} mA, and M_3 DC current is 5.0 (3 分) x10^{-1} mA. (e.g, 2.19 => 2.2, 0.34 => 0.3).

9

The small signal differential mode voltage gain (Va)/(Vi+) is -10.0 (3 分) V/V, voltage gain (Vb)/(Vi+) is +10.0 (3 分) V/V, voltage gain (Vc)/(Vi+) is +0.0 (3 分) V/V. (add + or - in each answer).

9

The small signal common mode voltage gain is -9.9 (3 分) x10^{-2} V/V. (add + or -).

In this circuit, which is the possible way to increase the input differential mode linear range?

- A. increase RD
- B. decrease VDD
- C. increase W/L of M1 and M2
- D. increase IREF