Dept EE, National Tsing Hua University HW 4 (chapter 11) EE2255 Electronics

Fig. 1 shows the common-source amplifier with V_{DD} as 1.8 V, C_L as 0.5 pF, and channel length as 1 µm. In **AC analysis**, V_{in} represents a small signal with AC amplitude = 1; in **transient analysis**, V_{in} is a 10 KHz sinusoidal waveform with 0.5-mV amplitude ($V_{p-p} = 1$ mV).

- (1) First of all, utilize **AC analysis** to design your *V_G*, *R_D*, and width of NMOS to make small-signal gain larger than 10 V/V and -3dB bandwidth wider than 30 MHz at the same time (hint: you need to know the conversion between dB and V/V).
- (2) Secondly, utilize **transient analysis** to display NMOS operating in saturation region $(V_{DS} > V_{GS} V_{th} > 0)$, and check the ratio of output amplitude to input amplitude is larger than 10 V/V.
- (3) Finally, try to achieve the best figure of merit (FoM) value as "gain (V/V) * bandwidth (MHz) / drain current of NMOS (mA)," and calculate it (hint: use the DC offset of drain current in transient analysis to calculate FoM).
- (4) If your FoM achieves above 300, 800, you can get 5, 10 bonus points respectively in this HW.

$$FoM = \frac{gain (V/V) \cdot BW (MHz)}{current (mA)}$$



Fig. 1

Appendix

(1) Setup of AC analysis



(2) Setup of voltage source used in AC analysis

🍠 Independent Voltage Source - Vin	×
Functions	DC Value
(none)	DC value:
PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	Make this information visible on schematic: \checkmark
O EXP(V1 V2 Td1 Tau1 Td2 Tau2)	Small signal AC analysis(.AC)
SFFM(Voff Vamp Fcar MDI Fsig)	AC Amplitude: 1
OPWL(t1 v1 t2 v2)	AC Phase:
OPWL FILE: Browse	Make this information visible on schematic: \fbox
	Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: 🗹
Additional PWL Points Make this information visible on schematic: 🗹	Cancel OK



(4) Setup of NMOS Schematic

🎔 Select Compo	onent Symbol			×
Top Directory:	C:\Users\PC-Lab\Doc	uments\LTspiceX	(VII\lib\sym	~
		N-Channel Mo substrate conr MOSFETS)	OSFET transistor with ex nection(used for monoliti	plicit hic
E_		Open this nmos4	: macromodel's test fixtur	re
C:\Users\PC-La	b\Documents\LTspiceX	(VII\lib\sym\		
[ADC]	[SpecialFunctions]	f Familia Danad	load	np
[Contrib]	lowitchesj	FerriteBead2	Innn	pji
[DAC]	bi2	a	Itline	pn
[Digital]	bv	g2	mesfet	pn
[FilterProducts]	сар	ĥ	njf	pn
[Misc]	CSW	ind	nmos	pn
[OpAmps]	current	ind2	nmos4	рс
[Optos] [PowerProducts]	aiode	15016750-2	npn	re
[References]	e e2	I FD	npn2	sc
			nprie	
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C	Cancel		ОК	

(5) Setup of NMOS Model

🍠 Edit Text on the Schen	natic:		×
How to netlist this text Comment SPICE directive	Justification Left ~ Vertical Text	Font Size 1.5(default) V	OK Cancel
odel NMOS NMOS(level=2 vto=	:0.5 kp=300u lambda=100	m tox= 300n Cgso=50p	Cgdo=50p) 🔨
Type Ctrl-M to start a new line.			

vto means V_{th} , kp means $\mu_n C_{ox}$, lambda means λ

(6) If you want to know the parasitic capacitance of NMOS, please run operating point simulation and check the <u>log</u> file in the same folder. To simplify the model, we assume gate-source capacitance Cgs = 2/3*W*L*Cox + W*Cgso, and gate-drain capacitance Cgd = W*Cgdo.



•••	4ac.log		None	\$ (i)
1 Circui	t: * /Users/hjchen/Downloads	/4ac.asc		
2				
3 Instan	ce "m1": Length shorter thar	recommended for a le	evel 2 MOSFET	r.
4 Direct	Newton iteration for .op po	int succeeded.		
5 Semico	nductor Device Operating Poi	.nts:		
6	MOSFET	Transistors		
7 Name:	m1			
8 Model:	nmos			
9 Id:	5.70e-04			
10 Vgs:	6.00e-01			
11 Vds:	1.23e+00			
12 Vbs:	0.00e+00			
13 Vth:	5.00e-01			
14 Vdsat:	1.00e-01			
15 Gm:	1.14e-02			
16 Gds:	6.49e-05			
17 Gmb:	0.00e+00			
18 Cbd:	0.00e+00			
19 Cbs:	0.00e+00			
20 Cgsov:	1.67e-14			
21 Cgdov:	1.67e-14			
22 Cgbov:	0.00e+00			
23 Cgs:	2.56e-14			
24 Cga:	0.000+00			
25 Cgb:	0.00e+00			
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29 Date:	Thu Jun 17 23:45:35 2021			
30 Total	elapsed time: 0.052 seconds.			
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32 tnom =	27			