Dept EE, National Tsing Hua University EE2255 Electronics
HW 4 (chapter 11)

Student ID: **Name:**

Notice

(1) **Delay is not allowed**. *(-100pt)*
(2) Build **two simulation files** for **AC analysis** and **transient analysis** respectively.
(3) In LTspice **AC analysis**, you must set
  (a) type of sweep = decade,
  (b) number of points per decades = 100,
  (c) start frequency = 1,
  (d) stop frequency = 100meg. *(-1pt)*
(4) In LTspice **transient analysis**, you must set
  (a) stop time = 200u,
  (b) maximum timestep = 1n. *(-5pt)*
(5) The NMOS model is set by the directive: **.model NMOS NMOS(level=2 vto=0.5 kp=300u lambda=100m tox= 300n Cgso=50p Cgdo=50p)**. *(-10pt)*
(6) You must attach **three screenshots** in **AC analysis** including
  (a) schematic,
  (b) width of NMOS (the channel length is fixed at 1 μm)
  (c) bode plot (to display gain and bandwidth). *(-10pt)*
(7) You must attach **four screenshots** in **transient analysis** including
  (a) schematic,
  (b) waveform 1 (to display saturation),
  (c) waveform 2 (to display output amplitude),
  (d) waveform 3 (to display drain current). *(-10pt)*
(8) You must extract the data by **cursor**, including
  (a) small-signal gain,
  (b) -3dB bandwidth,
  (c) amplitude of output voltage,
  (d) DC offset of drain current. *(-5pt)*
(9) Please check the hand-writing result in your photo is **clear**. *(-5pt)*

Fig. 1 shows the common-source amplifier with V_{DD} as 1.8 V, C_L as 0.5 pF, and channel length as 1 μm. In **AC analysis**, V_{in} represents a small signal with AC amplitude = 1; in **transient analysis**, V_{in} is a 10 KHz sinusoidal waveform with 0.5-mV amplitude ($V_{p\text{-}p}$ = 1 mV).

(1) First of all, utilize **AC analysis** to design your V_G, R_D, and width of NMOS to make small-signal gain larger than 10 V/V and -3dB bandwidth wider than 30 MHz at the same time (hint: you need to know the conversion between dB and V/V).

(2) Secondly, utilize **transient analysis** to display NMOS operating in saturation region ($V_{DS} > V_{GS} - V_{th} > 0$), and check the ratio of output amplitude to input amplitude is larger than 10 V/V.

(3) Finally, try to achieve the best figure of merit (FoM) value as "gain (V/V) * bandwidth (MHz) / drain current of NMOS (mA)," and calculate it (hint: use the DC offset of drain current in transient analysis to calculate FoM).

(4) If your FoM achieves above 300, 800, you can get 5, 10 bonus points respectively in this HW.

$$\text{FoM} = \frac{\text{gain (V/V)} \cdot \text{BW (MHz)}}{\text{current (mA)}}$$

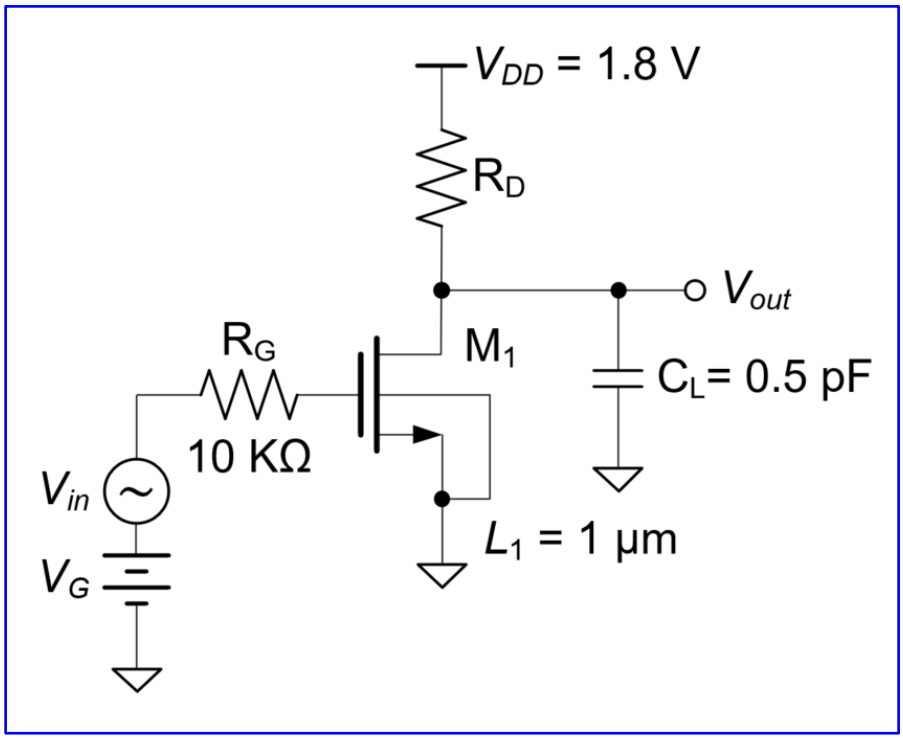
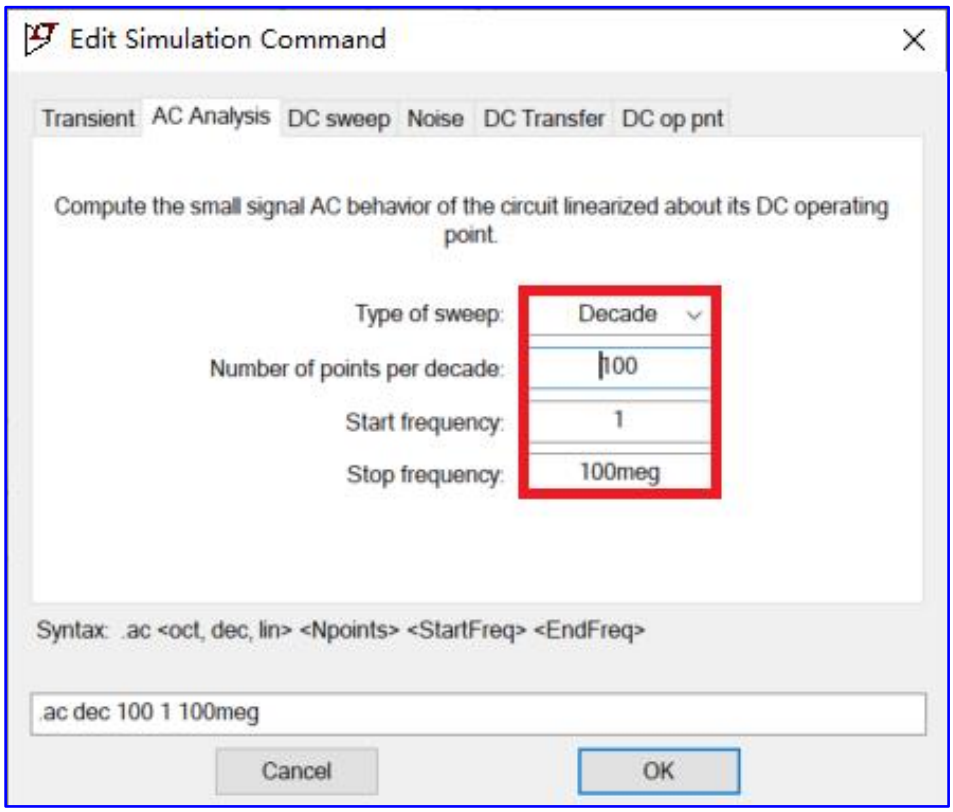


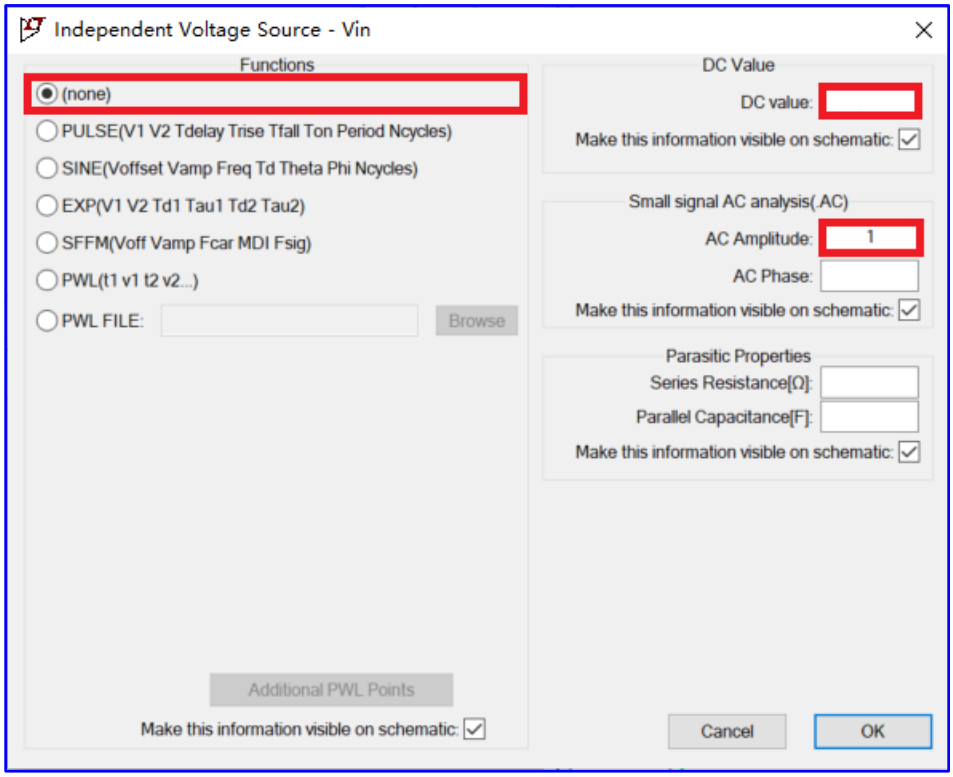
Fig. 1

Appendix

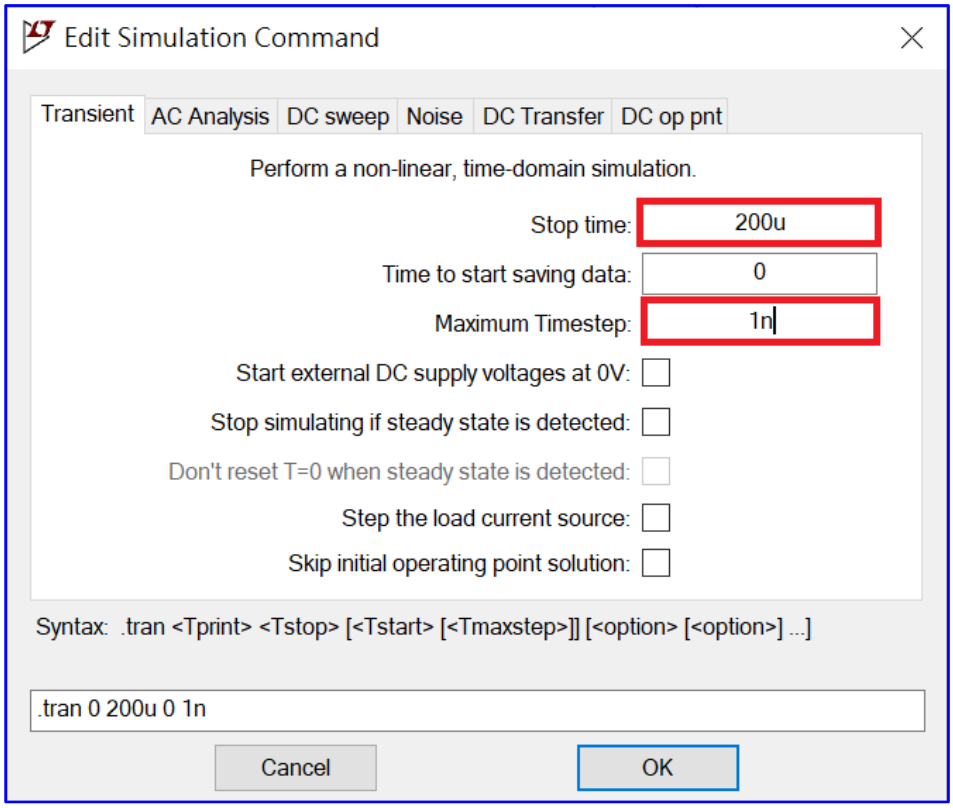
(1) Setup of AC analysis



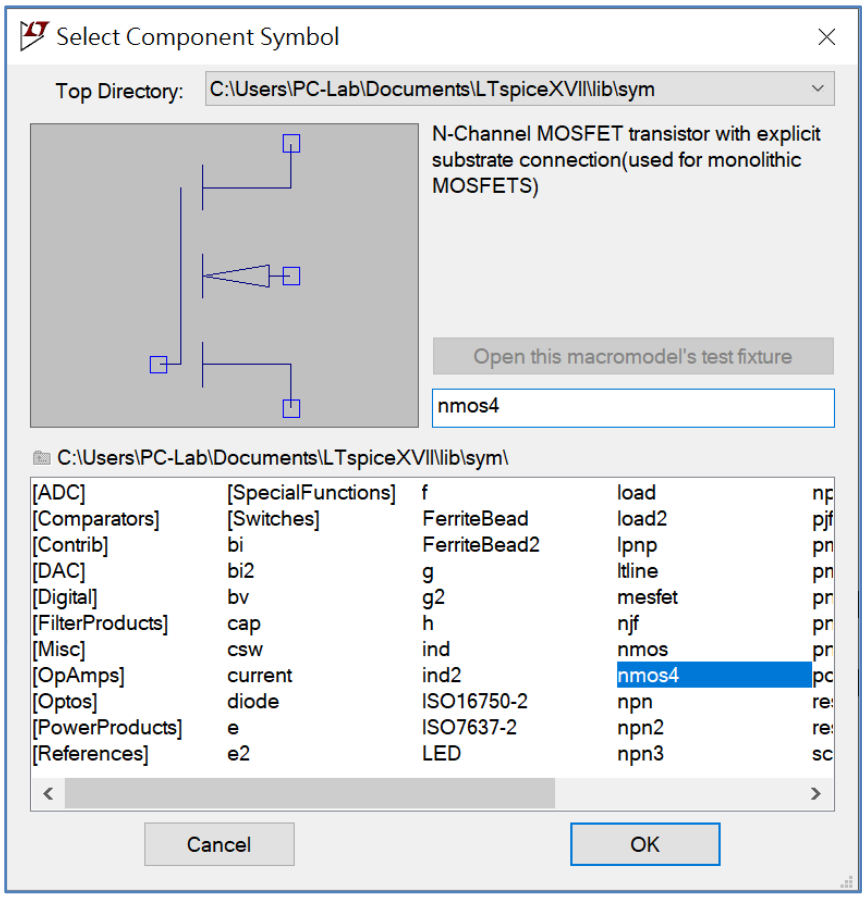
(2) Setup of voltage source used in AC analysis



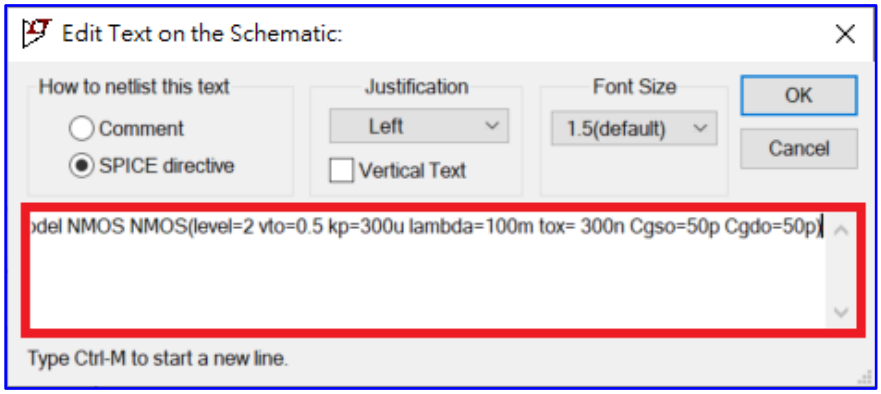
(3) Setup of Transient Analysis



(4) Setup of NMOS Schematic



(5) Setup of NMOS Model



vto means V_{th}, kp means $\mu_n C_{ox}$, lambda means λ

(6) If you want to know the parasitic capacitance of NMOS, please run operating point simulation and check the .log file in the same folder. To simplify the model, we assume gate-source capacitance Cgs = 2/3*W*L*Cox + W*Cgso, and gate-drain capacitance Cgd = W*Cgdo.