Dept. of EE, National Tsing Hua University EE2255 Electronics

HW3 (Chapter 6, 7)

Student ID: _____ Name: _____

Notice

(1) Delay is not allowed.(-100pt)

(2) We use LTspice transient analysis to see the voltage gain of signal. You must set stop time= 200u and maximum timestep = 1n. (-5pt)

(3) The NMOS model is set by the directive:
.model NMOS NMOS(vto=0.5 kp=300u lambda=100m). (-10pt)

(4) You must attach the screenshots of your NMOS size (like Fig. 5). (-10pt)

(5) You must attach screenshots of circuit and output waveform. (-10pt)

(6) You must extract the output amplitude by cursor. (-10pt)

(7) Please check the hand-writing result in your photo is clear. (-5pt or -10pt)

1. Fig. 1 shows the common-source amplifier with V_{DD} as 1.8 V. V_{in} is a 10KHz sinusoidal waveform with 0.5mV amplitude ($V_{p\text{-}p}$ = 1mV) .

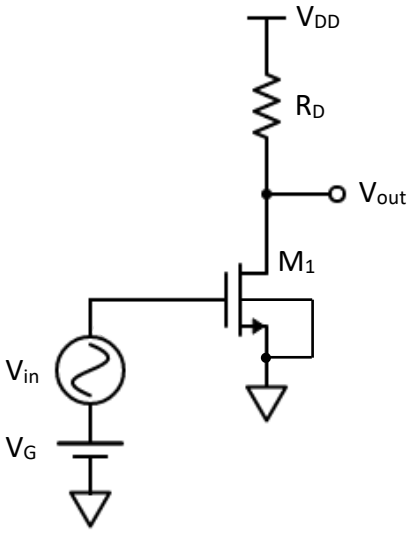

Fig. 1

(a) Please design your
W and L of NMOS (for 0.18μm technology both W and L should be longer than 0.18μm)
Gate bias V_G
Loading resistor R_D

You should achieve the voltage gain larger than 10 V/V. Note that the voltage gain means the

ratio of output amplitude to input amplitude.

(b) Please use **.OP** to show your output operating point and check your NMOS must be operating in "saturation region" ($V_{DS} > V_{GS} - V_{TH}$) .

(c) Base on λ and I_D. Please hand-calculate r_o of NMOS.

(d) Please use small signal model to calculate its voltage gain (r_o is NOT neglectable). Compare the results between hand-calculation and your simulation in (a).

2. Fig. 2 shows the common-drain amplifier (source follower) with V_{DD} as 1.8 V. V_{in} is a 10KHz sinusoidal waveform with 0.5mV amplitude (V_{p-p} = 1mV) .

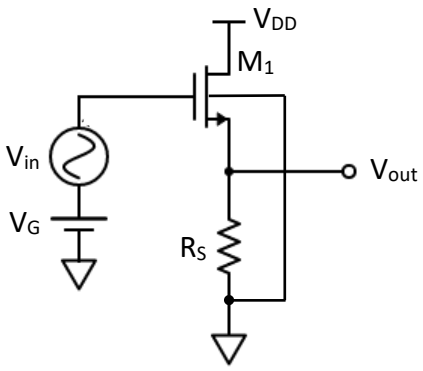

Fig. 2

(a) Please design your
W and L of NMOS (for 0.18μm technology both W and L should be longer than 0.18μm)
Gate bias V_G
Loading resistor R_S

You should achieve the voltage gain larger than 0.8 V/V. Note that the voltage gain means the ratio of output amplitude to input amplitude.

(b) Please use **.OP** to show your output operating point and check your NMOS must be operating in "saturation region" ($V_{DS} > V_{GS} - V_{TH}$) .

(c) Please use small signal model to calculate its voltage gain. Compare the results between hand-calculation and your simulation in (a) .

Appendix

(1) How to find NMOS schematic

Please choose nmos4 and short the “body port” to ground

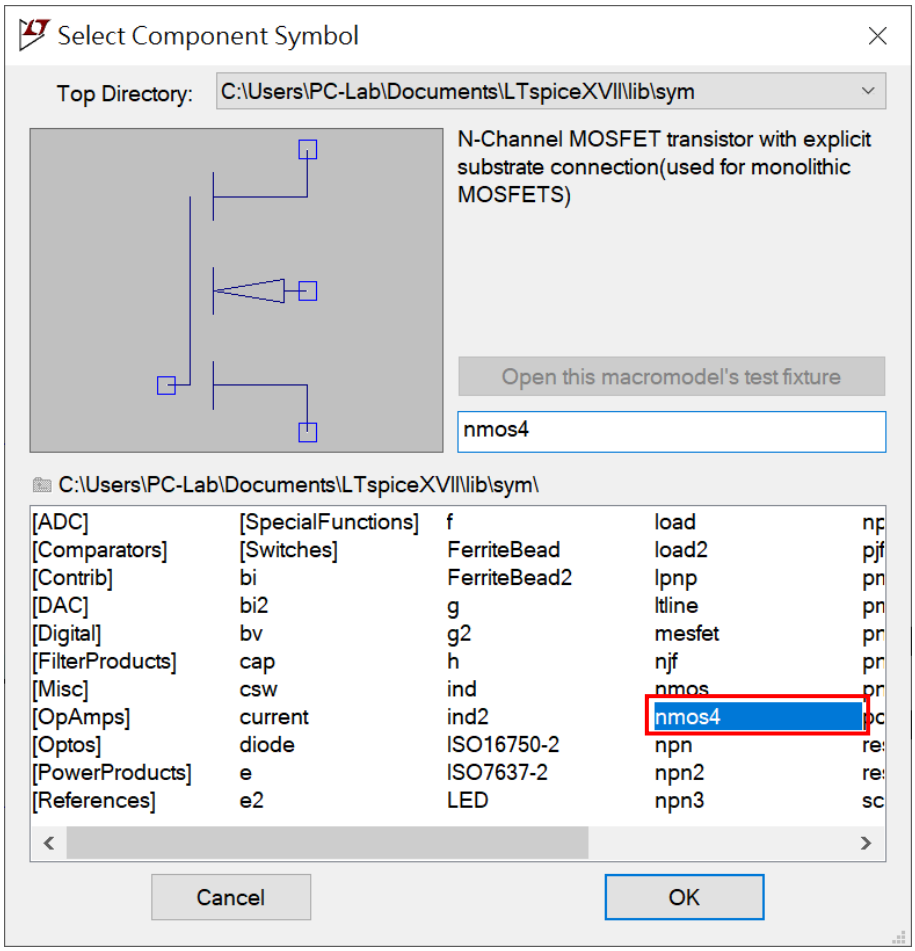

Fig. 3

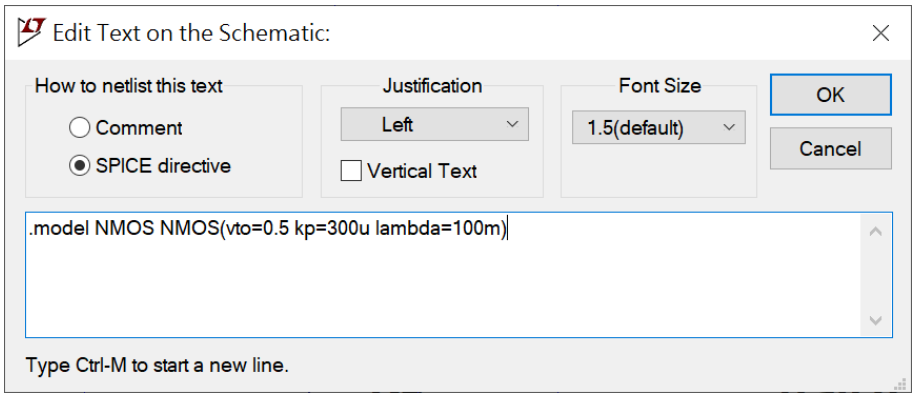

Fig. 4

In the model, vto means V_{TH}, kp means $\mu_n C_{ox}$, lambda means λ .

(2) How to change W and L of NMOS?

Right click on the NMOS schematic

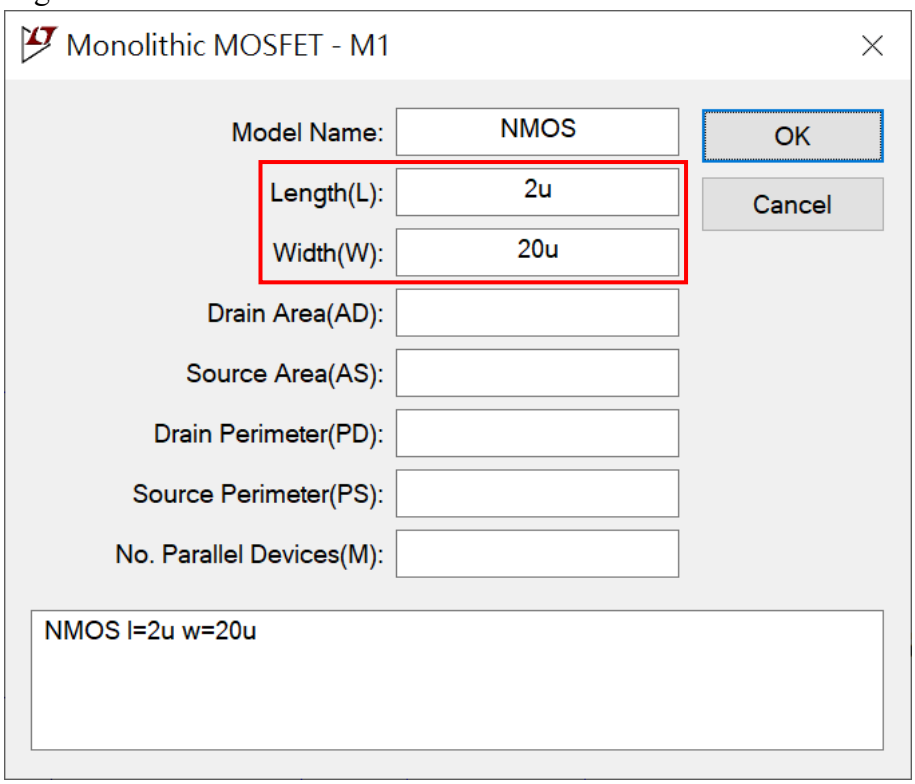

Fig. 5