林靖 108061112

1 AC Analysis

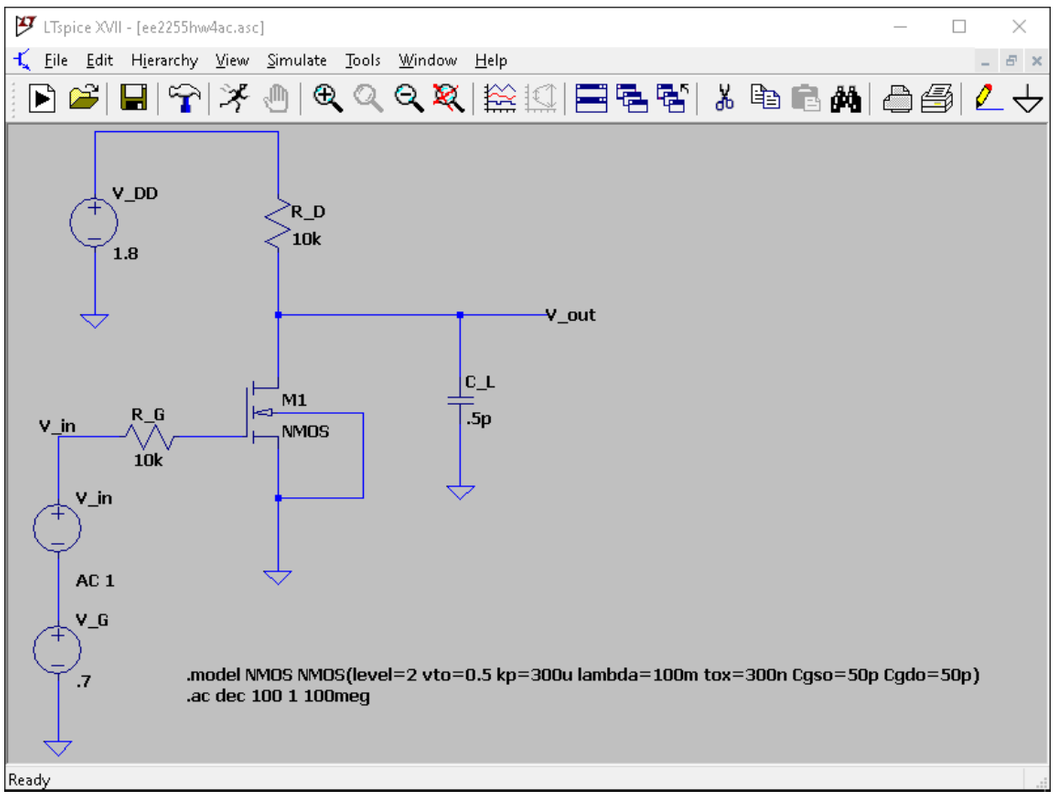

Figure 1: This is the schematic for the AC analysis. I designed the gate voltage and the drain resistor to be $V_G = 0.7V$ and $R_D = 10k\Omega$ respectively.

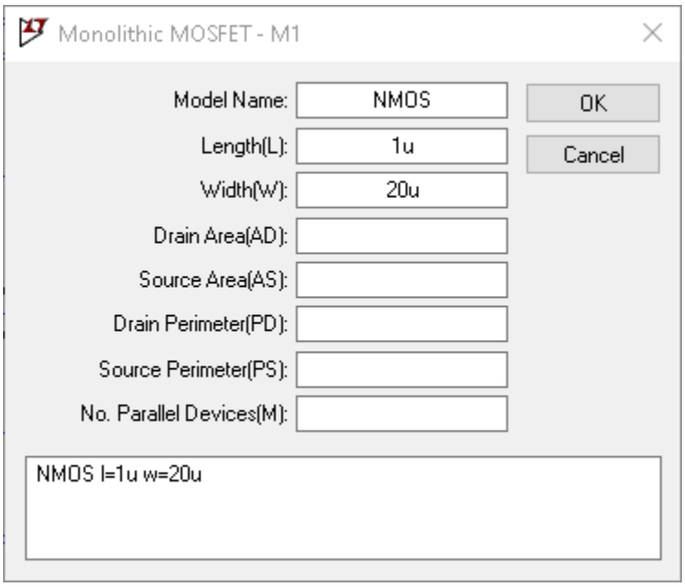

Figure 2: I designed the width of the NMOS to be $W = 20\mu m$.

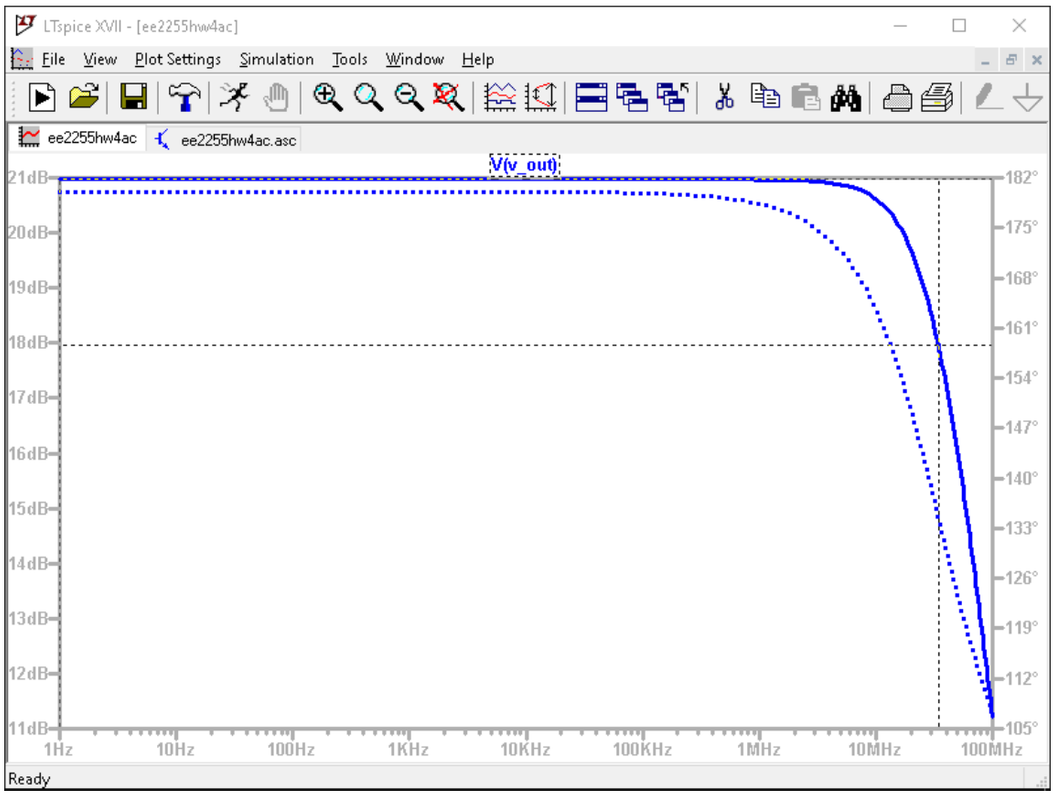

Figure 3: Cursor 1 and 2 in the bode plot are placed at 1Hz and 34.35MHz respectively.

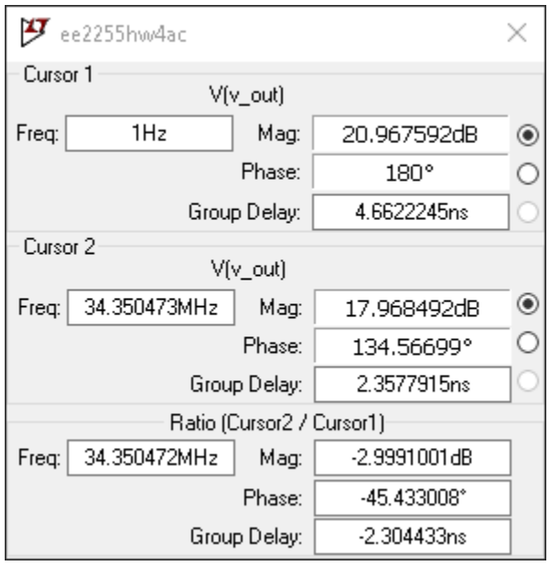

Figure 4: The data extracted by cursor 1 show that the small-signal gain at low frequency is larger than 20dB. The ratio shows that the -3dB-bandwidth is wider than 30MHz.

$$\texttt{small-signal gain}\ (V/V) = 10^{\frac{20.967592dB}{20dB}} = 11.178 > 10$$

2 Transient Analysis

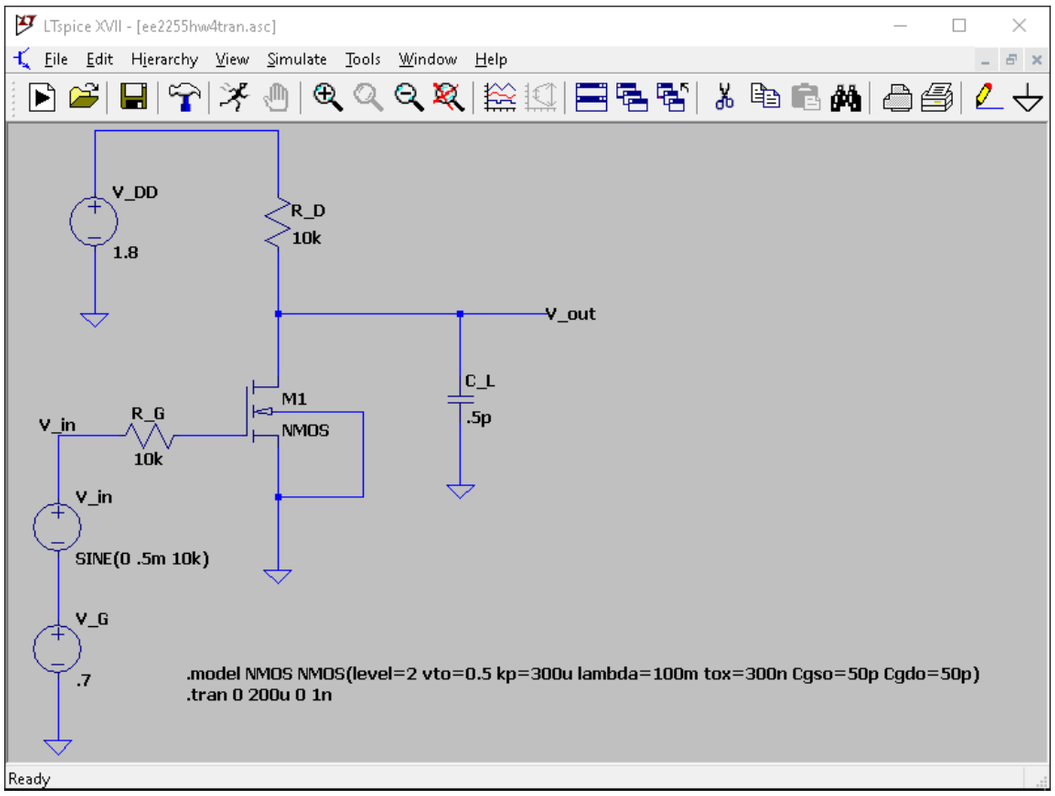

Figure 5: This is the schematic for the transient analysis. The only differences from Figure 1 are the voltage source syntax `SINE(0 .5m 10k)` and the simulation command `.tran 0 200u 0 1n` set.

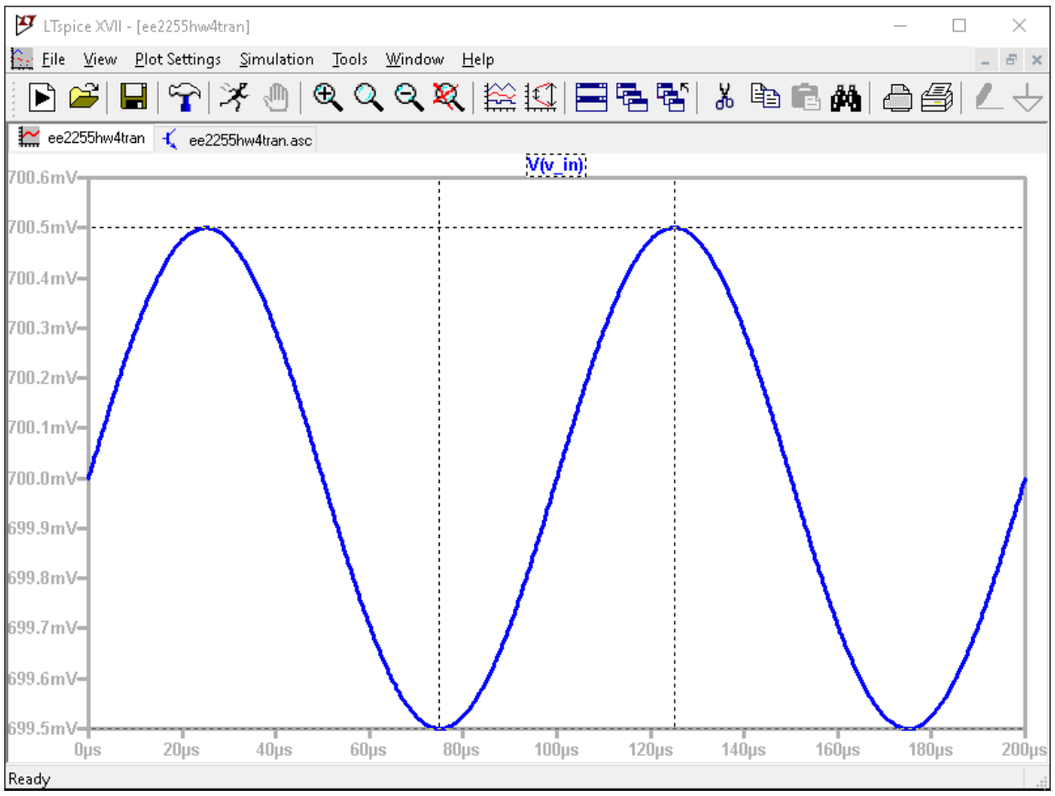

Figure 6: Cursor 1 and 2 are placed at the wave trough and the wave crest respectively.

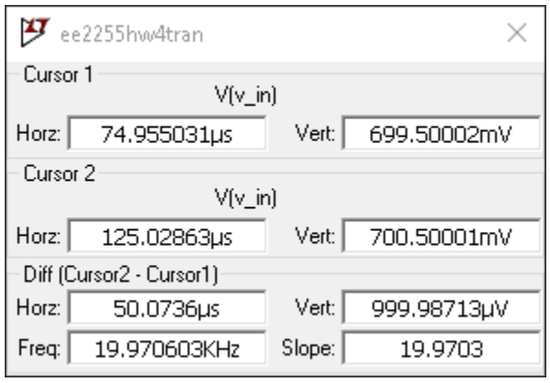

Figure 7: V_{in} is a sine wave with frequency $f = 10kHz$ and peak-to-peak amplitude $V_{p-p} = 1mV$.

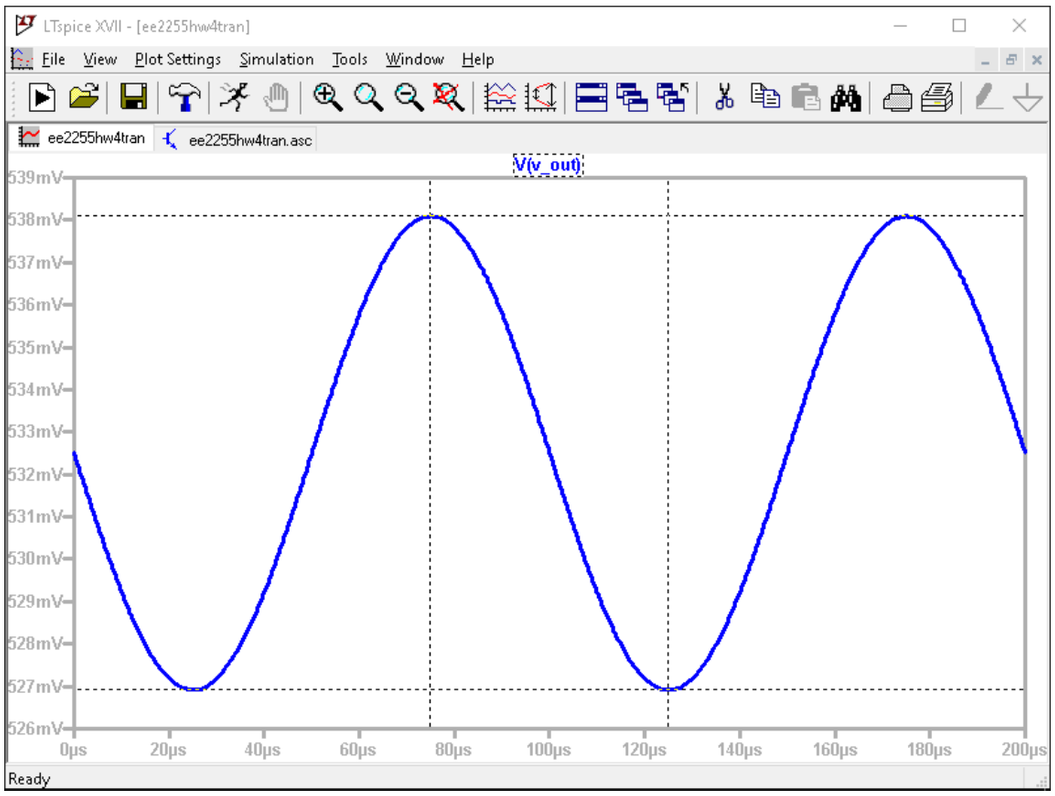

Figure 8: Cursor 1 and 2 are placed at the wave crest and the wave trough respectively.

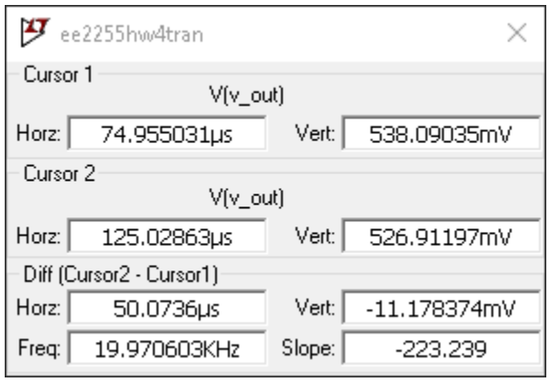

Figure 9: The diff shows that the small-signal voltage gain is larger than 10V/V.

The SPICE directive in Figure 5 sets $V_{TH} = \texttt{vto} = 500.0mV$. The data extracted by cursor 1 in Figure 7 show that $min(V_{GS}) = 699.5mV$. The gate voltage exceeds the threshold voltage so

$$V_{GS} > V_{TH}$$

holds. The data extracted by cursor 2 in Figure 7 show that $max(V_{GS}) = 700.5mV$. The data extracted by cursor 2 in Figure 9 show that $min(V_{DS}) = 526.9mV$. In the worse case scenario, $max(V_{OV}) = max(V_{GS}) - V_{TH} = 200.5mV$. The drain voltage exceeds the overdrive voltage so

$$V_{DS} > V_{OV}$$

holds. Hence the NMOS operates in saturation region.

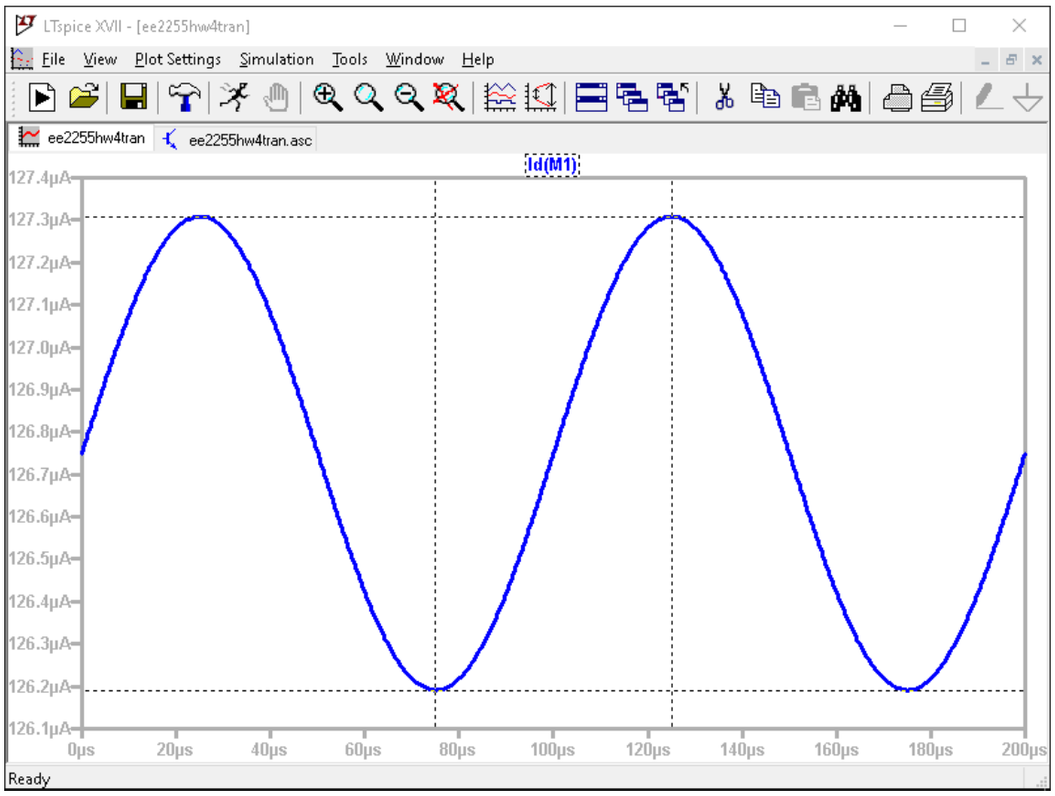

Figure 10: Cursor 1 and 2 are placed at the wave trough and the wave crest respectively.

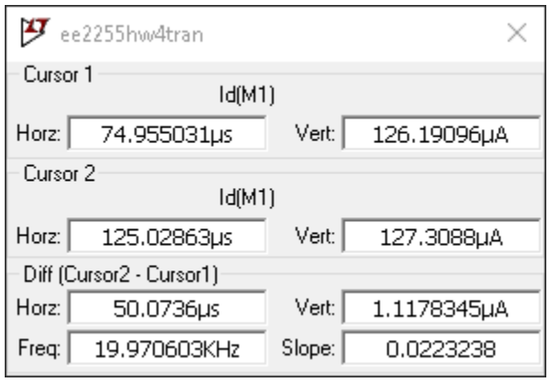

Figure 11: The data extracted by cursor 1 and 2 show that $min(I_D) = 126.2\mu A$ and $max(I_D) = 127.3\mu A$ respectively. The DC offset of the drain current is $[min(I_D) + max(I_D)]/2 = 126.75\mu A$.

3 Figure of Merit

The figure of merit of the common-source amplifier with gate voltage $V_G = 0.7V$, drain resistor $R_D = 10k\Omega$, and NMOS width $W = 20\mu m$ is

$$\texttt{FoM} = \frac{\texttt{gain}(V/V) \times \texttt{bandwidth}(MHz)}{\texttt{drain-current}(mA)}$$

$$= \frac{11.178 \times 34.35}{0.12675} \approx 3029 > 800.$$

Appendix

For the interested reader, I provide here a brief introduction to my attempt to maximize the figure of merit, although these are not referred to elsewhere in the homework assignment. Through some tedious fine-tuning, I found a local maximum for the function

$$\texttt{FoM}(V_G, R_D, W)$$

at

$$V_G \approx 0.5135V$$

$$R_D \approx 7.2863k\Omega$$

$$W \approx 282.5\mu m$$

subject to the specifications

$$\texttt{gain}(V_G, R_D, W) > 20dB$$

$$\texttt{bandwidth}(V_G, R_D, W) > 30MHz.$$

The figure of merit of the common-source amplifier with gate voltage $V_G = 0.5135V$, drain resistor $R_D = 7.2863k\Omega$, and NMOS width $W = 282.5\mu m$ is

$$\texttt{FoM} = \frac{\texttt{gain}(V/V) \times \texttt{bandwidth}(MHz)}{\texttt{drain-current}(mA)}$$

$$= \frac{10.000^{+} \times 30.000^{+}}{0.0093528} \approx 32076 \gg 800,$$

where the data were extracted by the cursors as shown in Figure 12 and Figure 13.

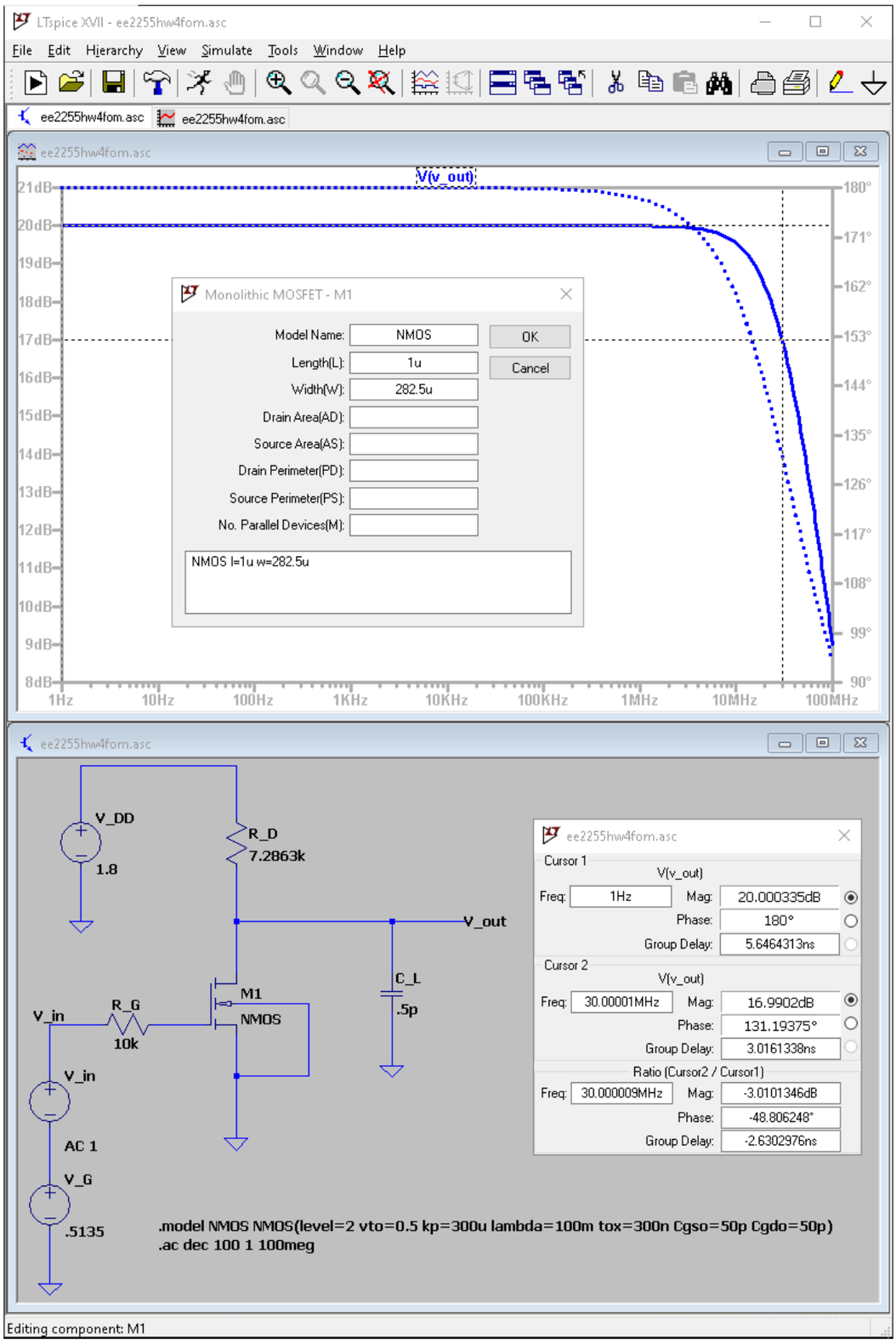

Figure 12: After fine-tuning, the data extracted by cursors show that the small-signal gain is a little bit larger than 20dB and the -3dB-bandwidth is a little bit wider than 30MHz. Note that the exact value of the half-power bandwidth is $20log_{10}\frac{1}{\sqrt{2}} \approx -3.0103$.

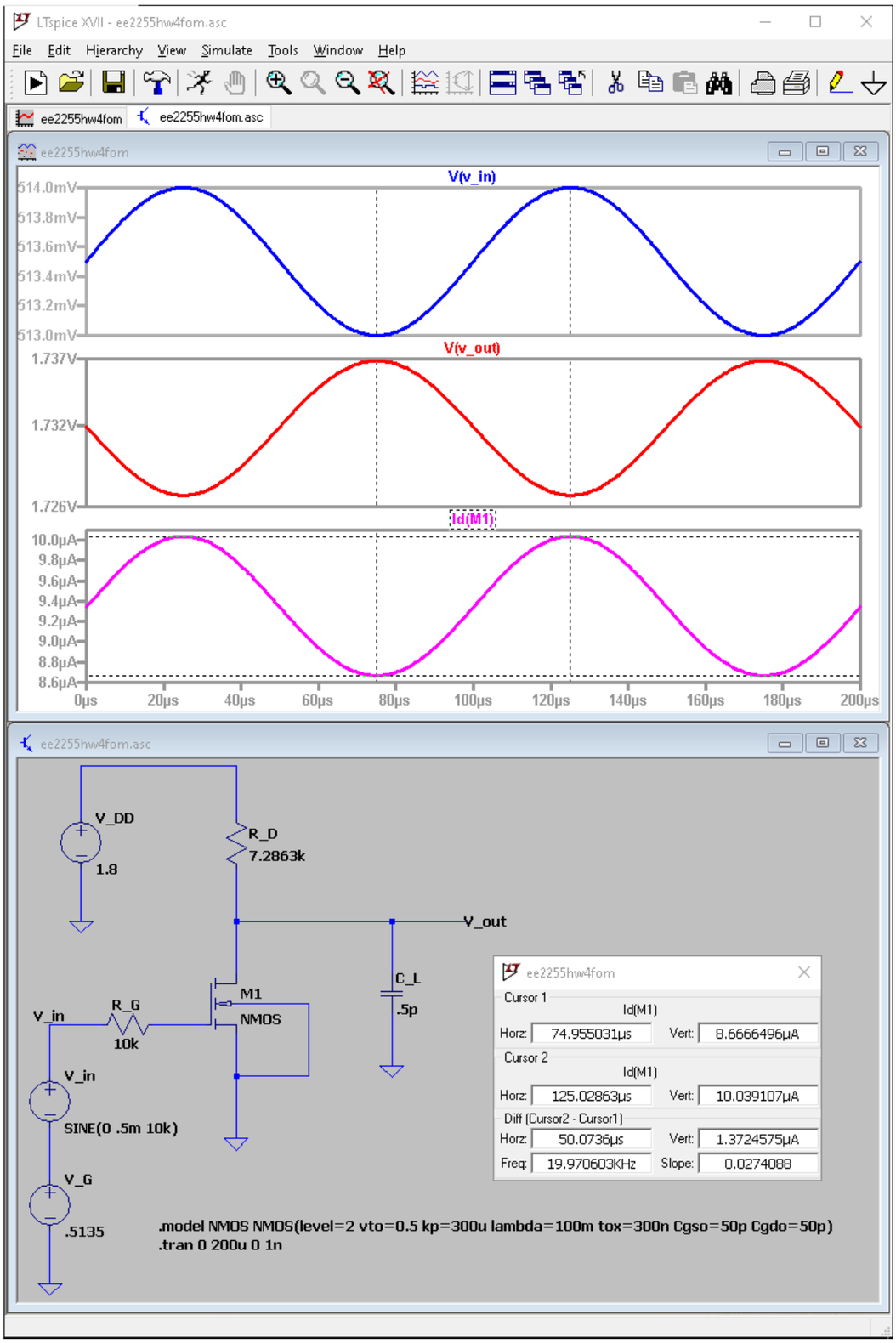

Figure 13: The data extracted by cursor 1 and 2 show that $min(I_D) = 8.6666\mu A$ and $max(I_D) = 10.039\mu A$ respectively. The DC offset of the drain current is $[min(I_D) + max(I_D)]/2 = 9.3528\mu A$. Note that $1726mV > 514mV - 500mV$ and $513mV > 500mV$ so the threshold voltage, the gate voltage, and the drain voltage satisfy $V_{DS} > V_{OV}$ and $V_{GS} > V_{TH}$ in the worse case scenario. Hence the NMOS operates in saturation region.