EECS1010 Logic Design
Lecture 7 Memory 不考

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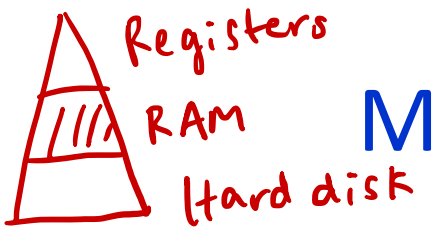
Outline

- Digital systems and information
- Boolean algebra and logic gates
- Gate-level minimization
- Combinational logic
- Sequential circuits
- Registers and counters
- Memory



Memory Definitions (1/3)

- Memory: a collection of cells capable of storing binary information together with necessary circuits to transfer information.
- Read operation: transfers the stored information out of memory.
- Write operation: stores new information into memory.
- Random Access Memory (RAM): a memory that can transfer data to or from any cell with the same access time.

16 bits
32 bits
64 bits

Memory Definitions (2/3)

- Memory address: a vector of bits that identifies a particular memory element.

G 10^9 2^{30}

M 10^6 2^{20}

K 10^3 2^{10}

- Typical data elements are:
  - Bit: a single digit
  - Byte: a collection of 8 bits
  - Word: a collection of binary bits whose size is a typical unit of access for the memory.

$2^{30} \times 8$

↓

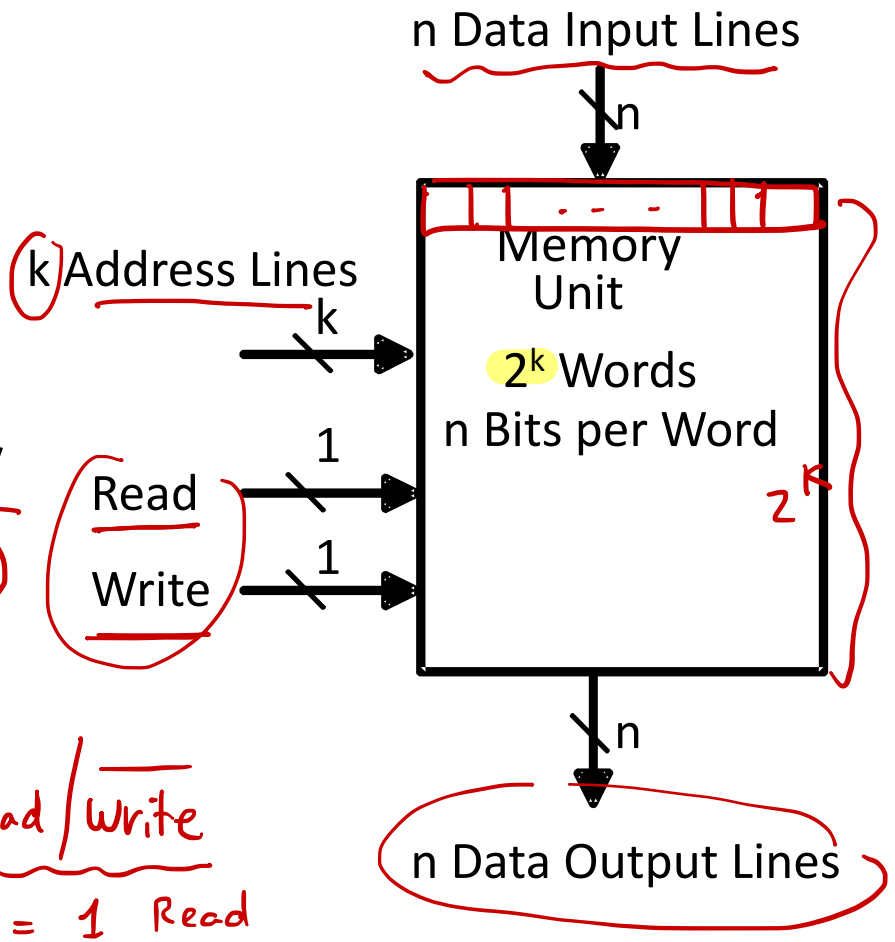
8GB

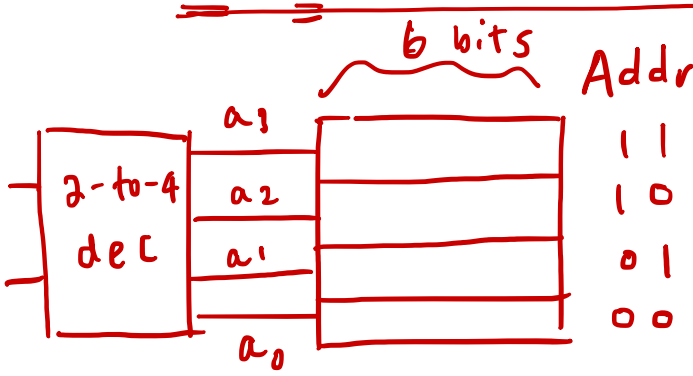
Memory Definitions (3/3)

- RAM: random-access memory
  - Volatile (information lost when power is off)
  - Read/write operation
- ROM: read-only memory
  - Nonvolatile
  - Information in ROM cannot be re-written.

Memory Block Diagram

- I/Os:
  - n data inputs
  - n data outputs
  - k address lines
  - 2 control inputs
- $2^k * n$ (depth*width) memory





$2^2 \times 6$ memory

Read / $\overline{\text{Write}}$

= 1 Read

= 0 Write

Basic Memory Operations (1/2)

- Address of a memory: k bits ($0 \sim 2^k - 1$ words)

k-to-2^k

- Decoder accepts the address and opens the path selected.

- A memory has two parts:
  - Memory cells that store data.
  - Decoding circuits that select the word.

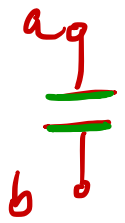
Basic Memory Operations (2/2)

- Read memory – an operation that reads a data value stored in memory.
  - Apply the binary address to the address line.
  - Activate the read control input.

- Write memory – an operation that writes a data value to memory.
  - Apply the binary address to the address line.
  - Apply the data to the data input lines.
  - Activate the write control input.

Memory Integrated Circuits

- Types of random access memory (RAM)
  - Static: information stored in latches. (SRAM)
  - Dynamic: information stored as electrical charges on capacitors. (DRAM)



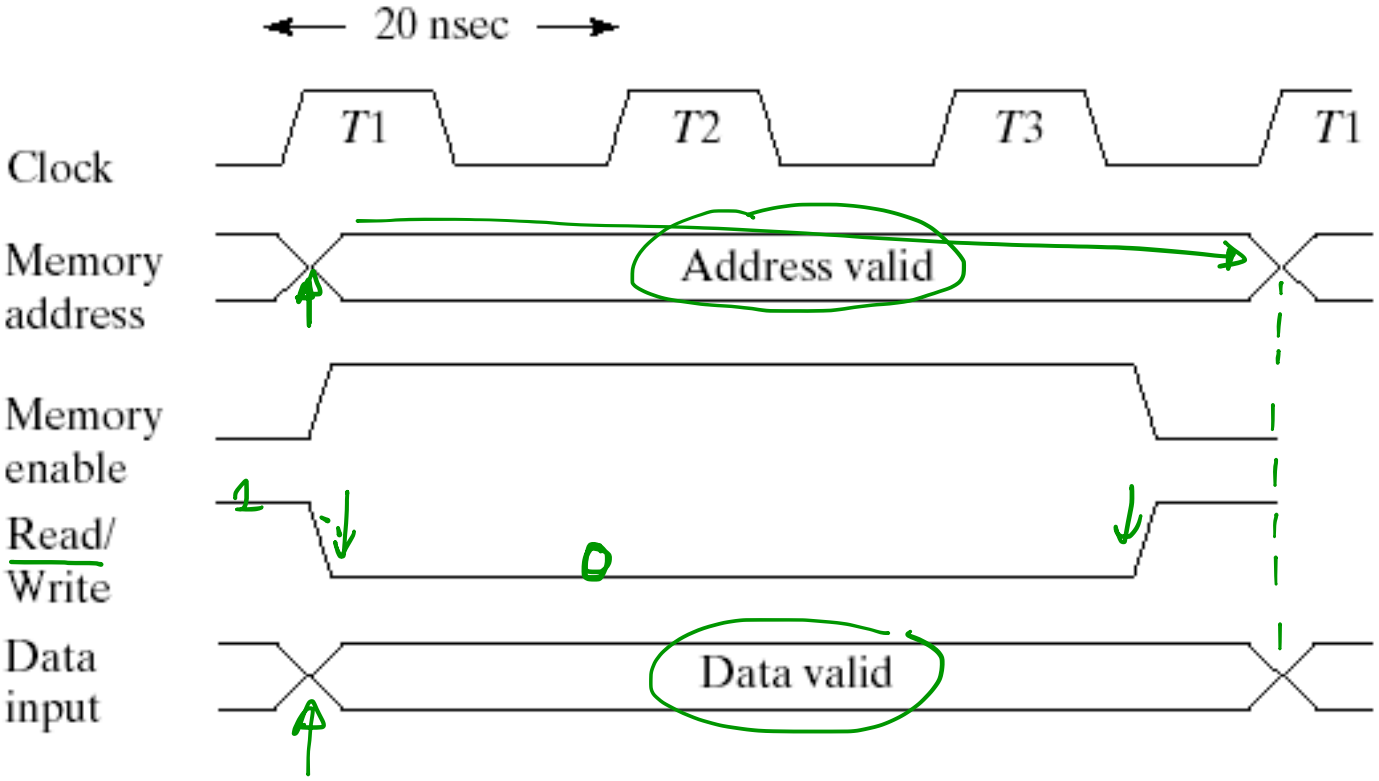
- Dependence on power supply
  - Volatile: information is lost when power turns off. RAM
  - Non-volatile: retains information when power is off. ROM. Flash

Timing of Memory

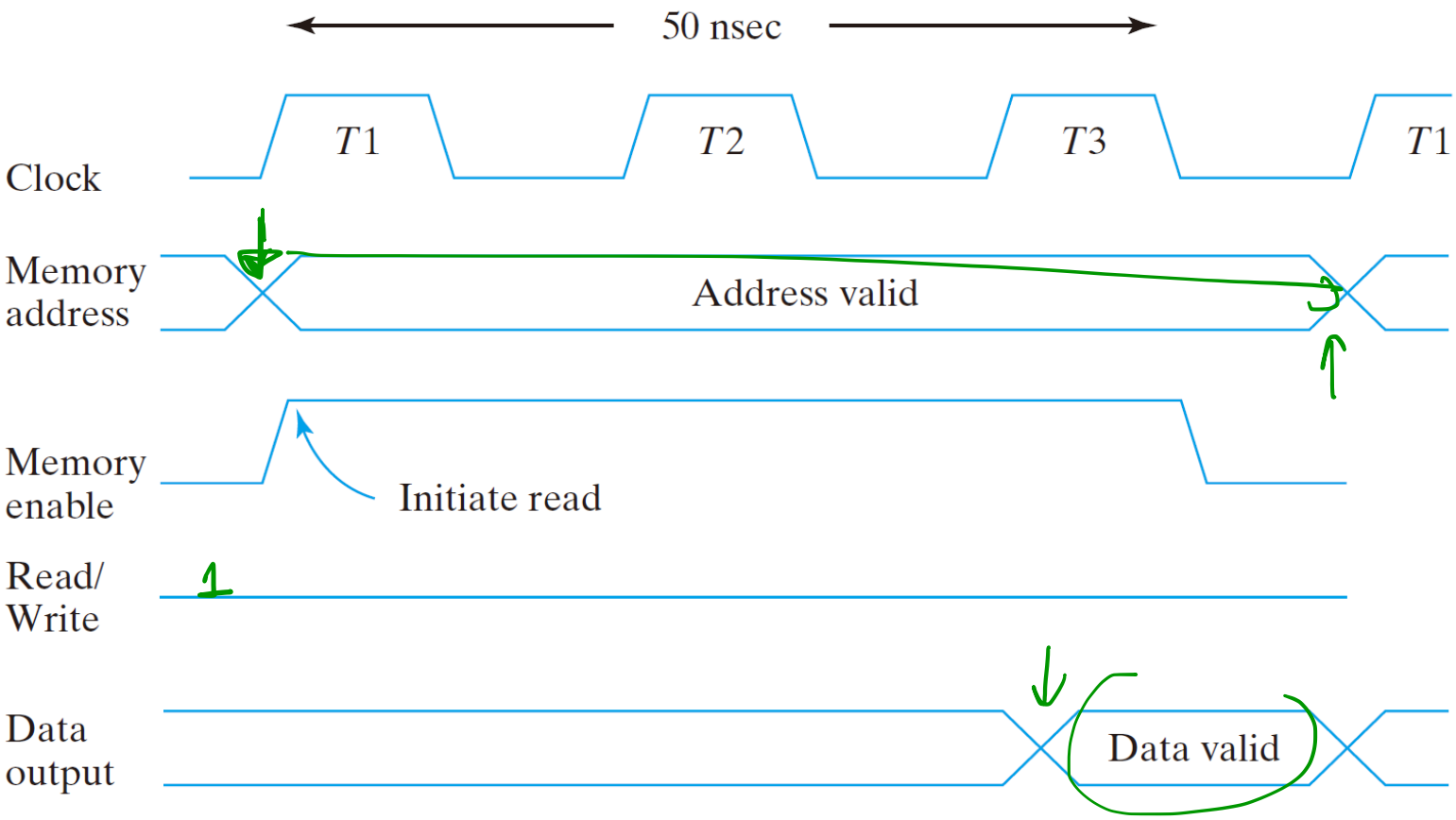
- The operation of a memory unit is controlled by an external device such as a CPU.
- The access time is the time required to select a word and read it.
- The write cycle time is the time required to complete a write operation.
- Read and write operations are controlled by a CPU and synchronized with a clock.

The Write Cycle

- At T1: provides the address and input data to the memory and the read/write control signal.

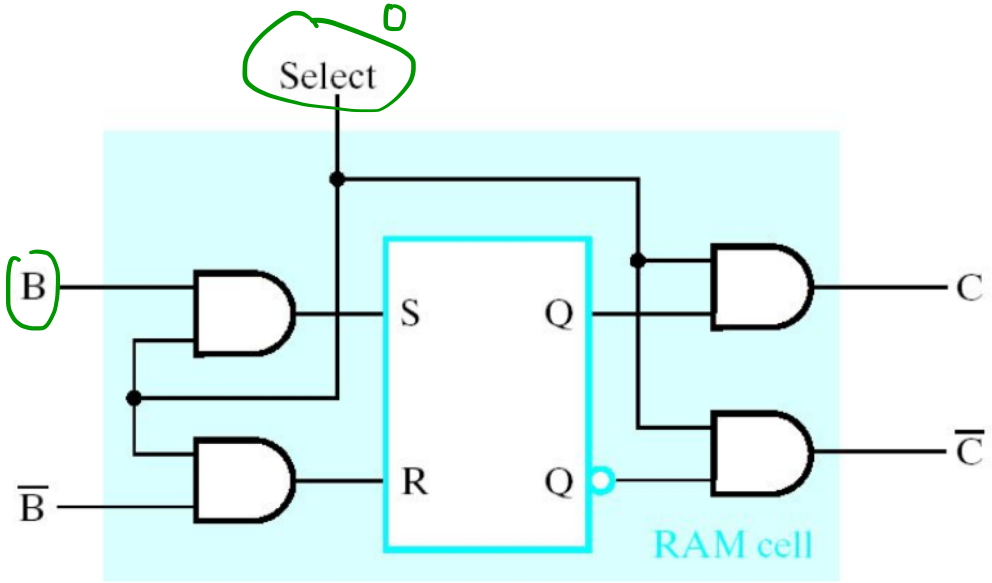


The Read Cycle



Static RAM Cell

- Array of storage cells used to implement static RAM.
- Storage cell : SR latch, ANDs

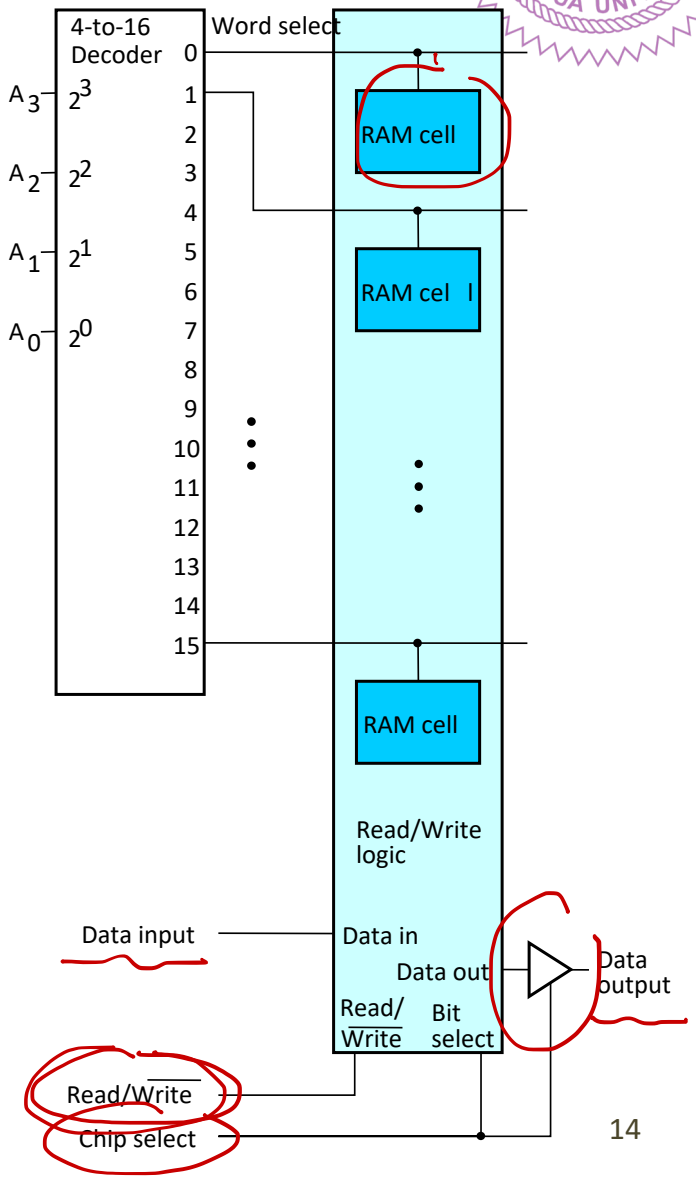


Function table

Select	B	C	$\overline{C}$	
0	X	0	1	
1	0	0	1	reset
1	1	1	0	set

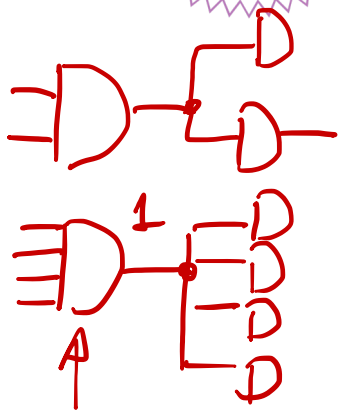
16-Word × 1-Bit RAM IC

- I/Os:
  - 4 address inputs (A_3, A_2, A_0, A_1)
  - Data input (1 bit)
  - Data output (1 bit)
  - Read/$\overline{\text{write}}$ control input
  - 4-to-16 decoder
  - 16 RAM cells



Cell Arrays and Coincident Selection (1/2)

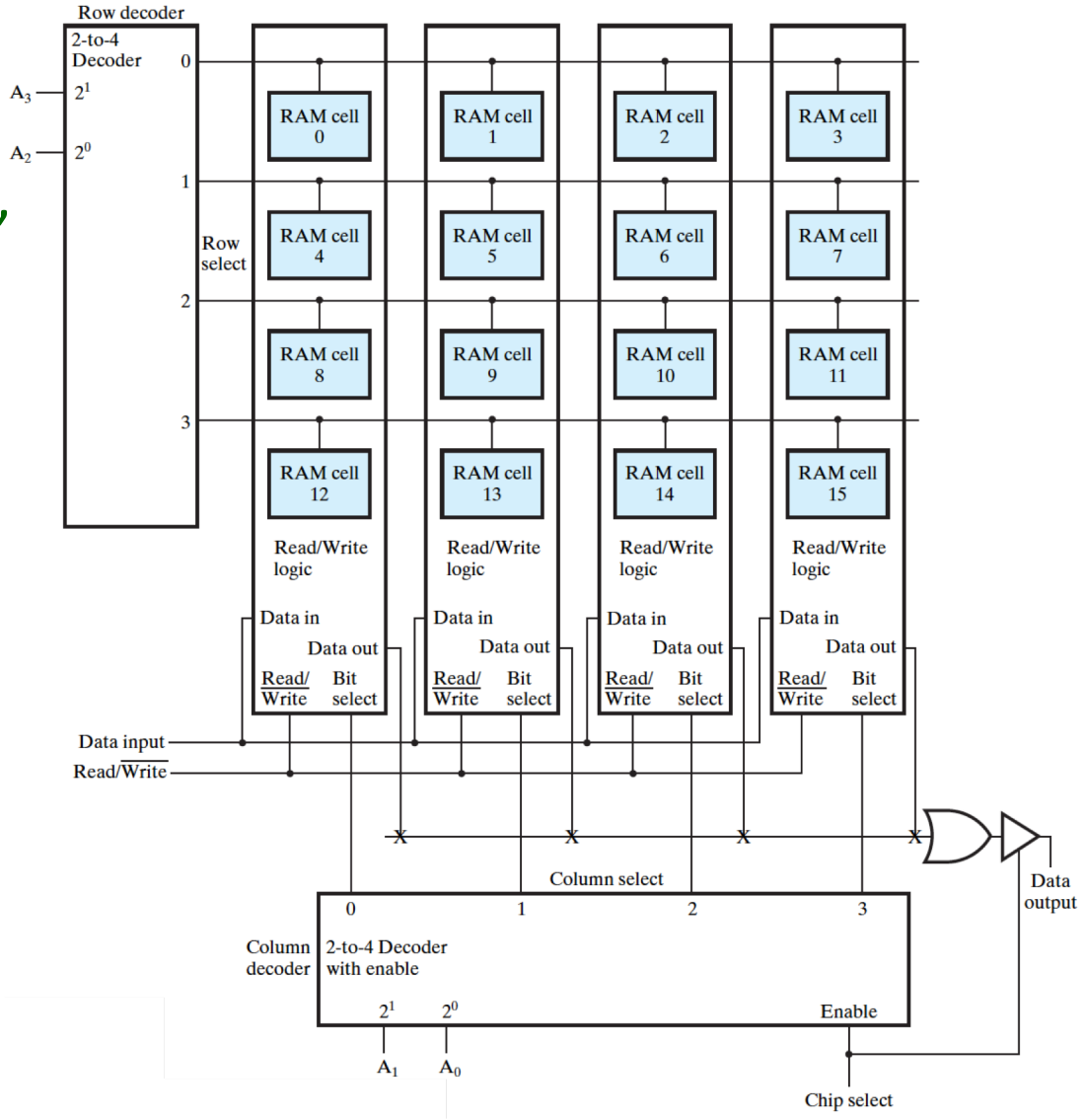
- Memory arrays can be very large
  - Large decoder: K-to-2^K
  - Read/$\overline{\text{Write}}$ shared by many RAM cells



- The decoder size and the number of inputs per gate can be reduced by using a coincident selection in a 2D array.

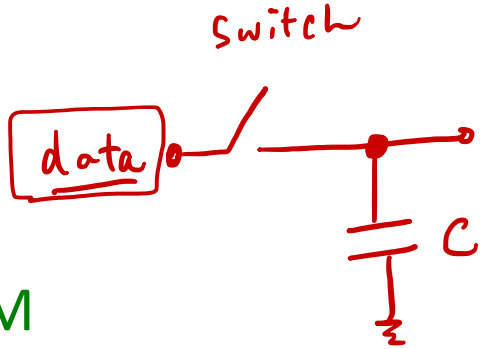
Cell Arrays and Coincident Selection (2/2)

- Instead of one 4-to-16 line decoder, use two 2-to-4 line decoders.

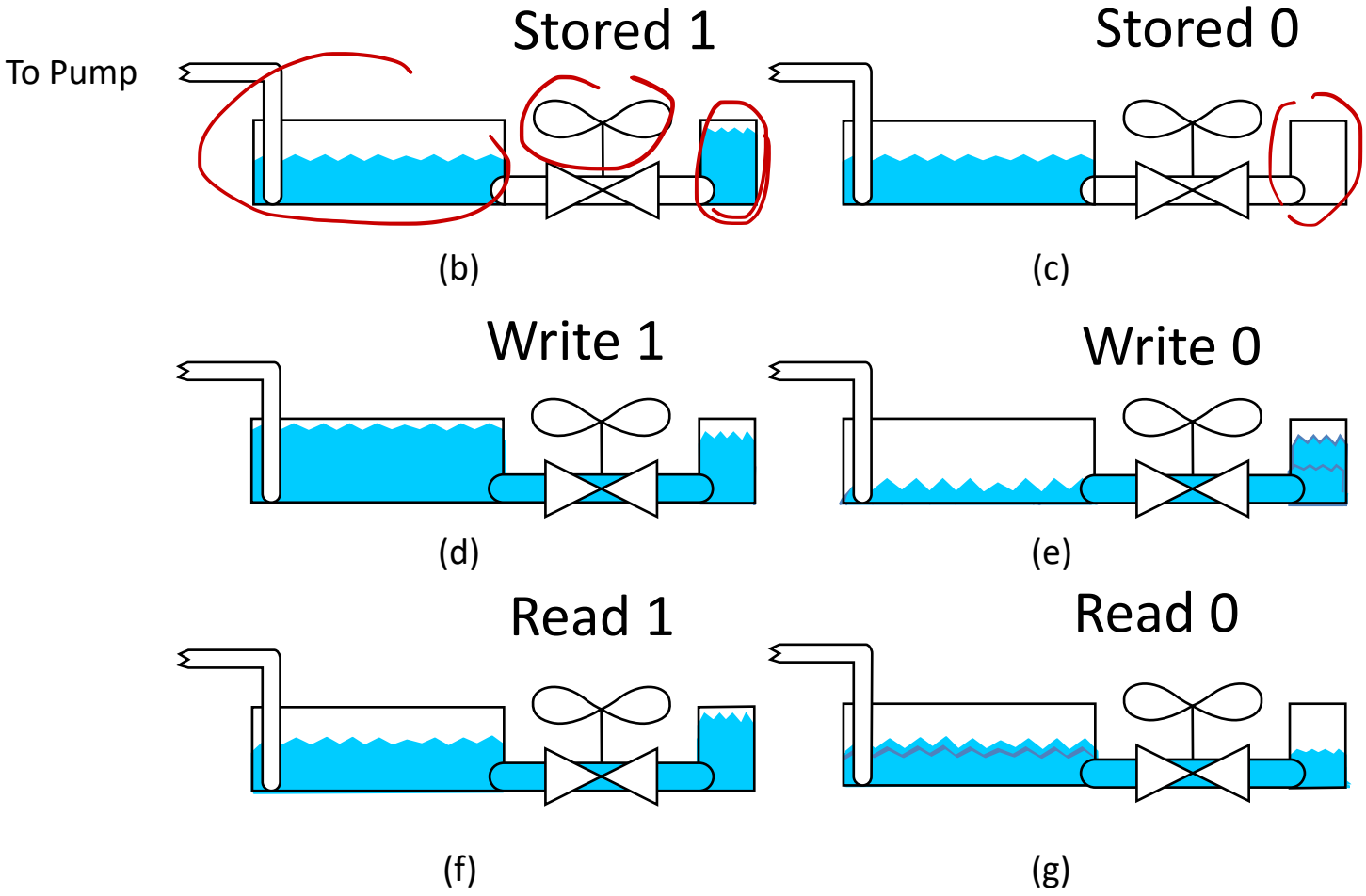


Dynamic RAM (1/2)

- DRAM: stores information temporarily
  - High storage capacity
  - Low cost
  - Design is more challenging than SRAM
  - Needs periodically refresh
- Basic principle: charge and discharge the capacitor



Dynamic RAM (2/2)

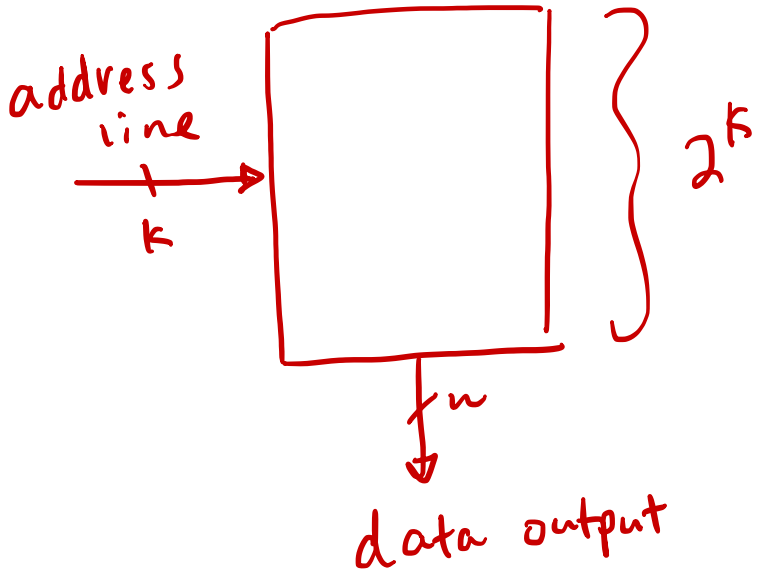


SRAM vs. DRAM

- SRAM
  - 6 transistors
  - Faster access time
- DRAM
  - 1 transistor + 1 capacitor
  - Slower access time
  - Smaller area
  - Smaller power
  - Higher storage capacity
  - Destructive read

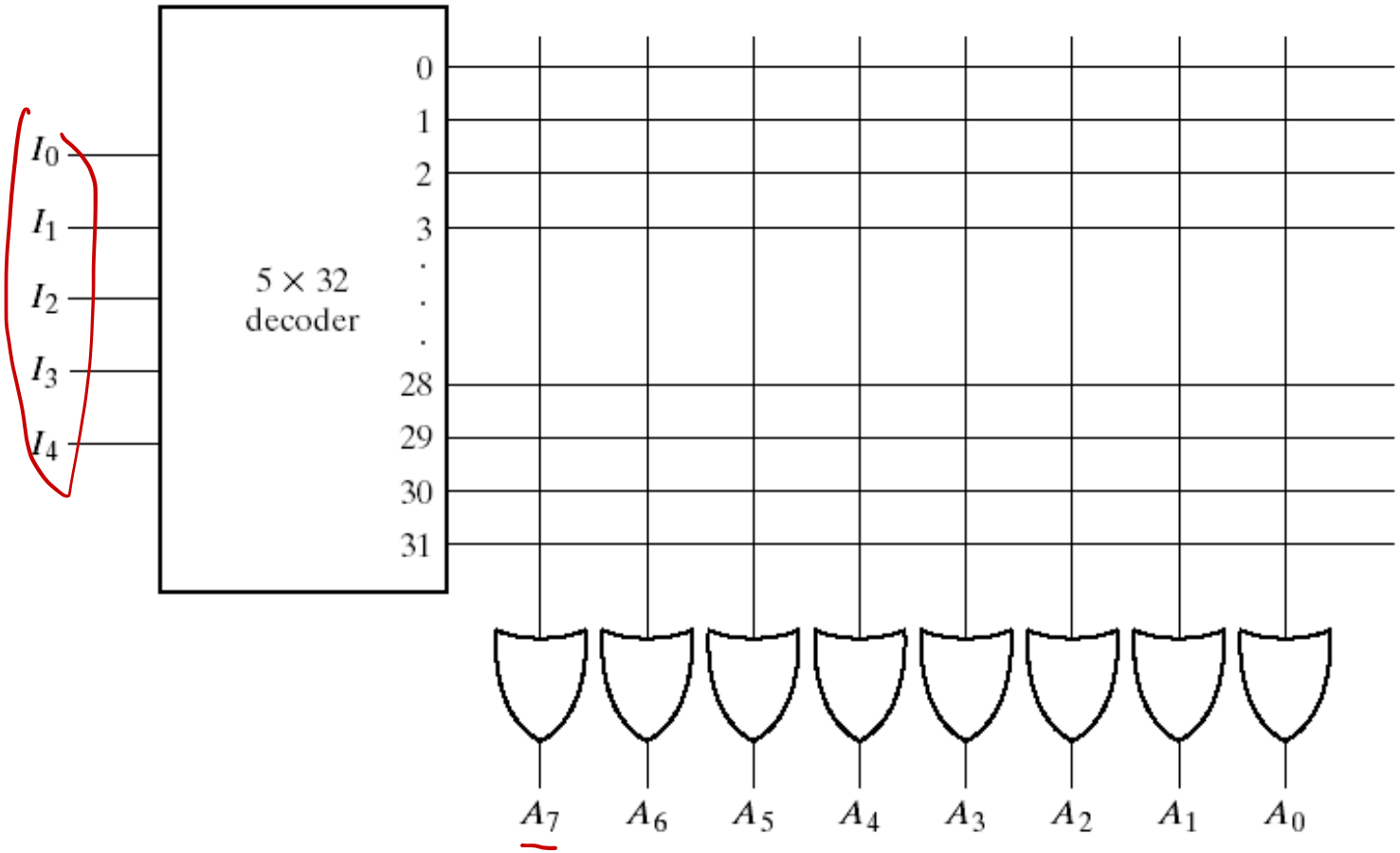
ROM

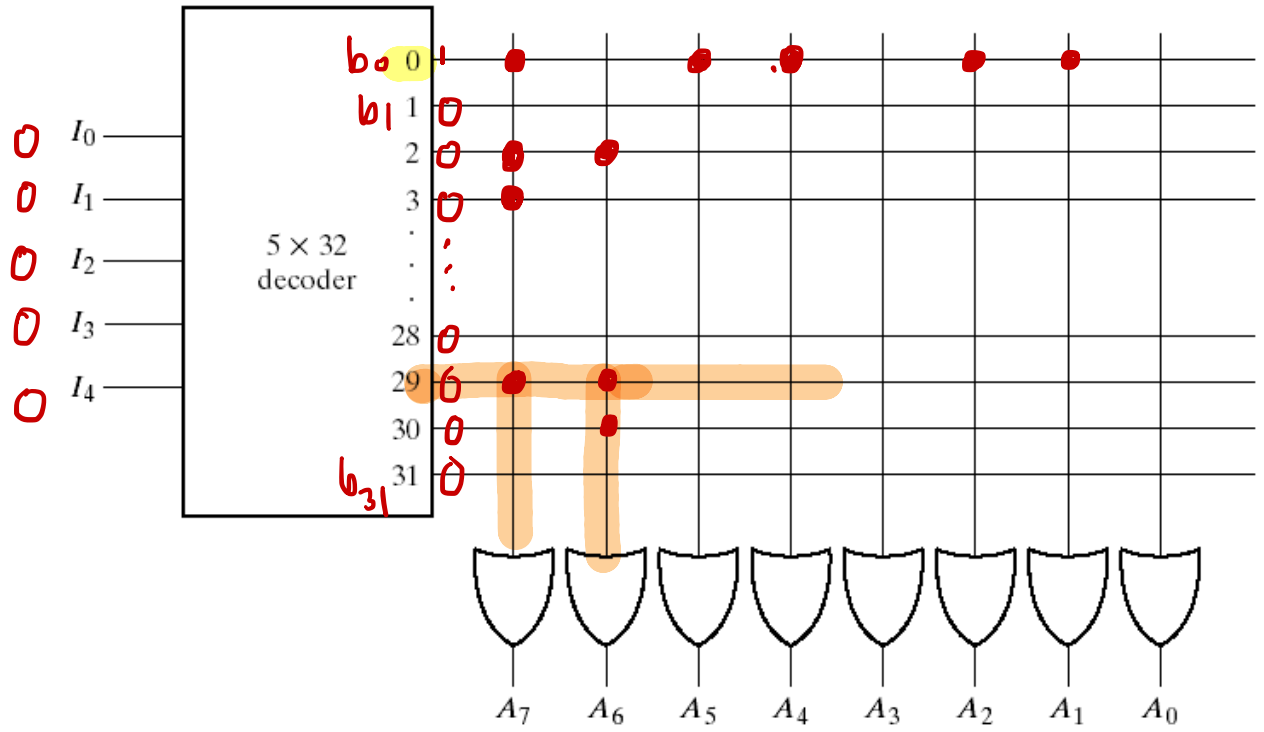
- Read-only memory: stores the information permanently.
- The data stores in ROM whether the power is on or off.
- 2^k * n ROM



ROM: decoder + OR gates.

ROM Example $2^5 \times 8$ bits





Inputs					Outputs							
I4	I3	I2	I1	I0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮					⋮					
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Combinational Circuit Implementation

- ROM: decoder + OR gates
- For n-input, m-output combinational circuit, we can use $2^n \times m$

(n-to-2^n decoder, m OR gates)