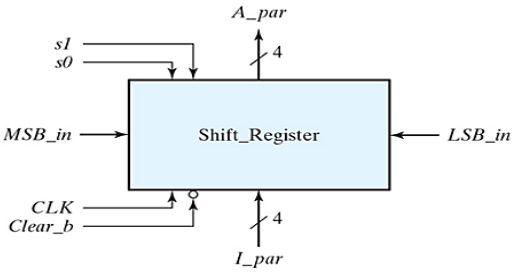
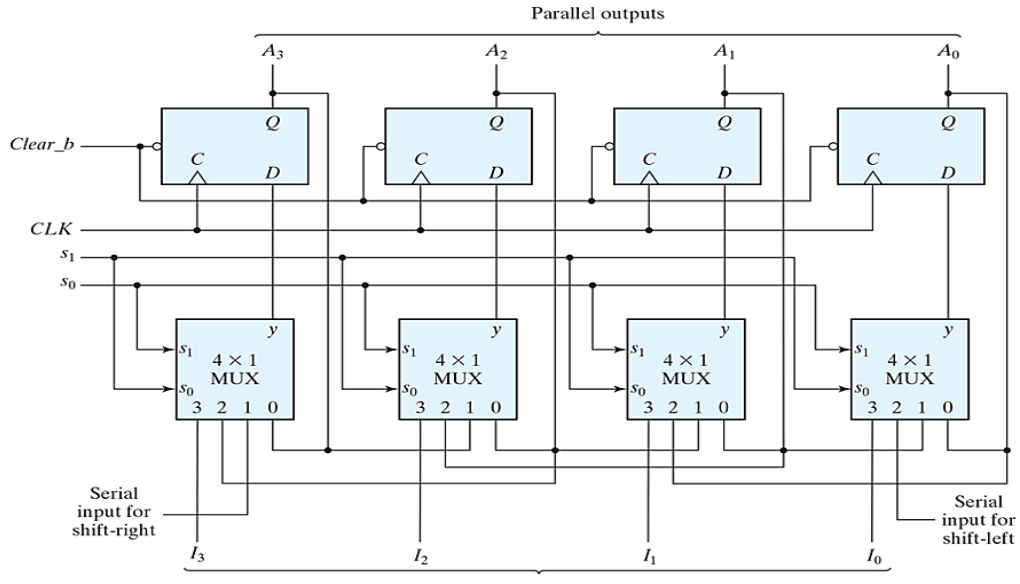
EECS1010 Logic Design Spring 2023
Homework 6

Due: **2:20pm on May 25th, 2023** (before the class starts). No late homework.
For each question, please write down the thinking/calculation process. No credit will be given if only answer without process is provided.

1. Using a 4-bit register, construct a 4-bit shift register that can shift/rotate its content one position to the left or right with asynchronous reset. (20%)
2. Design a modulo-9 counter using D FFs, with the counting sequence (0, 1, 2, 3, 4, 5, 6, 7, 8, 0, 1, ...), which produces $y = 1$ if the state '8' is encountered (i.e., when we go from state '8' to state '0'), and $y = 0$ otherwise. The counter stays in its current state iff $C = 0$, and makes state transition iff $C = 1$. You can use only D FFs. Show the state diagram and minimized state table, then derive the simplified output and excitation functions. Finally, show the schematic. (20%)
3. Construct an 8-bit universal shift register from 4-bit registers as shown below. (20%)



(a)



(b)

4. The content of a 5-bit shift register is initially 10101. The register is shifted five times to the left with the serial input 10101 (left bit is first input). What is the content of the register after *each shift*?
5. Use D flip-flops and gates to design a binary counter with each of the following repeated binary sequences. (20%)

   (a) 1, 4, 7

   (b) 0, 2, 4, 6, 7