EECS1010 Logic Design Spring 2023
Homework 5

Due: **2:20pm on May 18th, 2023** (before the class starts). No late homework.
For each question, please write down the thinking/calculation process. No credit will be given if only answer without process is provided.

1. Consider the timing diagram in Figure 1(a). D and Clock are the inputs to the circuits in Figure 1(b). Draw the waveforms of the Q_a, Q_b, and Q_c. (12%)

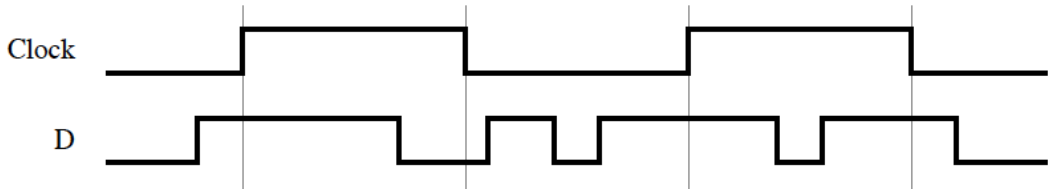


Figure 1(a)

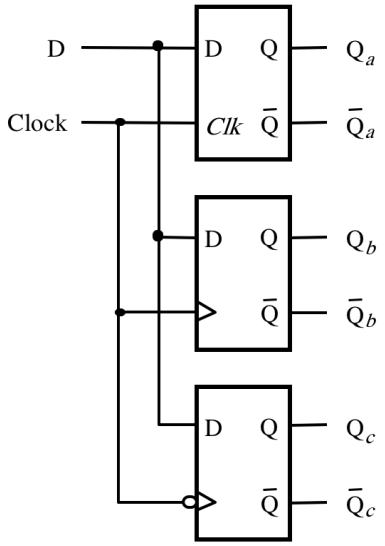


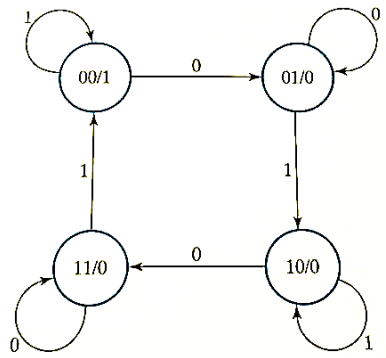
Figure 1(b)

2. Reduce the number of states in the following state table and tabulate the reduced state table. Assume the initial state is state A. Show the output sequence when the input sequence is 11010101001. (12%)

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	B	0	0
B	D	E	1	0
C	F	E	0	0
D	G	A	1	0
E	D	E	1	0
F	F	B	1	1
G	G	A	1	0

H	G	C	0	0

3. A sequential circuit has two flip-flops A and B, one input x and one output z. The state diagram is shown in the following figure. Design the circuit with D flip-flops using Gray code state assignment. (14%)



4. A sequential circuit with two *D* flip-flops A and B, two inputs *X* and *Y*, and one output Z is specified by the following input equations:

   D_A=X'B'+XY', D_B=A'+Y'B, Z=YA'B.

   Draw the logic diagram, derive the state table and the state diagram of this circuit. (14%)

5. Find the state machine diagram corresponding to the following description: There are two states, A and B. If in state A and input X is 1, then the next state is A. If in state A and input X is 0, then next state is B. If in state B and input Y is 0, then the next state is B. If in state B and input Y is 1, then the next state is A. Output Z is equal to 1 while the circuit is in state B. (14%)

6. A T flip-flop has a single input. When the input is 0, it holds the current value. When the input is 1, it toggles the stored value. (a) Show the function table and Boolean expression of a T flip-flop. (b) Show how to implement a D flip-flop with a T flip-flop. (14%)

7. Design a recognizer that recognizes an input sequence that has at least three 1's. The recognizer has a single input X, and a single output Y, and one asynchronous Reset input signal. The recognizer sets the output Y to 1 if the input signal X was equal to 1 in at least 3 clock cycles after reset. Provide the design flow and draw the logic diagram. (20%)