EECS1010 Logic Design Spring 2023

Homework 4

Due: **1:20pm on May 9th, 2023** (before the class starts). No late homework.
For each question, please write down the thinking/calculation process. No credit will be given if only answer without process is provided.

1. Design a four-bit 2's complementor with simplified Boolean function and logic diagram. (The output generates the 2's complement of the input binary number.) (20%)
2. Design a 3-to-8 decoder with an enabling function using only NOR and NOT gates. When the decoder is disabled, the outputs are 0. (20%)
3. Design a 4-to-2 priority encoder with input D[3:0] and output A[1:0] where D_0 has the highest priority and D_3 has the lowest priority. (20%)
4. Design a three-way magnitude comparator that outputs true if its three inputs are in strict order: a<b<c. a, b, and c are all three-bit signed 2's complement numbers. (20%, each 10%)
5. Design a 4x3 multiplier. The multiplicand has 4 bits and the multiplier has 3 bits. (20%)